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EVALUATION OF CAPACITANCE-VOLTAGE SPECTROSCOPY BY CORRELATION WITH MINORITY CARRIER LIFETIME MEASUREMENTS OF PECVD-DEPOSITED INTRINSIC AMORPHOUS LAYERS

Sebastian Gerke[1], Axel Herguth[1], Nils Brinkmann[1], Giso Hahn[1], Reinhart Job[2]
[1]University of Konstanz, Department of Physics, 78457 Konstanz, Germany
[2] Münster University of Applied Sciences, Department of Electrical Engineering and Computer Science, 48565 Steinfurt, Germany
sebastian.gerke@uni-konstanz.de, Tel.: +49 (0)7531 / 88-2260, Fax: +49 (0)7531 / 88-3895

ABSTRACT: Thick (150 nm) hydrogenated intrinsic amorphous silicon ((i) a-Si:H) layers, which are deposited with different recipes on crystalline silicon (c-Si) by plasma enhanced chemical vapour deposition (PECVD) are investigated by minority carrier lifetime measurements (τ_{eff}) and capacitance-voltage C(V) spectroscopy during thermal treatment. The minority carrier lifetime measurements permit an evaluation of the surface passivation and thus the saturation of defects like dangling bonds at the (i) a-Si:H/c-Si interface. The capacitance difference between high and low frequency curves is a measure for the combination of the defects in the (i) a-Si:H bulk as well as at the (i) a-Si:H/c-Si interface. An evaluation of the sensitivity of the C(V) measurement is carried out by correlating these with minority carrier lifetime measurements during thermal treatment. The results of the measurements suggest that a direct correlation between the quality of defect passivation at the interface and in the bulk is not possible. The contribution of the interface defects to the difference in capacity is smaller than the resolution of the C(V) measurement. Imperfections in the structure of the (i) a-Si:H layer probably microvoids affect the bulk defects and the resulting differences in capacity more than changes at the (i) a-Si:H/c-Si interface. An investigation of the Si-H_2 content by FTIR measurements supports this suggestion because the content indicates the formation of microvoids.
Keywords: Amorphous Silicon, Annealing, Capacitance, FTIR, Lifetime, Spectroscopy

1. INTRODUCTION

Almost all currently industrially produced crystalline silicon (c-Si) solar cells are based on a pn-homojunction. However, the more advanced heterojunction design for silicon solar cells using hydrogenated amorphous silicon (a-Si:H) in combination with crystalline silicon (c-Si) offers promising features. A hetero-(single)-junction cell is able to exceed the open circuit voltage of homojunction c-Si cells while maintaining a comparable current and fill factor and thus very high efficiencies may be reached with this concept [1, 2].

Compared to a diffused c-Si homojunction it is technologically more challenging to produce an excellent a-Si:H/c-Si heterojunction as the junction is established at the exposed crystal surface making it vulnerable to residual impurities and growth conditions. It is found that doped (p/n) a-Si:H layers deposited directly on c-Si bring along too many defects and therefore an intrinsic interlayer (i) a-Si:H is required to reasonably reduce the interface defect density [1, 2].

The (i) a-Si:H layer and its interface to the c-Si directly after plasma enhanced chemical vapour deposition (PECVD) are far from defect-free and a subsequent defect curing step is required [1-6]. Within this step the bond structure is reorganized and mainly dangling bonds are passivated. Dauwe *et al.* as well as Street [2, 6] have shown that the time span for this curing depends on the temperature. Too high temperatures deteriorate the passivation quality [5]. Common temperatures for the defect curing step in PV applications are ~300°C [1-4]. However, hydrogen diffusion in (i) a-Si:H already sets in at temperatures ~200°C [6, 7].

Schulze *et al.* [1] have observed that for very thin (i) a-Si:H layer a distinction between interface and bulk defects is not possible.

Usually the defect density in a-Si:H layers is determined by Photoelectron Spectroscopy (PES) [3] or Electron Spin Resonance (ESR) [6].

However, a qualitative analysis of the combination of interface and bulk defects should also be possible with capacitance-voltage C(V) spectroscopy [8-12].

In this contribution the sensitivity of C(V) spectroscopy is evaluated. This is done by investigating the behaviour of the surface passivation compared to the total defect quantity for thick (i) a-Si:H layers of different structures during thermal treatment.

The surface passivation quality and its changes are investigated by means of minority carrier lifetime measurements.

The curing was done at 200°C to slow down hydrogen diffusion within and effusion from the (i) a-Si:H layer.

2. SAMPLE PREPARATION

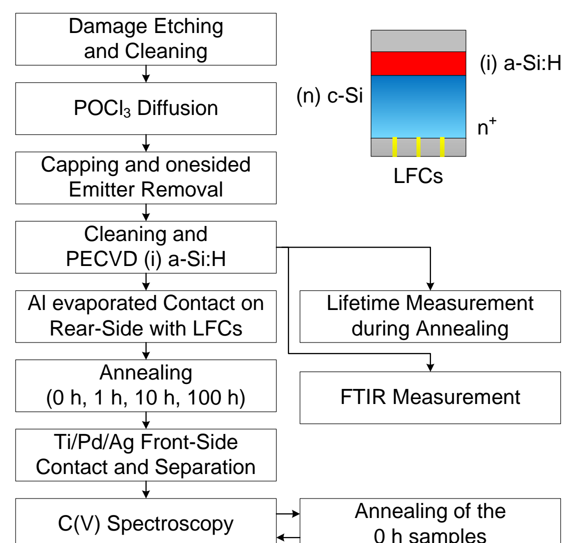

Figure 1: Process flow chart and schematic of the C(V) spectroscopy samples.

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Figure 1 illustrates the below described process flow as well as a schematic of the C(V) spectroscopy samples.

For lifetime and C(V) experiments, phosphorous doped (n-type, 7.5 Ωcm, 250 µm, <100> oriented) floatzone (FZ) silicon wafers with a chemically polished surface were used.

For the C(V) samples a high/low junction was established on both sides via tube furnace $POCl_3$-based diffusion prior to (i) a-Si:H deposition. The resulting n^+/n high-/low junction was etched away on the front side afterwards while the rear side was protected by printed etch resist wax (Inkjet DoD 300, Schmid).

The samples were RCA cleaned and any remaining oxide was removed in diluted HF directly before (i) a-Si:H deposition. Around 150 nm (i) a-Si:H was deposited on both sides of the lifetime samples and only on one side of the C(V) samples, respectively.

The deposition took place in a PlasmaLab 100 direct PECVD reactor from Oxford Instruments at a temperature of 225°C and a pressure of 1000 mTorr (~1,33 mbar). Different recipes (Tab. I) regarding the gas flow of hydrogen (H_2) were used to create layers with different structure. As the concentration of hydrogen during deposition influences the growth and the structure of the (i) a-Si:H [6, 7]. The additional hydrogen leads to a more homogeneous layer because weak Si-Si bonds are broken up by the hydrogen [6].

Table I: Hydrogen gas flow settings for the deposition of 150 nm (i) a-Si:H layers with different structure.

Recipe	(I)	(II)	(III)
H_2	full	half	none

The n^+ diffused rear side of the C(V) samples was coated with electron beam evaporated aluminium as electrical contact. Additional Laser Fired Contacts (LFCs) had been set to reduce resistance. The necessary front side electrode (Ti/Pd/Ag) was added after thermal treatment (discussed in the experiments in chapter 3.2). Both, the front and the rear side contacts were deposited via electron beam evaporation. Finally, the C(V) samples were separated in 4x4 mm² pieces to get a quasi 1D-capacitor structure.

3. EXPERIMENTS AND RESULTS

3.1 Passivation quality

The lifetime samples were placed on a hotplate at 200 ± 2°C in ambient air for defect curing. In order to track the degree of curing (and degradation afterwards), the effective minority carrier lifetime (τ_{eff}) of the samples was measured at room temperature via transient photo conductance decay (WCT 120, Sinton Instruments).

The results of the minority carrier lifetime measurement at an injection level of Δn = 1.0E+15 cm^{-3} and the according maximum surface recombination velocity (SRV) S_{eff} are shown in Figure 2.

As can be seen in the left charts in Figure 2, the effective minority carrier lifetime of all samples rises within the first few minutes, but drops for longer times as expected [1-4], right side of Figure 2. This is ascribed to a reorganisation of atomic hydrogen in the (i) a-Si:H which leads at first to a better passivation of existing defects at the (i) a-Si:H/c-Si interface [1-4]. For longer times the hydrogen effuses and already passivated defects lose their hydrogen [2, 6].

Recipes (II) and (III) yield the highest minority carrier lifetime values even though recipe (I) offers the highest hydrogen flow during deposition. This is related to the hydrogen based reconstruction of the amorphous network during deposition [6, 7]. This reconstruction also affect the layer growth rate so that for same times of deposition the deposited thickness varied from 140 nm for recipe (I) to 152 nm for recipe (II) and 172 nm for recipe (III).

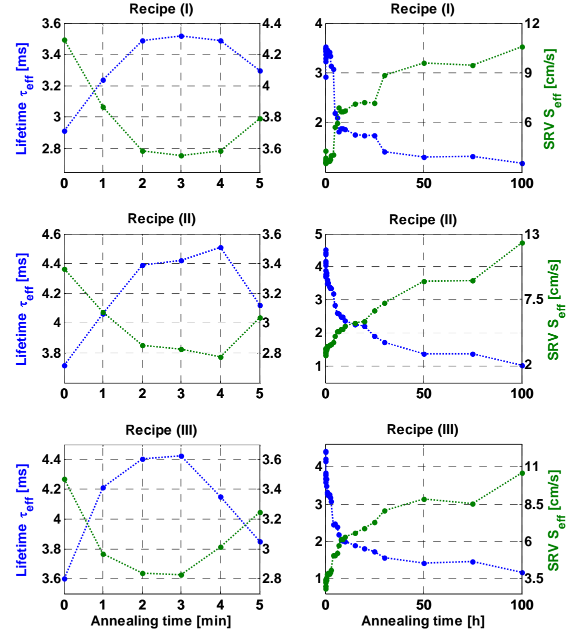

Figure 2: Evolution of the effective minority carrier lifetime τ_{eff} and deduced surface recombination velocity (SRV) S_{eff} during the thermal treatment for different structures of the (i) a-Si:H layers. Lines are guides to the eye.

However the continuation of annealing up to 100 h shows that effective minority carrier lifetimes (τ_{eff}) continuously decrease.

Furthermore, it can be seen in Figure 2 that after 25 h of annealing the minority carrier lifetimes of all samples are in the same range so the passivation quality seems to become nearly the same for all samples.

3.2 Capacitance spectroscopy

A similar experiment was carried out with the C(V) samples. In this case various sub-samples were heated to 200 ± 2°C in ambient air on a hotplate for different curing times in a upside down position of the amorphous layer. Afterwards a front electrode (Ti/Pd/Ag) was deposited via electron beam evaporation.

The voltage dependent capacity was measured at a multitude of frequencies ranging from 50 kHz to 1 MHz with an AC-amplitude of 30 mV. The measurements were done with a HP 4192A impedance analyser at an ambient temperature of 20°C in a light and electrical shielded metering chamber.

An exemplary set of C(V) curves after 100 h of thermal treatment is shown in Figure 3 (top). The general shape of the C(V) curve is determined by the broadening of the space charge region reaching out from the front electrode across the (i) a-Si:H layer into the (n) c-Si [13].

In addition, it can be seen that the capacity features a bump at low voltages which changes its position with frequency. This variation of the capacity is caused by charging and discharging of defect states in the (i) a-Si:H layer [8-12].

With rising frequency certain defects lose the ability to trap and reemit electrons/holes fast enough and thus do not contribute to the capacity any more. The difference in capacity (*ΔC*) between high and low frequency curves is proportional to the defect concentration, containing the defects at the (i) a-Si:H/c-Si interface as well as the defects in the bulk of the (i) a-Si:H layer [8-12]. The evaluation of *ΔC* after several annealing steps can be seen in Figure 4.

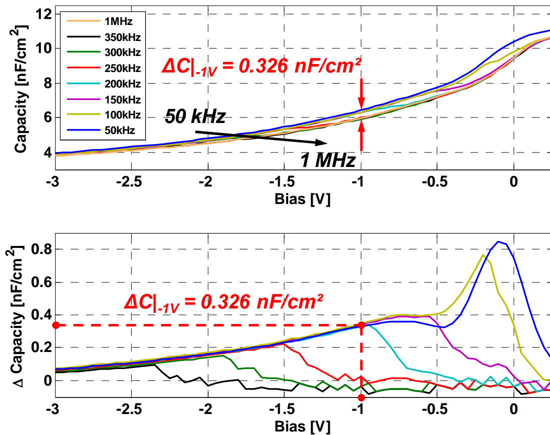

Figure 3: Comparison of low and high frequency capacitance-voltage measurements for recipe (I) taken after a curing time of 100 h at 200°C. The gap calculated starting from the 1 MHz curve can be ascribed to charging processes of defects at the (i) a-Si:H layer and the (i) a-Si:H/c-Si interface.

As discussed in section 3.1 the passivation quality depends on the defect density at the interface. The differences in capacities correlate with the minority carrier lifetime analysis (Fig. 2 left) for the starting values of the samples. Figure 4 shows the RMS values of *ΔC* of several samples during annealing. It can be seen that the difference in capacity decreases first for recipe (I), while *ΔC* for recipes (II) and (III) rises.

Comparing the changes of the differences in capacity with the changes of the minority carrier lifetimes values (added in Fig. 4) it can be seen that they do not match. In comparison with the minority carrier lifetimes values the capacitance difference for recipe (I) after 1 h of annealing should be between the ones for recipes (II) and (III). Also after 10 h of annealing the order of the *ΔC* values should be different. After 100 h of annealing the defect concentrations for all recipes have increased. While the minority carrier lifetime values are in the same range, the *ΔC* measurements are obviously more different to each other comparing to the values of 10 h of annealing where they are nearly the same.

The results of the measurements lead to the conclusion that a direct investigation of the surface passivation quality of amorphous layers using C(V) spectroscopy may not be possible. Defects in the (i) a-Si:H layer bulk generate higher capacitance differences than changes at the (i) a-Si:H/c-Si interface. These changes and their ratio to the total amount of defects are not high enough to be evaluated by the finite instrument resolution of the used impedance analyser (Fig. 4). Therefore, in this case the C(V) spectroscopy becomes more a measure for bulk defects than for the combination of interface and bulk defects of the layer.

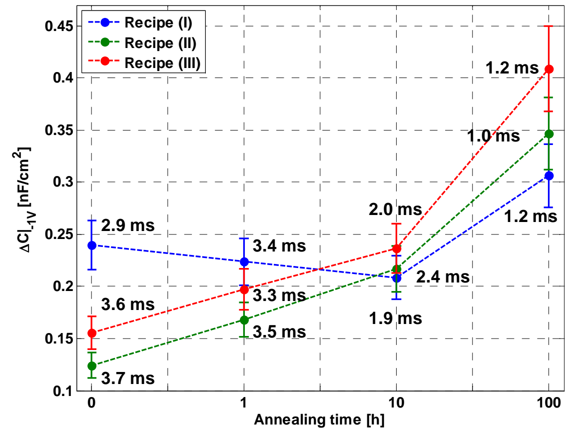

Figure 4: Evolution of the capacitance difference *ΔC* at -1 V between low and high frequency C(V) measurements. The change of *ΔC* reproduces the change in defect density at the (i) a-Si:H layer and the (i) a-Si:H/c-Si interface. Lines are guides to the eye.

The evaporated front side contact consists of a Ti/Pd/Ag stack avoid the effusion of the hydrogen from the (i) a-Si:H layer to the ambient air.

To allow for an assessment of the influence of this hydrogen barrier the fully prepared C(V) "zero hour" samples were additionally annealed and investigated. After ten hours of thermal treatment at 200°C the C(V) spectroscopy yields no changes in the evaluation of *ΔC* regarding to the first investigation. This is probably because less hydrogen effuses during the annealing step compared to the uncovered samples. Enough hydrogen remains in the (i) a-Si:H layer to passivate existing defects. This clarification has shown that it is not possible to continue the C(V) spectroscopy with fully prepared samples. A thermal treatment prior to capping the amorphous layer is necessary.

3.3 FTIR spectroscopy

To investigate the observed structural dependence closer, the bond structure of the (i) a-Si:H layer was analysed by Fourier Transform Infrared spectroscopy (FTIR) with a Vertex 80 FTIR spectrometer from Bruker Optics. The evaluation of the FTIR spectroscopy was carried out according to the method described in [14].

Table II: Content of $Si\text{-}H_2$ before annealing for different recipes of (i) a-Si:H.

Recipe	(I)	(II)	(III)
$Si\text{-}H_2$ rel. Error	14.20% ± 1.04%	15.36% ± 1.00%	14.83% ± 0.96%

The measurements showed that the (i) a-Si:H layers deposited with recipes (II) and (III) features a higher $Si\text{-}H_2$ content than recipe (I), Table II.

According to Langford *et al.* a higher $Si\text{-}H_2$ content could indicate the formation of hydrogen-rich microvoids in the layer [15]. The hydrogen effuses from the microvoids and saturates defects in its vicinity [7]. This

could explain the evolution of the differences in capacity shown in Figure 4 as well as the characteristics of the minority carrier lifetimes shown in Figure 2.

The differences in the structure of the layers caused by the different deposition recipes and the hereby different embedding of hydrogen in the layers [6, 7] could also explain the more stable behaviour of recipe (I) compared to the continuous decrease of the recipes (II) and (III). The passivation of defects at the interface and in the bulk is in the beginning and after a few minutes of annealing better at the layers containing more Si-H_2. After longer thermal treatment the hydrogen effuses from the (i) a-Si:H. This effusion also takes part from the hydrogen-rich microvoids and causes defects in the microvoids itself. However, this leads to a continuous decrease of the performances of microvoid-rich layers.

4. CONCLUSIONS

Two different experiments were conducted to gain information on the interface and bulk defect concentration of (i) a-Si:H layers deposited on c-Si. In these experiments samples with a (i) a-Si:H/c-Si heterojunction deposited with several recipes are heated up to 200 ± 2°C for various durations.

Minority carrier lifetime measurements were carried out to evaluate the passivation of the (n) c-Si by the (i) a-Si:H layer during thermal treatment. With capacitance-voltage spectroscopy the quantitative behaviour of the defects in the (i) a-Si:H bulk as well as at the (i) a-Si:H/c-Si interface were investigated.

The quality of surface passivation by (i) a-Si:H layers with different structures depends on the recipe and the duration of the defect curing step. This is based on the influence of hydrogen, contained in the amorphous layer during deposition, on defects at the (i) a-Si:H/c-Si interface.

Moreover, it has been found that a direct correlation of the surface passivation quality with the defect passivation in the bulk is not possible for thicker layers. The contribution of the interface defects to the difference in capacity (ΔC) is smaller than the resolution of the C(V) measurement. Differences in the structure of the (i) a-Si:H layers, caused by the varied recipes, affect the bulk defects and the resulting ΔC more than changes at the (i) a-Si:H/c-Si interface.

It has been shown that the recipe with the highest content of Si-H_2 bonds, recipe (II), leads to the highest minority carrier lifetime values and to the lowest difference in capacity. This correlation of the Si-H_2 bond structure and the electrical characteristics is probably a product of hydrogen-rich microvoids.

Furthermore, an additional C(V) investigation of full prepared samples has shown that a thermal treatment prior to capping the amorphous layer is necessary. The electrode at the front side of the amorphous layer hinders the hydrogen from effusion in such a manner that changes in the differences of capacity after 10 h of annealing are not measureable.

5. ACKNOWLEDGEMENTS

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