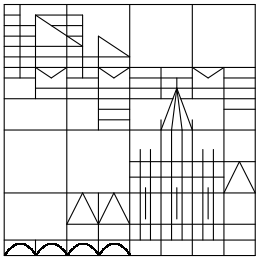

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**Abstract**

We consider the *wiring* or *layer assignment problem* for edge-disjoint layouts. The wiring problem is well understood for the case that the underlying layout graph is a square grid (see [8]). In this paper, we introduce a more general approach to this problem. For an edge-disjoint layout in the plane resp. in an arbitrary planar layout graph, we give equivalent conditions for $k$-layer wirability. Based on these conditions, we obtain linear-time algorithms to wire every layout in a tri-hexagonal grid, respectively every layout in a tri-square-hexagonal grid using at most five layers.

## 1 Introduction

The *wiring problem* consists in converting a two-dimensional edge-disjoint layout into a three-dimensional vertex-disjoint layout. Wiring edge-disjoint layouts is a fundamental and classical problem in VLSI-design. Typically, the general layout problem in VLSI-design consists of two phases, the *placement* and the *routing*. Often, the routing phase is again divided into two steps. First, a two-dimensional layout is constructed satisfying certain conditions induced by the underlying layout model. This layout describes the course of the wires connecting the corresponding terminals. In the second step, the *wiring step* or *layer assignment step*, the edges of the wires are assigned to different layers to avoid physical contacts between different wires. The layout can be viewed as a projection of this final three-dimensional wiring into the plane. In connection with *graph drawing*, the wiring problem is of interest as well. There, an edge-disjoint embedding of a graph is given. The problem consists in a visualization of the graph by a three-dimensional vertex-disjoint

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embedding whose projection into the plane is again the edge-disjoint embedding of the graph.

Consider an edge-disjoint *layout* in the plane resp. in a planar graph (called *layout graph*). Such a layout may be an edge-disjoint realization of *nets*, i. e., of prescribed sets of vertices *(terminals)*, or an edge-disjoint embedding of a graph. More precisely, an edge-disjoint realization of nets consists in pairwise edge-disjoint Steiner trees *(wires)* connecting the terminals of the nets. On the other hand, an edge-disjoint embedding of a graph is a mapping of the vertices of that graph into the plane resp. onto vertices of a planar layout graph, and of the edges of the graph to pairwise edge-disjoint paths. The construction of edge-disjoint layouts is a fundamental problem. For an overview we refer to [3, 9, 12].

Then the wiring problem can be described as follows. There is a number of graphs isomorphic to the layout resp. the layout graph, called *layers*. Each path resp. Steiner tree of the layout is realized by a sequence of subpaths in different layers such that two different wires are vertex-disjoint. A vertical connection between layers, a so-called *via*, is used at each layer change. The main optimization goal is to minimize the number of layers.

Several results have been obtained for the wiring problem for edge-disjoint layouts in regular grids, especially square grids [1, 2, 4, 5, 6, 10, 13, 16, 15, 17]. Most of these results are based on a combinatorial framework introduced in [8] which applies to edge-disjoint layouts in square grids. Moreover, only layouts where terminals are placed on the boundary of the layout graph are considered. A technique using two-colorable maps is developed, and necessary and sufficient conditions for the wirability in a fixed number of layers are given. For two layers these conditions are easy to test. On the other hand, it is $\mathcal{NP}$-complete to decide if a layout is three-layer wirable [7]. Every layout is wirable in four layers, and such a wiring can be constructed in time linear in the size of the layout [1], [15]. In [15], the concept of two-colorable maps is applied to octo-square grids, but no guarantee for the number of layers required for the wiring is given. If the layout graph is a tri-hexagonal grid, every edge-disjoint layout is wirable in five layers [14].

Nothing is known so far about the wiring problem for layouts in the plane resp. in general planar layout graphs with arbitrary terminal positions. In this paper, we develop a general approach to this problem. It leads to necessary and sufficient conditions for $k$-layer wirability of edge-disjoint layouts where at most two different wires meet in a vertex. These conditions generalize the framework given in [8]. Again, two-layer wirability is easy to test. And of course, since deciding three-layer wirability for grid-based layouts is $\mathcal{NP}$-complete, the problem is $\mathcal{NP}$-complete for layouts in planar layout graphs as well. For layouts in special planar layout graphs guarantees are given for the number of layers required for the wiring. We prove that every layout in a tri-hexagonal grid is wirable in at most five layers. Moreover, every layout in a tri-square-hexagonal grid is wirable in at most five layers as well. In both cases, such a wiring can be constructed in time linear in the size of the layout. Observe that our approach for layouts in tri-hexagonal grids is different from the approach given in [14].

The wiring theory presented here is restricted to layouts where at most four wire edges are incident to the same vertex. But it is extendable to the case that more than four wire

edges belonging to at most two different wires are incident to the same vertex. The case that more than two different wires meet at a vertex seems to be much more involved.

The paper is organized as follows. In Section 2, we introduce the necessary definitions and notations. The general approach to wiring edge-disjoint layouts is developed in Section 3. Finally, in Section 4 we present linear-time algorithms for wiring layouts in tri-hexagonal and tri-square-hexagonal grids using at most five layers.

# 2 Preliminaries

We consider an edge-disjoint layout in the plane or in a planar layout graph. Such a *layout in the plane* consists of vertices, called *terminals*, in the plane and pairwise edge-disjoint Steiner trees connecting specified sets of terminals, called *wires*. A special case of an edge-disjoint layout is an edge-disjoint embedding of a graph, i. e., a mapping of the vertices of that graph into the plane and a realization of its edges by pairwise edge-disjoint paths. Similarly, for an edge-disjoint *layout in a planar graph* consider an undirected graph $G$, the *layout graph*, with a fixed embedding in the plane. Then the layout consists of *terminals* placed on vertices of $G$ and pairwise edge-disjoint Steiner trees connecting specified sets of terminals, respectively pairwise edge-disjoint paths realizing edges of the embedded graph. A layout in the plane, respectively the vertices and edges of the layout graph $G$ occupied by a layout, induce a planar embedded graph. In the following we identify a layout $L$ with this induced graph.

A *conducting layer*, or simply *layer* is a graph isomorphic to the layout $L$. Conducting layers $L_0, \ldots, L_{k-1}$ are assumed to be stacked on top of each other, with $L_0$ on the bottom and $L_{k-1}$ on the top. A contact between two layers, called a *via*, can be placed only at a vertex of a layer.

A correct *layer assignment* or *wiring* $W(L)$ of a given layout $L$ is a mapping of each edge of $L$ to a layer such that:

1. No two different wires share a vertex on the same layer.

2. If adjacent edges of a wire are assigned to different layers, a via is established between these layers at their common vertex.

3. If a via connects $L_h$ and $L_j$ $(h < j)$, then layers $L_i, h < i < j$, are not used at that vertex by any other wire.

Note that a correct wiring can be interpreted as a three-dimensional configuration of *vertex-disjoint* wires. In the following, we restrict to layouts where at most two different Steiner trees meet at the same vertex. The case that more than two different wires meet at a vertex seems to be much more involved. The wiring theory presented here is formulated only for layouts where at most four wire edges are incident to the same vertex. But it is extendable to the case that more than four wire edges belonging to at most two different wires are incident to the same vertex.

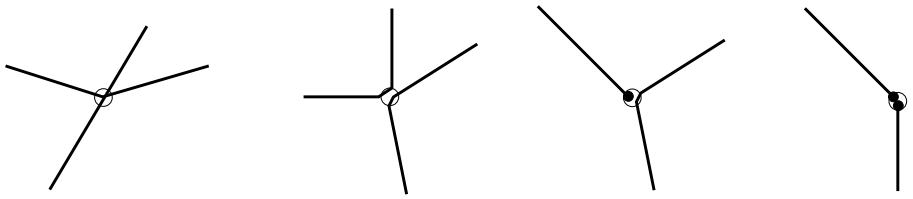



Figure 1: The different possibilities of non-trivial vertices. Each of the two wires may end at a terminal in that vertex. Possibility c) occurs when one wire ends at a terminal and d) occurs when both wires end at a terminal in that vertex.

To determine a correct wiring of a layout $L$, only those vertices where two different wires meet are of relevance. In the following we call these vertices *non-trivial vertices* of the layout. In Figure 1, all possibilities of non-trivial vertices where at most four wire edges meet are shown.

**Definition 2.1** *The subgraph of $L$ induced by all non-trivial vertices and all edges incident to at least one non-trivial vertex of $L$ is called the* core *of $L$, denoted $core(L)$.*

The following lemma shows that we can restrict to the core of a layout $L$. In [8], it is proved for layouts in grids, where different wires may cross or both bend at the same vertex, but do not meet at terminals. But the proof of the lemma applies to the more general layouts we consider here as well.

**Lemma 2.2** *[8] A layout $L$ is wirable in $k$ layers if and only if each connected component of $core(L)$ is.*

**Proof** In order to prove the non-trivial part of the lemma, consider a $k$-layer wiring $W$ of the core $core(L)$. All edges of $L - core(L)$ are assigned to an arbitrary layer, say $L_0$. If necessary, a via is established on a trivial vertex connecting the wires incident to that vertex. □

The concept of $k$-layer wirability developed in the following sections uses the characterization of two-layer wirable layouts. The two-layer wirability of both, grid based and non-grid based layouts, is well understood in context with *via minimization* for two-layer wirable layouts. So, the concept of conflict graphs resp. Lemma 2.3 is well-known (see for example [11]), however expressed differently there.

Obviously, in a two-layer wirable layout two wire edges that are incident to the same vertex but belong to different wires must be assigned to different layers. The *conflict graph* corresponding to $core(L)$, denoted $core(L)^c = (V^c, E^c)$, is defined as follows. For each edge in $core(L)$ there is a vertex in $V^c$, and two vertices are joined by an edge in $E^c$ if and

only if the two corresponding edges are incident to the same vertex and belong to different wires. Then a two-layer wiring of $core(L)$ is equivalent to a correct two-coloring of the vertices of $V^c$, i. e., a two-coloring where vertices of $V^c$ incident to the same edge have different colors. It is well-known that a graph is two-colorable if and only if all cycles have even length.

**Lemma 2.3** *A layout $L$ is two-layer wirable if and only if all cycles in the conflict graph $core(L)^c$ corresponding to $core(L)$ have even length.*

# 3 A characterization of $k$-layer wirability

In this section, we develop a complete characterization of $k$-layer wirability for planar layouts. First, we observe that we can restrict to the 2-edge-connected components of a layout core.

**Lemma 3.1** *A layout $L$ is wirable in $k$ layers if and only if each 2-edge-connected component of $core(L)$ is wirable in $k$ layers.*

**Proof** In order to prove the non-trivial part of the lemma, consider a decomposition of $core(L)$ into its 2-edge-connected components. These 2-edge-connected components can be ordered topologically. Let $W$ be a $k$-layer wiring of the 2-edge-connected components, and $P$ be a wire going through different components. Then there is an edge $\{u, v\}$ on $P$ such that $u$ and $v$ belong to different components, say $C(u)$ and $C(v)$. Assume w.l.o.g. that $C(u)$ is before $C(v)$ in the topological ordering.

Now, a correct $k$-layer wiring $W^*$ of the subgraph of $core(L)$ induced by $C(u)$, $\{u, v\}$ and $C(v)$ is constructed as follows. In case the wiring of $C(u)$ and $C(v)$ are compatible, i. e., $P$ is wired both times above (resp. below) the wire it meets in $u$ and in $v$, the wiring of $C(v)$ and $C(u)$ remains fixed, $\{u, v\}$ is wired in the same layer as $P$ in $u$, and an appropriate via is placed on $v$. Otherwise, only the wiring of $C(u)$ remains fixed and the wiring of $C(v)$ is flipped. That is, if an edge of $C(v)$ belongs to layer $L_i, 0 \leq i \leq k-1$, in $W$, then this edge is assigned to layer $L_{k-i}$ in $W^*$. Then again, $\{u, v\}$ is wired in the same layer as $P$ in $u$, and an appropriate via is placed on $v$. Finally, a sequence of flippings according to an arbitrary linear extension of the topological ordering of the 2-edge-connected components of $core(L)$ induces a correct wiring of $L$ in $k$ layers. □

In the following, we assume that $core(L)$ is 2-edge-connected. The *dual graph* of a planar graph with respect to a fixed combinatorial embedding is defined as follows. For each face of the graph there is a dual vertex, and there is an edge connecting two dual vertices if and only if their faces are incident with a common primal edge. The subgraph of the dual graph of $L$ corresponding to $core(L)$ is denoted by $core(L)^d$. That is, $core(L)^d$ is the graph induced by all edges dual to edges of $core(L)$. Since $core(L)$ is 2-edge-connected, $core(L)^d$ contains no loops. The edges of $core(L)^d$ that are dual to edges of $core(L)$ incident to a

trivial vertex are called the *boundary edges* of $core(L)^d$, or just *the boundary* of $core(L)^d$. Vertices of $core(L)^d$ incident to boundary edges are called *boundary vertices*, all other vertices of $core(L)^d$ are called *inner vertices*. See Figure 3. Obviously, a vertex is an inner vertex if and only if it is dual to a face of $core(L)$ that contains only non-trivial vertices.

Figure 2: Diagonal edges corresponding to a pair of neighbored edges of $core(L)$ that belong to the same wire.

We first give a characterization of two-layer wirable layouts different from that given in Section 2. This characterization is of fundamental importance for what follows. It is based on the dual of the layout core. Let us call two edges of a planar graph that are incident to the same vertex and have a common face *neighbored*. For a layout $L$, define *diagonal edges* connecting certain vertices of $core(L)$ with vertices of $core(L)^d$. Precisely, for every pair of neighbored edges of $core(L)$ that belong to the same wire and whose common vertex is non-trivial, a diagonal edge is introduced connecting that common non-trivial vertex and the vertex of $core(L)^d$ corresponding to the common face. See Figure 2 and Figure 3. For a vertex $v \in core(L)^d$ denote $diag(v)$ the number of diagonals incident to $v$. Then the *extended degree* of $v$, $exdeg(v)$, is the sum of the degree of $v$ (denoted $deg(v)$), and the number of diagonal edges incident to $v$, i. e., $exdeg(v) := deg(v) + diag(v)$. Now, $deg(v)$ is equal to the number of edges on the face $F^v$ dual to $v$, which is again equal to the number of vertices on $F^v$. Thus, $exdeg(v) = |F^v| + diag(v)$. A vertex $v \in core(L)^d$ is called *even* if $exdeg(v)$ is an even number, otherwise $v$ is called *odd*.

**Lemma 3.2** *A layout $L$ is two-layer wirable if and only if*

1. *for each inner vertex of $core(L)^d$ the extended degree is even,*
2. *for each connected component of the boundary of $core(L)^d$ the sum of the extended degrees of the boundary vertices minus the number of boundary edges is even.*

**Proof** In a two-layer wiring, two neighbored edges incident to a common non-trivial vertex are assigned to different layers if and only if they belong to different wires. Thus, $core(L)$ is two-layer wirable if and only if for every face of $core(L)$ the number of vertices on that face incident to neighbored edges belonging to different wires is even.

First, consider an inner vertex $v$ of $core(L)^d$ dual to face $F^v$ of $core(L)$. Let $m(v)$ denote the number of vertices on $F^v$ incident to neighbored edges on $F^v$ belonging to different wires. Since an inner vertex $v \in core(L)^d$ is dual to a face $F^v$ containing only non-trivial

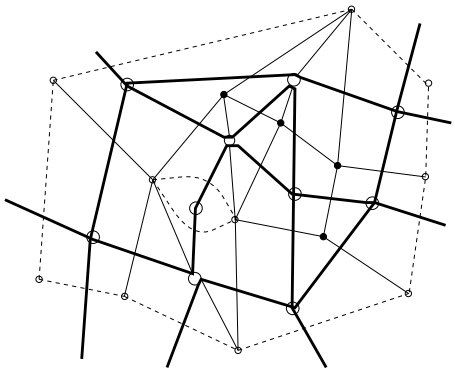


Figure 3: Part of a layout core (bold), its dual and its diagonals (thin); the dashed edges are the boundary edges of the dual; inner vertices of the dual are black.

vertices, $F^v$ is two-layer wirable if and only if $m(v)$ is even. Thus, $F^v$ is two-layer wirable if and only if $exdeg(v) = |F^v| + diag(v) = m(v) + 2diag(v)$ is even.

Now, consider a connected component $B$ of the boundary of $core(L)^d$. Denote $exdeg(B)$ the sum of the extended degrees of the boundary vertices of $B$, and $|B|$ the number of boundary edges on $B$. For a boundary vertex $v$, denote $deg_{core(L)}(v)$ the number of incident edges dual to edges of $core(L)$, and $deg_B(v)$ the number of incident edges on the boundary $B$. Then we have

$$exdeg(v) = deg(v) + diag(v) = deg_{core(L)}(v) + deg_B(v) + diag(v).$$

The edges of $core(L)$ dual to edges incident to vertices on $B$ form a cycle in $core(L)$. Denote $m(B)$ the number of vertices on that cycle incident to neighbored edges belonging to different wires. Then this cycle is two-layer wirable if and only if $m(B)$ is even. We have

$$\begin{aligned} exdeg(B) - |B| &= \sum_{v \in B} exdeg(v) - |B| \\ &= \sum_{v \in B} deg(v) + \sum_{v \in B} diag(v) - |B| \\ &= \sum_{v \in B} deg_{core(L)}(v) + \sum_{v \in B} deg_B(v) + \sum_{v \in B} diag(v) - |B|. \end{aligned}$$

Now,

$$\sum_{v \in B} deg_{core(L)}(v) = m(B) + \sum_{v \in B} diag(v) + |B|,$$

and thus

$$\begin{aligned} exdeg(B) - |B| &= m(B) + 2\sum_{v \in B} diag(v) + \sum_{v \in B} deg_B(v) + |B| - |B| \\ &= m(B) + 2\sum_{v \in B} diag(v) + \sum_{v \in B} deg_B(v). \end{aligned}$$

Since every edge on $B$ is counted twice, $\sum_{v \in B} deg_B(v)$ must be even. Thus, $m(B)$ is even if and only if $exdeg(B) - |B|$ is even. □

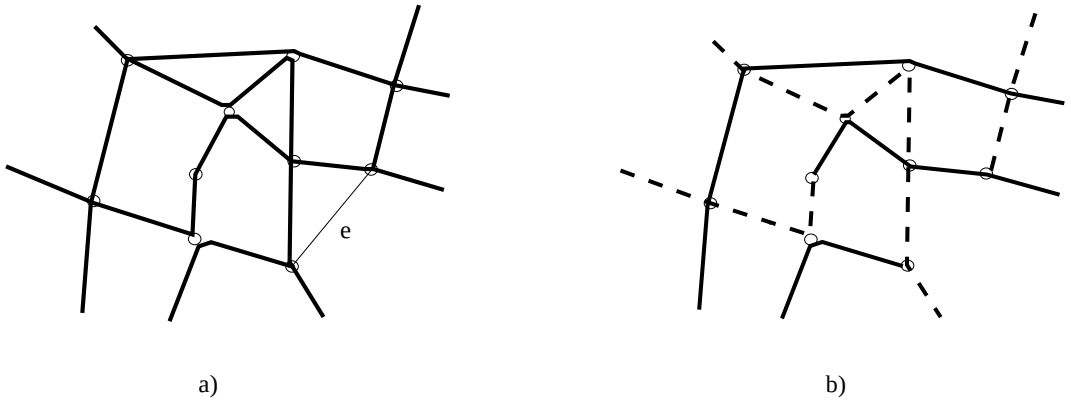
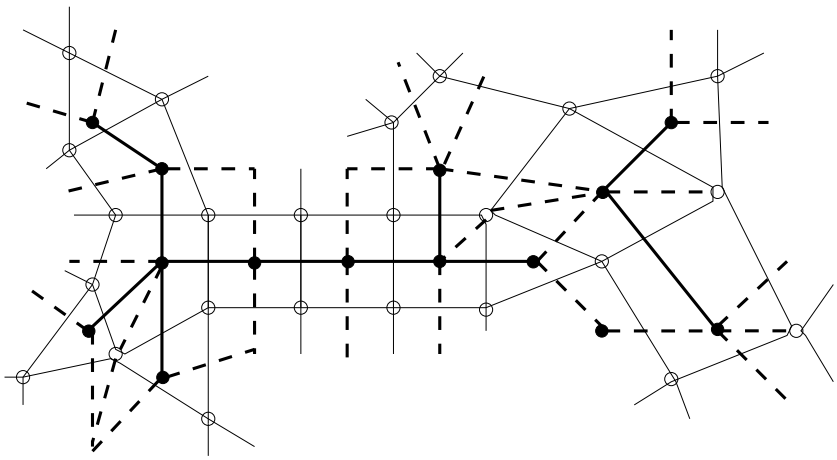



Figure 4: a) The layout $L$ from Figure 3. Edge $e$ forms a legal removal set (thin). b) A two-layer wiring of $L - \{e\}$.

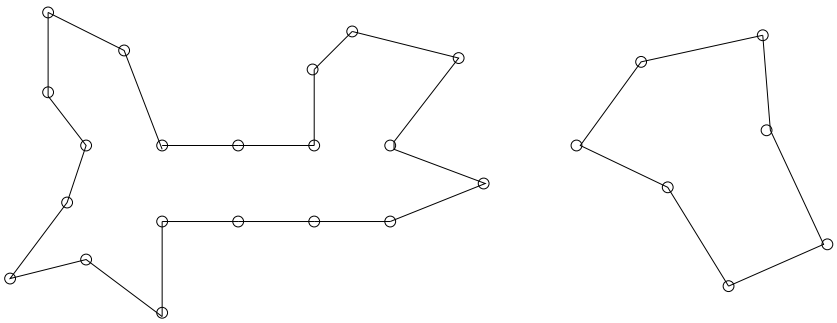
The general wiring theory developed now relies on the construction of an appropriate set of wire edges whose removal leaves a two-layer wirable layout. The declaration what "appropriate" means is our goal now. More precisely, for a $k$-layer wirable layout we give an equivalent characterization of a set of wire edges whose removal leaves a two-layer wirable layout. This characterization of a set of wire edges consists in giving forbidden patterns for the dual edges.

**Definition 3.3** *Consider a subset $R$ of wire edges of $core(L)$. $R$ is called a* removal set *of $core(L)$ if its removal leaves a two-layer wirable layout. The elements of $R$ are also called* removal edges. *Denote $R^d$ the set of edges dual to edges of $R$. A removal set $R$ is called* legal *if $R^d$ contains no cycle and no path connecting two vertices of the same connected component of the boundary of $core(L)^d$.*

Consider a legal removal set $R$ of $core(L)$. If $core(L)$ is 2-edge-connected, the graph induced by $core(L) - R$ is connected. Thus it has a two-layer wiring that is unique up to the choice of the layers, say in layer *bottom* and layer *top*. Such a two-layer wiring induces a *type classification* of vertices $u$ and $v$ *with respect to* $\{u, v\}$ for every edge $\{u, v\} \in R$.



a)



b)

Figure 5: a) Part of a layout (thin), the dual of a legal removal set $R^d$ (bold), the dual edges not belonging to $R^d$ and the diagonal edges (dashed). Observe that $R^d$ forms trees. b) The cycles of layout edges dual to these trees.

$$type_{\{u,v\}}(v) := \begin{cases} 1 & \text{if } \{u,v\} \text{ is incident in } v \text{ to a wire edge} \\ & \text{of the same wire in the top layer, or} \\ & \text{of a different wire in the bottom layer;} \\ 2 & \text{otherwise.} \end{cases}$$

Obviously, this classification is well defined. Observe, that for a vertex $v$ incident to edges $\{u,v\},\{w,v\} \in R$ that belong to different wires, $type_{\{u,v\}}(v) \neq type_{\{w,v\}}(v)$. Then Lemma 3.2 implies the following corollary.

**Corollary 3.4** *For a legal removal set $R$, the edges of $R^d$ form paths connecting odd vertices of $core(L)^d$, respectively an odd vertex to a boundary vertex of $core(L)^d$.*

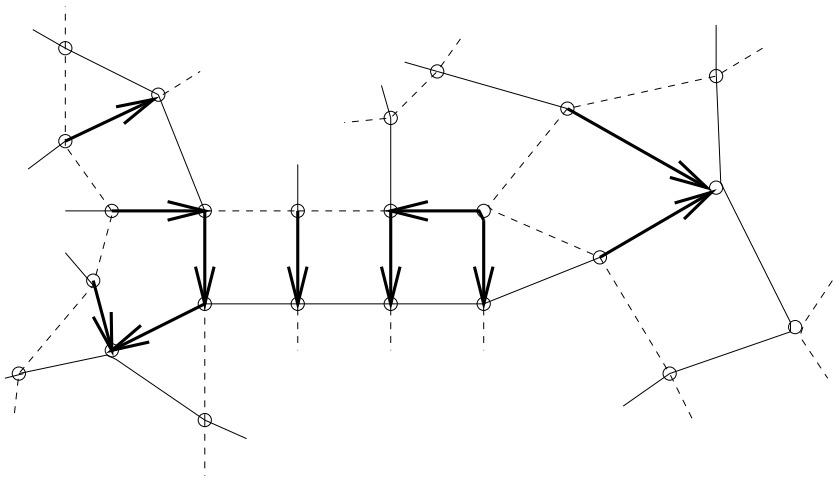


Figure 6: The layer graph $\vec{R}$ (bold) induced by a two-layer wiring (thin; dashed resp. not dashed) that corresponds to $R^d$ in Figure 5.

Since $R$ is legal, these paths form trees whose leaves are odd, respectively lie on the boundary. Note that two different paths containing a vertex of the same boundary component are considered to belong to the same tree.

**Lemma 3.5** *Let $R$ be a legal removal set of $core(L)$. For a type classification induced by a two-layer wiring of $core(L) - R$, $type_{\{u,v\}}(v) \neq type_{\{u,v\}}(u)$ for every edge $\{u, v\} \in R$.*

**Proof** A tree $T$ of edges of $R^d$ induces a cycle of wire edges not in $R$, i. e., the cycle of edges of $core(L)$ around $T$. More precisely, every inner vertex of $core(L)$ belonging to $T$ corresponds to its dual cycle in $core(L)$, and every boundary vertex of $core(L)$ belonging to $T$ corresponds to the cycle in $core(L)$ around the corresponding boundary component. Then the union of these cycles minus the edges of $R$ form the cycle induced by $T$. See Figure 5 a) and b).

In a two-layer wiring of $core(L) - R$, such a cycle must contain an even number of layer changes. Now, consider an edge $\{u, v\} \in R$ dual to an edge of $T$. Assume $type_{\{u,v\}}(v) = type_{\{u,v\}}(u)$. Then for all edges $\{x, y\} \in R$ dual to an edge of $T$ we have $type_{\{x,y\}}(x) = type_{\{x,y\}}(y)$. But for an edge of $R$ dual to an edge incident to a leaf of $T$, the type of the two end vertices must be different with respect to that edge. This is a contradiction. See Figure 6. □

Lemma 3.5 guarantees that we can define an orientation on the edges of $R$.

**Definition 3.6** *An edge $\{u, v\} \in R$ is oriented from $u \to v$ if and only if $type_{\{u,v\}}(u) = 1$ and $type_{\{u,v\}}(v) = 2$. Let $\vec{R}$ denote the directed graph, called* layer graph, *induced by $R$ and this orientation.*

Obviously, two adjacent arcs of $\vec{R}$ that belong to the same wire are oriented towards each other. So, two subsequent edges on a directed path in $\vec{R}$ must belong to different wires. The *length* of a directed path is defined as the number of edges on that path. Now we are ready to prove the main theorem of this section.

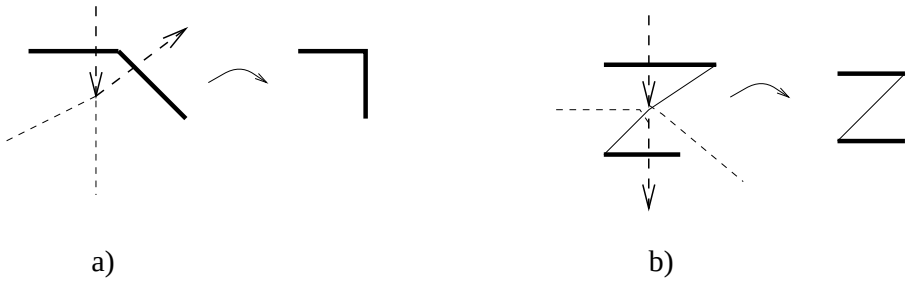



Figure 7: Removal sets that do not induce 3-layer wirability and the corresponding forbidden patterns. A pattern corresponding to neigboring edges is shown in a). A pattern corresponding to two subsequent parallel edges, i. e. two edges of the same face that are not neigboring, both incident to a diagonal ending at the same vertex are shown in b).

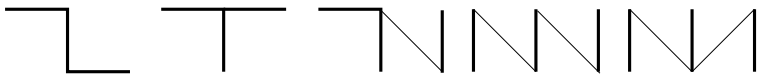


Figure 8: Examples of forbidden patterns for 4-layer wirability.

**Theorem 3.7** *A layout $L$ is wirable in $k$ layers if and only if there exists a legal removal set $R$ such that the length of any directed path in $\vec{R}$ is at most $k-2$.*

**Proof** "$\Rightarrow$" Consider a wiring of $core(L)$ in layer $L_i, 0 \leq i \leq k-1$. Let $R$ be the set of all wire edges wired in layer $L_i, 0 \leq i \leq k-1$, and $\vec{R}$ the corresponding directed layer graph. For a directed path in $\vec{R}$, two subsequent arcs $(u,v)$ and $(v,w)$ belong to different wires and thus must be wired in different layers. Because of the orientation, the layer of $(u,v)$ must be below the layer of $(v,w)$. Consequently, the length of any directed path in $\vec{R}$ is at most $k-2$.

"$\Leftarrow$" Assume there exists a legal removal set $R$ such that the length of every directed path in $\vec{R}$ is at most $k-2$. For an edge $(u,v) \in \vec{R}$ denote $l_{max}(u,v)$ the maximum length of a directed path in $\vec{R}$ terminating with $(u,v)$. A wiring of $core(L)$ in $k$ layers $L_i, 0 \leq i \leq k-1$, is constructed as follows.

$$layer(u,v) = \begin{cases} L_0 \text{ resp. } L_{k-1}, & \text{if } (u,v) \notin \vec{R}; \\ L_i, 1 \leq i \leq k-2, & \text{if } (u,v) \in \vec{R} \text{ and } l_{max}(u,v) = i-1. \end{cases}$$

The assignment of $(u, v)$ to $L_0$ resp. $L_{k-1}$ is according to a fixed two-layer wiring of $core(L) - R$. □

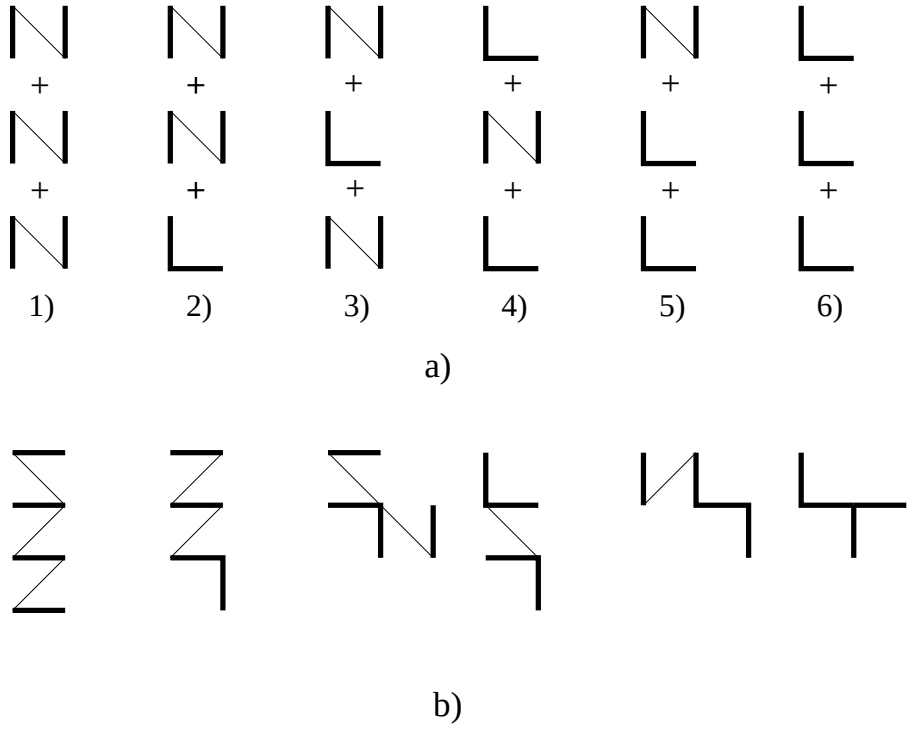



Figure 9: a) Combinations of forbidden patterns for 3-layer wirability that lead to forbidden patterns for 5-layer wirability. b) Examples of forbidden patterns for 5-layer wirability.

**Remark** The proof of Theorem 3.7 induces an algorithm to construct a $k$-layer wiring from a legal removal set $R$ where the length of any directed path in $\vec{R}$ is at most $k-2$. This algorithm can be easily implemented to run in time linear in the size of the layout.

A characterization of $k$-layer wirability for $k > 2$ in terms of forbidden patterns in the dual $R^d$ of a legal removal set $R$ is now easily derived from Theorem 3.7. Let us call two edges belonging to the same face that are not neighbored *parallel edges*.

**Lemma 3.8** *A layout $L$ is wirable in three layers if and only if there exists a legal removal set $R$ such that $R^d$ contains none of the patterns shown in Figure 7.*

**Proof** $core(L)$ is wirable in three layers if and only if there exists a legal removal set $R$ such that $\vec{R}$ contains no directed path of length two. For a directed path in $\vec{R}$ two subsequent edges must belong to different wires. These two edges meet at a non-trivial vertex, say $v$. In case the two corresponding dual edges in $R^d$ are neigboring in $v$, they

form a pattern of type a) shown in Figure 7. Otherwise they form a pattern of type b) shown in Figure 7. More precisely, the two corresponding dual edges in $R^d$ are parallel, i. e. belong to the same face but are not neigbored in $v$, and are each incident to a diagonal ending at $v$. □

Lemma 3.8 can be easily extended to giving forbidden patterns for wirability in $k \geq 4$ layers. From the patterns shown in Figure 7 we just have to generate patterns dual to directed paths of length $k-1$ in the layer graph. Forbidden patterns for wirability in four layers are all possible combinations of two forbidden patterns for wirability in three layers,where two patterns are combined by identifying two edges. See Figure 8 for some examples. Accordingly, forbidden patterns for wirability in five layers are all possible combinations of three forbidden patterns for wirability in three layers. See Figure 9.

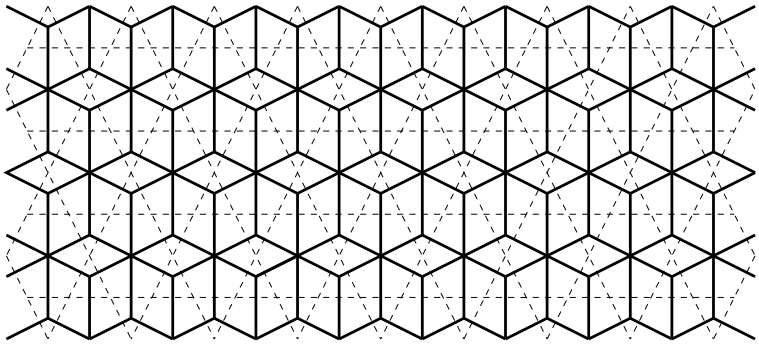
# 4 Algorithms

In this section we prove that every layout in a tri-hexagonal grid and every layout in a tri-square-hexagonal grid is wirable in five layers. We present algorithms that construct a removal set for such a layout satisfying Theorem 3.7 for $k = 5$. That is, the dual $R^d$ corresponding to the constructed removal set $R$ contains none of the patterns illustrated in Figure 9.

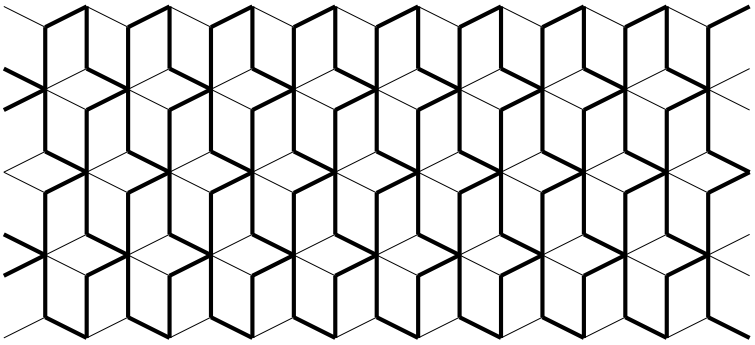
## 4.1 Layouts in Tri-Hexagonal Grid Graphs

A tri-hexagonal grid graph is a grid consisting of grid lines of three different directions, the horizontal direction and two diagonal directions. In every grid point, lines of two different directions meet, either one horizontal and one diagonal line, or two diagonal lines. Consequently, every vertex has degree four. The faces of the dual of a tri-hexagonal grid graph are all squares. See Figure 10 a) for a tri-hexagonal grid and its dual.

The algorithm to construct a legal removal set $R$ for a layout $L$ in a tri-hexagonal grid works as follows. Firstly, all vertices of the layout are considered to be non-trivial. Then obviously, 5-layer wirability of this layout induces 5-layer wirability of the original layout. The dual of the layout is scanned "row-wise" from bottom to top, and from left to right. For every vertex of the dual of the layout, its extended degree and its vertex class is considered. That is, the vertex set of the grid dual to a tri-hexagonal grid is partitioned into three different classes: vertices of degree six (*class 1*), vertices of degree three incident to an up-going vertical edge and two diagonal edges (*class 2*), and vertices of degree three incident to an down-going vertical edge and two diagonal edges (*class 3*). See Figure 11. Now alternatingly, in every second row only vertices of class 1 and class 2 are visited, repectively only vertices of class 3. Depending on the extended degree and the class of the visited vertex, an incident edge is added to $R^d$ in such a way, that $exdeg(v)$ is even for all vertices $v \in L^d - R^d$, and $R^d$ contains no forbidden pattern for 5-layer wirability.

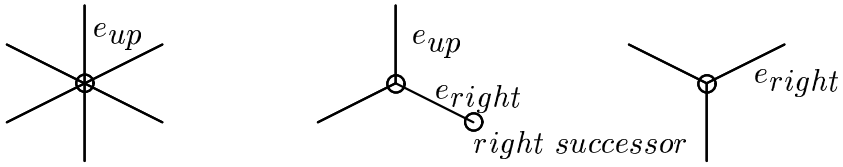


a)



b)

Figure 10: a) A tri-hexagonal grid graph (dashed) and its dual graph (bold). b) Dual edges that might be added to $R^d$ by the algorithm (bold).




1) 2) 3)

Figure 11: The three different classes of vertices in the grid dual to a tri-hexagonal grid.

**Algorithm 4.1 Tri-Hexa**

**Input:** *The dual $L^d$ of a layout $L$ in a tri-hexagonal grid together with its rows, i. e., alternating rows consisting of vertices of class 1 and class 2, respectively consisting of class 3.*

**Output:** *A subset $R^d$ of $L^d$ such that $exdeg(v)$ is even for all vertices $v \in L^d - R^d$ and $R^d$ contains no forbidden pattern for 5-layer wirability.*

**begin**

$R^d := \emptyset$

**for** *all rows from bottom to top* **do**

**for** *all vertices $v$ of one row from left to right* **do**

**if** *$exdeg(v)$ is odd in $L^d$ and $v$*

*belongs to class 2,* **then** $R^d := \begin{cases} R^d + e_{right}, & \text{if right successor is odd;} \\ R^d + e_{up} & \text{otherwise.} \end{cases}$

*belongs to class 1,* **then** $R^d := R^d + e_{up}$

*belongs to class 3,* **then** $R^d := R^d + e_{right}$

$L^d := L^d - R^d$

**end**

**Theorem 4.2** *For a layout $L$ in a tri-hexagonal grid, Algorithm 4.1 constructs a subset $R^d$ of $L^d$ that contains no forbidden pattern for 5-layer wirability. The running time is linear in the size of the layout.*

**Proof** Algorithm 4.1 considers only those edges of $L^d$ shown in Figure 10 b). In the dual of a tri-hexagonal grid there exist parallel edges of three different directions, parallel edges of vertical direction and parallel edges of two different diagonal directions. It is easy to see that Algorithm 4.1 maintains the following invariants.

**I1** In $R^d$ there are at most two subsequent parallel edges of vertical direction.

**I2** In $R^d$ there are no two subsequent parallel edges of diagonal direction.

**I3** The maximum number of neighbored edges $\delta^{neighbored}(v)$ in $R^d$ incident to a vertex $v$ is

$$\delta^{neighbored}(v) := \begin{cases} 3, & \text{if } v \text{ is in class 1;} \\ 1, & \text{if } v \text{ is in class 2;} \\ 2 & \text{if } v \text{ is in class 3.} \end{cases}$$

**I4** If for a vertex of class 1, edge $e_{up} \in R^d$, then its neighbored edges are not in $R^d$.

A necessary condition for a pattern of type 1) shown in Figure 9 a) are four subsequent parallel edges in $R^d$. Similarly, a necessary condition for a pattern of type 2) are three subsequent parallel edges in $R^d$. This is impossible because of invariants I1 and I2.

A pattern of type 3) is impossible as well, since it must contain two subsequent parallel edges in diagonal direction. This is again a contradiction to I2.

A necessary condition for a pattern of type 4) resp. 5) are two subsequent parallel edges, which must be in vertical direction because of I2. But there is no edge in $R^d$ neighbored to one of these vertical edges because of I3 resp. I4.

There are three possible configurations for a pattern of type 6). The configuration that all edges are incident to the same vertex is impossible because of I3. Three incident neighbored edges are only possible at a vertex of class 1. Then the two outer edges are both also incident to a vertex of class 2. But, because of I3 the fourth edge required to build a configuration of type 6) cannot exist. Thirdly, in $R^d$ there occurs no sequence of four edges, where two subsequent edges are neighbored. Since, the longest sequence of edges, where two subsequent edges are neighbored, consistes of three edges beginning at a vertex of class 2 and ending at a vertex of class 1.

Obviously, Algorithm 4.1 can be implemented to run in time linear in the size of the layout.

□

From a legal removal set determined by Algorithm 4.1, a 5-layer wiring of a layout in a tri-hexagonal grid can be constructed in linear time as well, according to Theorem 3.7.

## 4.2 Layouts in Tri-Square-Hexagonal Grid Graphs

A tri-square-hexagonal grid graph is the dual graph of the union of two grids, a hexagonal grid and the dual of a hexagonal grid. The faces are triangles, squares and hexagons. It contains only vertices of degree four and the faces of its dual are squares. See Figure 12 for a tri-square-hexagonal grid and its dual.

The algorithm to construct a legal removal set $R$ for a layout $L$ in a tri-square-hexagonal grid again scans the dual of the layout "row-wise" from bottom to top and from left to right. The vertices of the grid dual to a tri-square-hexagonal grid are partitioned into six different classes: vertices of degree six *(class 1)*, three different classes of vertices of degree four *(class 2, 3 and 4)*, and two different classes of vertices of degree three *(class 5 and 6)*. See Figure 13.

Alternatingly, in every second row only vertices of class 1 and class 2 are visited, or only vertices of class $3, 4, 5$ and 6. Depending on the extended degree and the class of the visited vertex, an edge is added to $R^d$ in such a way that $exdeg(v)$ is even for all vertices $v \in L^d - R^d$, and $R^d$ contains no forbidden pattern for 5-layer wirability.

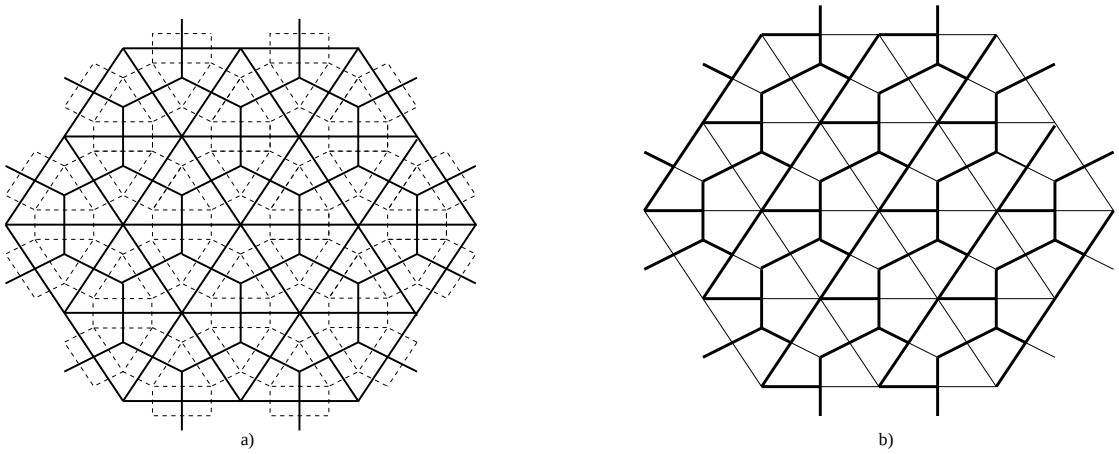



Figure 12: a) A tri-square-hexagonal grid graph (dashed) and its dual graph (bold). b) Dual edges that might be added to $R^d$ by the algorithm (bold).

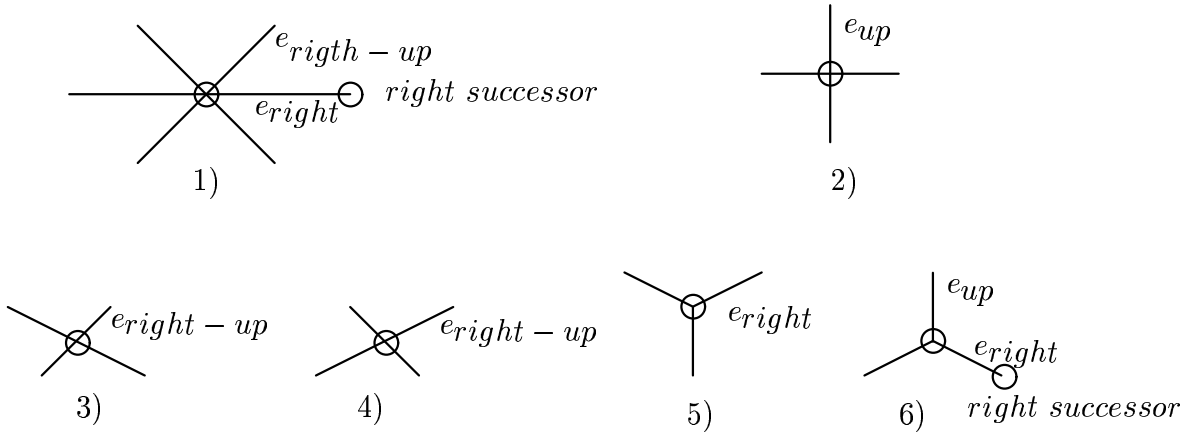



Figure 13: The six different classes of vertices in the grid dual to a tri-square-hexagonal grid.

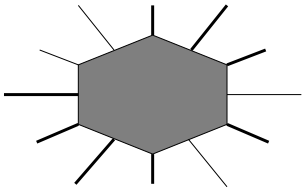


Figure 14: Edges of $L^d$ arranged around a hexagon.

**Algorithm 4.3 Tri-Square-Hexa**

**Input:** *The dual $L^d$ of a layout $L$ in a tri-square-hexagonal grid and its rows, i. e. alternating rows of vertices of class 1 and class 2, respectively of class 3, 4, 5 and 6.*

**Output:** *A subset $R^d$ of $L^d$ such that $exdeg(v)$ is even for all vertices $v \in L^d - R^d$, and $R^d$ contains no forbidden pattern for 5-layer wirability.*

**begin**

$R^d := \emptyset$

**for** *all rows from bottom to top* **do**

**for** *all vertices $v$ of one row from left to right* **do**

**if** *$exdeg(v)$ is odd in $L^d$ and $v$*

*belongs to class 1,* **then** $R^d := \begin{cases} R^d + e_{right}, & \text{if right successor is odd;} \\ R^d + e_{right-up} & \text{otherwise.} \end{cases}$

*belongs to class 2,* **then** $R^d := R^d + e_{up}$

*belongs to class 3,* **then** $R^d := R^d + e_{right-up}$

*belongs to class 4,* **then** $R^d := R^d + e_{right-up}$

*belongs to class 5,* **then** $R^d := R^d + e_{right}$

*belongs to class 6,* **then** $R^d := \begin{cases} R^d + e_{right}, & \text{if right successor is odd;} \\ R^d + e_{up} & \text{otherwise.} \end{cases}$

$L^d := L^d - R^d$

**end**

**Theorem 4.4** *For a layout $L$ in a tri-square-hexagonal grid Algorithm 4.3 constructs a subset $R^d$ of $L^d$ that contains no forbidden patterns for 5-layer wirability. The running time is linear in the size of the layout.*

**Proof** Algorithm 4.3 considers only those edges of $L^d$ shown in Figure 12 b). Observe that the parallel edges in $L^d$ are arranged around a hexagon. See Figure 14. Every sequence of four subsequent parallel edges in $R^d$ contains a vertical and a horizontal edge. An edge parallel to a horizontal edge is of diagonal direction and lies either above or below the horizontal edge. Then Algorithm 4.3 maintains the following invariants.

**I1** In $R^d$ there is no edge parallel to a vertical edge.

**I2** In $R^d$ there is no edge that is parallel to a horizontal edge and above that horizontal edge.

**I3** There are at most three subsequent parallel edges. Such a set of three parallel edges consists of a horizontal edge and two diagonal edges lying below the horizontal edge.

**I4** The maximum number of neighbored edges $\delta^{neighbored}(v)$ in $R^d$ incident to a vertex $v$ is

$$\delta^{neighbored}(v) := \begin{cases} 1, & \text{if } v \text{ is in class 1 or 4;} \\ 2, & \text{if } v \text{ is in class 2, 3, 5 or 6.} \end{cases}$$

**I5** The longest sequence of edges, where every two subsequent edges are neighbored consistes of two edges.

A necessary condition for a pattern of type 1) shown in Figure 9 a) are four parallel edges in $R^d$. This is impossible because of invariants I1, I2 and I3. A necessary condition for a pattern of type 2) shown in Figure 9 a) is a sequence of three parallel edges in $R^d$. These must lie according to I3. The lowermost of these is a diagonal edge and the uppermost is a horizontal edge. But then none of these edges will have a neighbored edge.

A necessary condition for a pattern of type 3) are two neighbored edges that both belong to a pair of parallel edges. This is impossible because of I1, I2 and I3.

A necessary condition for a pattern of type 4) are two parallel edges. These must lie according to I3. But not for both parallel edges there is a neighbored edge in $R^d$. Similarly, a necessary condition for a pattern of type 5) are two parallel edges which again lie according to I3. But because of I4, none of these parallel edges belongs to a set of three neighbored edges in $R^d$.

There are three possible configurations for a pattern of type 6). The configuration that all edges are incident to the same vertex is impossible because of I4. Three incident neighbored edges are impossible as well because of I4. Thirdly, in $R^d$ there occurs no sequence of four edges, where two subsequent edges are neighbored because of I5.

Obviously, Algorithm 4.3 can be implemented to run in time linear in the size of the layout. □

From a legal removal set determined by Algorithm 4.3, a 5-layer wiring of a layout in a tri-square-hexagonal grid can be constructed in linear time as well according to Theorem 3.7.

# 5 Concluding Remarks

We presented a general approach to the problem of wiring edge-disjoint layouts. Equivalent conditions for the $k$-layer wirability of an edge-disjoint layout where at most two wires meet in a vertex are given. Based on these conditions, we obtain linear-time algorithms to wire every layout in a tri-hexagonal grid and every layout in a tri-square-hexagonal grid using at most five layers. Our approach generalizes the framework introduced in [8]. There, equivalent conditions for the $k$-layer wirability of an edge-disjoint layout in a square grid are given. These conditions are based on a legal partition of the layout grid into a two-colorable map. A legal partition is characterized by "forbidden patterns" for the partition lines. The two color regions of the partition correspond to regions where horizontal edges are wired above vertical edges, resp. to regions where vertical edges are wired above horizontal edges. This framework is not applicable to more general grids resp. planar layout graphs, since there we can have layout edges of more than two different directions. The equivalent conditions for $k$-layer wirability developed in this paper are based on the characterization of legal removal sets. This leads to "forbidden pattern" as well, which are quite similar to the forbidden patterns given in [8]. Thus, our approach delivers a more general interpretation of the framework presented there.

**Acknowledgements** We thank Majid Sarrafzadeh for drawing our attention to the layer assignment problem for general planar layouts.

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