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Screen-Printed Al-Alloyed Rear Junction Solar Cell Concept Applied to Very Thin (100 µm) Large-Area n-Type Si Wafers

Y. Schiele*, F. Book, S. Seren, G. Hahn, B. Terheiden

University of Konstanz, Department of Physics, P.O. Box X916, D-78457 Konstanz, Germany

Abstract

Reducing the thickness of crystalline Si wafers processed to solar cells returns two significant benefits. Firstly, processing cost is reduced by saving cost- and energy-intensive Si material. Secondly, the required diffusion length of minority carriers is smaller, thus, wafers with a smaller carrier lifetime (e.g. due to higher base doping) can be utilized. In this work, the industrially feasible "PhosTop" cell concept is employed by manufacturing large-area n-type rear junction solar cells with a screen-printed Al-alloyed emitter featuring a selective phosphorous front surface field and a SiO_2/SiN_x passivation on the front.

PC1D simulations for substrates with different base doping concentrations show that the range of base resistivities utilizable for those PhosTop solar cells is extended towards higher doping concentrations with decreasing wafer thickness. PC1D forecasts a conversion efficiency of the chosen 2.8 Ωcm n-type Czochralski-Si wafers of 19.2% for 100 µm thickness, merely 0.1% less than for standard thickness but saving ~25% of the Si material. The manufactured thin large-area solar cells achieve a maximum efficiency of 19.0%.

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Keywords: thin wafers; n-type; Al emitter; selective

1. Introduction

Over 40% of module cost [1] and more than 50% of the energy payback time of a photovoltaic installation based on crystalline Si [2] is caused by the required Si feedstock, the crystal growing and

* Corresponding author. Tel: +49-7531-88-4995; fax: +49-7531-88-3895
E-mail address: yvonne.schiele@uni-konstanz.de

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wafering. Hence, reducing wafer thickness of crystalline Si solar cells substantially decreases energy consumption for fabrication and correspondingly cost per watt-peak of PV systems if conversion efficiency remains constant. Thus, wafer thickness in industrial solar cell production has been decreasing continuously on balance.

Furthermore, the required diffusion length of minority carriers in the Si bulk of thinner solar cells is expected to be smaller, which is relevant especially for rear junction cell concepts demanding high diffusion lengths. Thus, wafers with a smaller carrier lifetime (e.g. due to higher base doping) can be employed.

Replacing p-type Si wafers, predominantly utilized in current solar cell production, by n-type Si material provides various benefits. n-type Si is more tolerant of metal impurities as e.g. Fe [3] allowing a higher carrier diffusion length for the same impurity concentration. Additionally, no light-induced degradation (LID) of solar cell efficiency caused by boron-oxygen complexes [4] occurs.

In recent years, applying the industrial standard processing sequence for p-type Si solar cells to n-type substrates, known as the "PhosTop" cell concept [5], has proven a promising candidate for a simple and economical fabrication of n-type Si solar cells [6,7]. From this approach a solar cell with a phosphorous front surface field (FSF) and a screen-printed Al-alloyed rear emitter emerges.

2. PC1D Simulations

Applying the standard solar cell process to n-type silicon leads to the major difference that the p/n-junction is located on the rear of the device. Since most of the minority carriers are generated at the front, they need to have a larger diffusion length than in the front junction p-type solar cell. On the other hand, reduced wafer thickness results in a smaller distance between the place of generation and separation, tolerating a smaller diffusion length compared to thicker wafers.

In order to examine the potential of the described PhosTop solar cells depending on their wafer thickness by employing n-type Czochralski (Cz)-Si wafers with different base doping concentrations, PC1D simulations [8] are carried out. For these simulations, the following parameters are assumed:

- Base resistivities:
  $\rho = 0.55$ Ωcm (□), $\rho = 0.80$ Ωcm (○), $\rho = 1.5$ Ωcm (△), $\rho = 2.8$ Ωcm (▽), $\rho = 4.5$ Ωcm (◇)
- Effective minority carrier lifetime in Si bulk (solely limited by Auger recombination [9]):
  τ_{bulk}(□) = 2.0 ms, τ_{bulk}(○) = 3.7 ms, τ_{bulk}(△) = 9.6 ms, τ_{bulk}(▽) = 22 ms, τ_{bulk}(◇) = 37 ms
- Surface recombination velocity (SRV):
  Front SRV = 2.1×10^4 cm/s (adaption: PC1D fit of internal quantum efficiency (IQE) = measured IQE);
  Rear SRV = 1×10^7 cm/s (thermal limit)
- Doping profiles of the selective FSF and the Al-alloyed emitter:
  PC1D fit of profiles determined by electrochemical capacitance voltage (ECV) measurement
- Front reflectance: from reflectance measurement including metalization

For each of the different base resistivities, the PC1D simulations forecast the maximal conversion efficiency at a specific wafer thickness (Fig. 1); the higher the base doping concentration, the smaller the optimal thickness of the Si substrate and the sharper the optimum, which the reduced effective diffusion length caused by an increased doping concentration and therefore a less effective FSF accounts for. The highly resistive (4.5 Ωcm) material achieves its maximal efficiency potential at the industrial standard wafer thickness of approximately 200 µm, the highly doped (0.55 Ωcm) substrate at only 60 µm.

For the 2.8 Ωcm n-type wafers, the maximal solar cell efficiency of 19.3% is achieved at a thickness of approximately 165 µm, merely decreased by 0.1% at a thickness of 100 µm but saving ~25% of the Si material (assuming 140 µm kerf loss). Furthermore, 100 µm is a thickness which could be processed with adapted but conventional manufacturing technologies and equipment.

It has to be taken into account that the simulated solar cell concept features no special light trapping for thin wafers where less light is absorbed. Thus, there is still room for enhancing efficiency in the small thickness range.

Contrary to the conventional p-type solar cell, in the discussed n-type rear junction alternative, the base contributes to lateral conductivity and thus causes the series resistance to be smaller. This contribution is injection level dependent. For n-type Si with high resistivity, the base has a high injection level under illumination [6]. Therefore, a wide range of low doping concentrations can be employed. This range is further extended towards higher doping concentrations by reducing wafer thickness, as thinner solar cells tolerate smaller diffusion lengths. Among other benefits, this saves Si material (i.e. cost) and it provides the opportunity to utilize a larger ratio of the n-type Cz-Si ingot, in which base doping varies much more than in boron-doped Si due to the small segregation coefficient of phosphorous.

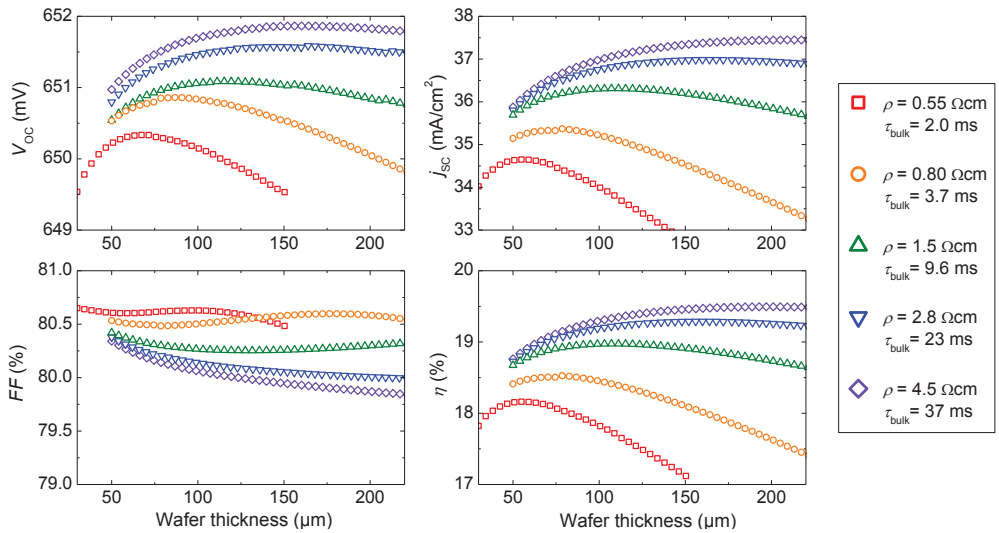

Fig. 1. PC1D simulated IV characteristics as a function of wafer thickness for different base resistivities ρ and the corresponding effective minority carrier lifetime in Si bulk τ_{bulk}. In the calculations of *FF*, lateral conductivity altering with ρ is disregarded since PC1D assumes a one-dimensional device

3. Experimental

Manufacturing solar cells based on the PhosTop concept is an industrially feasible method for large-area n-type Si solar cells. As substrate, n-type Cz-Si with an area of 125×125 mm^2 semi-square and a base resistivity of 2.8 Ωcm (determined by ECV measurement after $POCl_3$ diffusion and oxidation) is utilized. The effective minority carrier lifetime measured on Al_2O_3 passivated lifetime samples of this material after the high temperature process steps is τ_{eff} = 13 ms. However, the IV results of the PC1D simulation calculated by this value instead of the Auger limit do not change relevantly. In order to significantly reduce the amount of Si material, but continue using conventional processing, a wafer thickness of 100 µm after texturization is chosen. The emitter is formed by alloying the full-area screen-printed Al on the rear into the silicon wafer. The silver finger grid on the front is established by screen-printing, too.

Cell performance of the n-type rear junction cell concept is limited mainly by its front surface recombination velocity, in particular with low ohmic substrates [6]. Therefore, an improved front surface passivation and antireflection coating (ARC) consisting of a SiO_2/SiN_x stack is applied. Additionally, in order to keep the minority carriers off the front surface, a phosphorous FSF is diffused into the Si surface.

The improvement in the form of a reduced carrier recombination rate and a lower contact resistivity is investigated by comparing a heavily $POCl_3$-diffused and selectively etched-back FSF with a homogeneous 50 Ω/□ reference FSF.

In order to examine the differences occurring due to the reduction of the thickness, PhosTop solar cells are manufactured from wafers with a standard thickness of 180 µm as a reference complementary to the 100 µm thin wafers. As the thermal capacity of the thin solar cells is considerably smaller, they are more sensitive to variations of the co-firing parameters which must be accurately adapted. The processing sequence and the resulting composition of the described PhosTop solar cell are depicted in Fig. 2.

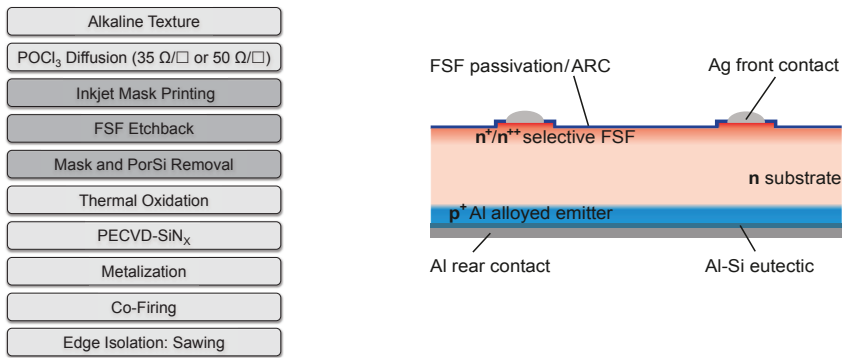

Fig. 2. (a) Processing sequence and (b) schematic representation of the PhosTop solar cell with selective FSF, SiO_2/SiN_x passivation/ARC on the front, Al-alloyed emitter on the rear and screen-printed metal contacts

4. Solar Cell Results

4.1. Electrical characterization

IV measurements of the best solar cells, manufactured according to the procedure described in section 3, yield the results listed in Table 1. The solar cells with selective FSF achieve efficiencies of up to $\eta = 19.3\%$ compared to the homogeneous FSF samples with $\eta = 18.1\%$. In general, the samples with selective FSF exhibit an increased short circuit current density j_{SC} (~2 mA/cm^2) and open circuit voltage V_{OC} (~10 mV) compared to the references with homogeneous FSF which can be explained by the reduced minority carrier recombination rate due to a lower doping concentration in the etched-back regions and a better passivation of these regions by the SiO_2/SiN_x stack. This causes an increased IQE particularly at small wavelengths (Fig. 3a) enhancing j_{SC} as well as a reduced saturation current density j_{01} ($\Delta j_{01} \approx 2\times10^{-13}$ A/cm^2) increasing V_{OC}.

The profile of the electrically active phosphorous doping concentration is found to have changed during the high temperature oxidation. In ECV measurements, a reduced surface doping concentration and a deeper driven-in concentration profile after oxidation is observable (Fig. 3b), in particular with solar cells featuring a homogeneous FSF. This yields a higher contact resistivity and thus a larger series resistance R_S of the homogeneous FSF solar cells.

The IQE measurements (Fig. 3a) indicate that the current losses of the thin solar cells in the long wavelength range are partly compensated by a slightly increased IQE between 400 and 850 nm. Comparing the selective FSF solar cells of different wafer thicknesses by means of the PC1D calculations, it is observed that j_{SC}, V_{OC}, and *FF* vary only marginally. The almost negligible difference in the resulting efficiency (19.2% at 100 µm) suggests the PhosTop process applied to 100 µm thin wafers to be promising.

The measured j_{SC} and V_{OC} values are in very good accordance with the simulated values. The marginally fallen short *FF* of the thin solar cells with selective FSF is mainly caused by finger interruptions (Fig. 4b) and cracks which are both observable in electroluminescence images (Fig. 4a).

Table 1. Comparison of the best IV characteristics measured on the manufactured thin solar cells and on the samples with standard thickness (area=148 cm^2) with selective FSF and the reference homogeneous FSF. Additionally, the IV characteristics of a 100 µm and a 180 µm thick solar cell with selective FSF prognosticated by PC1D are listed. Series resistances R_S and saturation current densities j_{01} are obtained from two-diode model fits of the illuminated solar cell IV curves

Solar cell type	V_{OC} **(mV)**	j_{SC} **(mA/cm^2)**	*FF* **(%)**	η **(%)**	R_S **(Ωcm^2)**	j_{01} **(A/cm^2)**
Hom. FSF						
180 µm	643	35.2	79.8	18.1	0.38	4.9×10^{-13}
100 µm	643	34.9	80.3	18.0	0.40	5.2×10^{-13}
Sel. FSF						
180 µm	652	36.9	80.0	19.3	0.24	3.0×10^{-13}
100 µm	651	36.6	79.8	19.0	0.24	2.9×10^{-13}
PC1D (sel. FSF)						
180 µm	652	37.0	80.0	19.3		
100 µm	651	36.8	80.1	19.2		

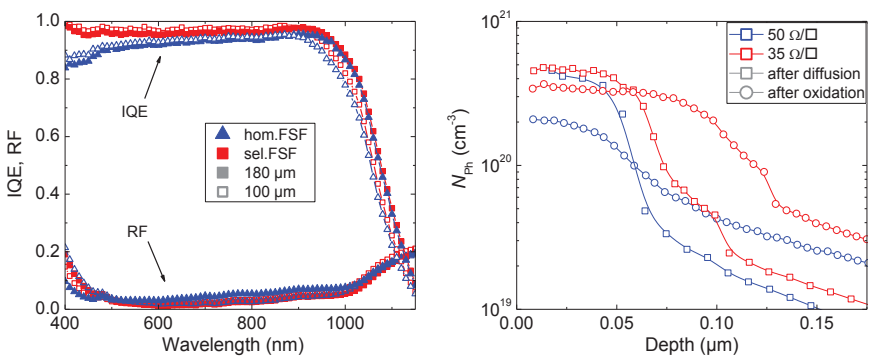

Fig. 3. (a) Internal quantum efficiency (IQE) and reflectance (RF) of thin solar cells with homogeneous/selective FSF compared to the corresponding data of samples with standard thickness (scaled to j_{SC} from measured IV characteristics). (b) Phosphorous doping profiles of hom. and sel. FSF determined by ECV measurement after $POCl_3$ diffusion and after subsequent thermal oxidation

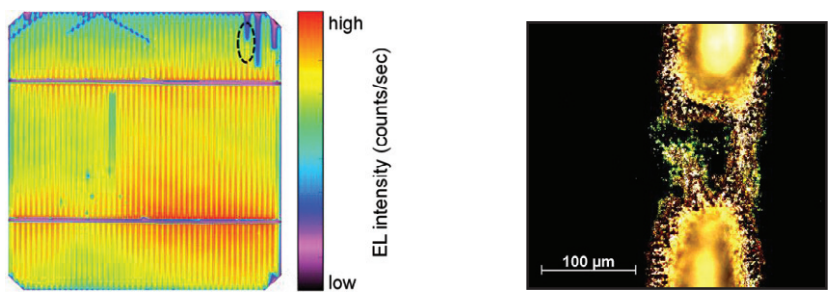

Fig. 4. (a) Electroluminescence image of the best 100 µm thin PhosTop solar cell with selective FSF depicting finger interruptions and cracks at the edge. (b) Microscope image of finger interruption

4.2. Solar cell bend

As the back contact of the PhosTop solar cells in this work is established by full-area screen-printing of Al paste, the solar cells suffer from the bimetal effect. This causes a strong mechanical bend (bow) of the solar cells featuring a reduced thickness of 100 µm (~6 mm, see Fig. 5a, top).

The bimetal effect is caused by a significantly higher temperature averaged linear thermal coefficient of expansion (TCE) of AlSi (TCE = 23×10^{-6} K^{-1} [10]) compared to Si (TCE = 3.5×10^{-6} K^{-1} [11]). During co-firing, a liquid phase consisting of Si and Al is formed, from which a Si layer doped with Al (emitter) grows epitaxially on the wafer, whereafter the remaining AlSi liquid solidifies (eutectic) at temperatures below 577°C. During cooling down to room temperature, eutectic and paste matrix contract more than the Si wafer leading to a convex wafer bow (Fig. 5b). In order to reverse this deformation, the solar cell is now further cooled down to approximately -50°C. Then, the sample heats up again with AlSi expanding more than Si, finally yielding a flat solar cell at room temperature (Fig. 5a, bottom) [12].

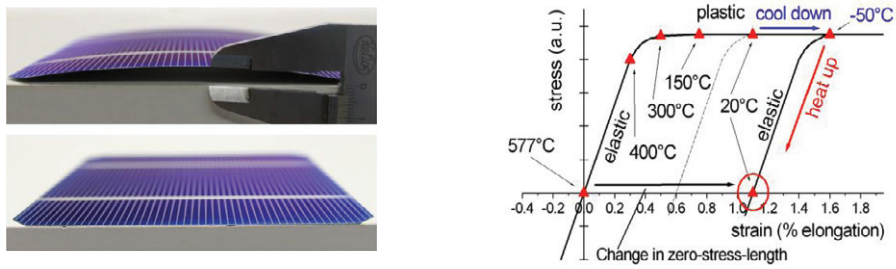

Fig. 5. (a) Solar cell with bow of ~6 mm (top), same solar cell after removing the bow (bottom). (b) Stress – strain diagram during cooling down of the solar cell after co-firing and during procedure of bow removal [12]

It is demonstrated that the IV characteristics of the PhosTop solar cells are not altered by the described bow removal procedure. Accordingly, the manufactured solar cells are flattened after co-firing and prior to the different characterization steps in order to avoid mechanical stress by handling (vacuum chucks etc.) which would cause additional cracks.

5. Conclusion

In this work, the industrially feasible PhosTop cell concept was employed to manufacture large-area n-type rear junction solar cells with screen-printed Al-alloyed emitter featuring a selective phosphorous front surface field and a SiO_2/SiN_x passivation on the front. PC1D simulations for substrates with different base doping concentrations have shown that the range of base resistivities utilizable for the PhosTop solar cells is extended towards higher doping concentrations with decreasing wafer thickness. For the chosen 2.8 Ωcm n-type Cz-Si wafers a potential conversion efficiency of 19.2% for 100 µm thickness has been calculated, merely 0.1% less than for standard wafer thickness but saving ~25% of the Si material.

The PhosTop solar cells with a strongly reduced wafer thickness suffered from the bimetal effect due to the full-area screen-printed Al paste. However, the resulting mechanical bend could be eliminated by a quick and simple cooling procedure. Despite the mechanical stress, the manufactured 100 µm thin large-area solar cells from Cz-Si have achieved a maximum efficiency of 19.0%.

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References

[1] Powell DM, Winkler MT, Choi HJ, Simmons CB, Berney Needleman D, Buonassisi T. Crystalline silicon photovoltaics: a cost analysis framework for determining technology pathways to reach baseload electricity costs. *Energy Environ Sci* 2012;**5**:5874-83.

[2] Sinke WC, van Hooff W, Coletti G, Ehlen B, Hahn G, Reber S et al. Wafer-based crystalline silicon modules at 1 €/WP: final results from the Crystalclear integrated project. *Proc 24th EU PVSEC*, Hamburg, Germany, 2009, p. 845-56.

[3] Macdonald D, Geerligs LJ. Recombination activity of interstitial iron and other transition metal point defects in p- and n-type crystalline silicon. *Appl Phys Lett* 2004;**85**:4061-3.

[4] Glunz SW, Rein S, Lee JY, Warta W. Minority carrier lifetime degradation in boron-doped Czochralski silicon. *J Appl Phys* 2001;**90**: 2397-404.

[5] Meier DL, Davis HP, Garcia RA, Salami J, Rohatgi A, Ebong A, Doshi P. Aluminum alloy back p-n junction dendritic web silicon solar cell. *Sol En Mat & Solar Cells* 2001;**65**:621-7.

[6] Book F, Wiedenmann T, Schubert G, Plagwitz H, Hahn G. Influence of the front surface passivation quality on large area n-type silicon solar cells with Al-alloyed rear emitter. *En Proc* 2011;**8**:487-92.

[7] Schmiga C, Rauer M, Rüdiger M, Meyer K, Lossen J, Krokoszinski H-J et al. Aluminium-doped p^+ silicon for rear emitters and back surface fields: results and potentials of industrial n- and p-type solar cells. *Proc 25th EU PVSEC*, Valencia, Spain, 2010, p. 1163-8.

[8] Clugston DA, Basore PA. PC1D version 5: 32-bit solar cell modeling on personal computers. *Proc 26th IEEE PVSC*, Anaheim, CA, USA, 1997, p. 207-10.

[9] Kerr MJ, Cuevas A. General parameterization of Auger recombination in crystalline silicon. *J Appl Phys* 2002;**91**:2473-80.

[10] Touloukian YS (Ed). *Thermal expansion: metallic elements and alloys*. New York: IFI/Plenum; 1975; p. 658.

[11] Okada Y, Tokumaru Y. Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 K. *J Appl Phys* 1984;**56**:314-20

[12] Huster F. Aluminium-back surface field: bow investigation and elimination. *Proc 20th EU PVSEC*, Barcelona, Spain, 2005, p. 635-8.