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THE ETCHBACK SELECTIVE EMITTER TECHNOLOGY AND ITS APPLICATION TO MULTICRYSTALLINE SILICON

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ABSTRACT

We have developed a simple and industrially applicable selective emitter cell process using only one diffusion step and an emitter etchback to create the high sheet resistance emitter [1, 2]. The process generates a deeper doping profile with a lower surface phosphorous concentration than a directly diffused emitter with the same sheet resistance. This results in an extremely low emitter saturation current j_{0E} even at a moderate sheet resistance of 60-80 Ω/□. The highest independently confirmed cell efficiency on Cz-Si (146 cm²) was 18.7%.

In this work the etching behavior of the acidic solution at the grain boundaries is studied by SEM imaging and high resolution LBIC measurements at 405 nm wavelength. The etchback also leads to a change in reflectivity, which is quantified by reflectance measurements. We furthermore investigate the influence of the base material quality on the gain that can be achieved by this process. Large area solar cells have been processed from solar grade and UMG mc silicon.

INTRODUCTION

On today's industrial type silicon solar cells, the front side is homogeneously doped to a level of typically 50-60 Ω/□, which is a compromise between emitter performance and sufficiently low contact resistance. This compromise can be overcome by a selective emitter, which is heavily doped underneath the contact grid, and weakly doped in the illuminated area. This leads to a reduced contact resistance as well as lower Auger and SRH recombination, resulting in an improved blue response and a higher open circuit voltage.

For the formation of a selective emitter, numerous production sequences have been published, but only few technologies have been implemented into industrial cell production, since the achievable gain is limited and the additional production costs have to be low.

We have developed a simple production sequence that uses one diffusion step and only processing equipment that is already established in an industrial production environment [1, 2].

CELL CONCEPT

The processing sequence used to create the selective emitter structure is based on the standard screen printing process which is widely used in industrial production.

It starts with damage etching and a heavy diffusion, subsequently the emitter is masked by inkjet or screen-printing in the area that will be contacted. The emitter is then etched back in an acidic solution to the desired sheet resistance. During the etching process, a thin layer of porous silicon is formed, which acts like an antireflective coating (ARC), so the resulting emitter sheet resistance and the etching homogeneity can be controlled by the wafer color. The porous silicon and the masking layer are subsequently removed in an alkaline solution. The following process steps remain unchanged from the standard process, which continues with the plasma enhanced chemical vapor deposition (PECVD) of SiN_X, screen-printing of the metallization, co-firing and edge isolation.

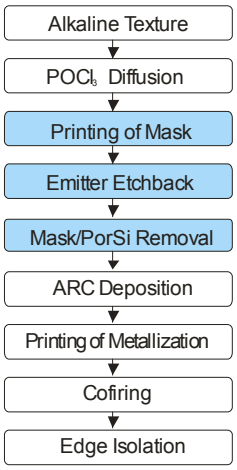

Figure 1 Processing sequence for the production of an etchback selective emitter solar cell. The additional steps to the standard screen-printing process are marked in blue.

EMITTER CHARACTERIZATION

The etchback process leads to a different emitter profile compared to a direct $POCl_3$ diffusion. Fig. 3 shows the SIMS profiles of a 90 Ω/□ direct diffusion and a 50 Ω/□ diffusion (increased diffusion temperature) that was etched back to 90 Ω/□. The emitter quality is characterized by symmetrical QSSPC samples on 0.5 Ωcm FZ-Si. Fig. 3 shows the superior quality of the etchback emitter compared to the directly diffused emitter at the same sheet resistance due to the deeper doping profile and lower surface phosphorous concentration. The emitter can be further improved by etching back from a lower starting sheet resistance, which also lowers the contact resistance

of the final solar cell. When etching back from 17 Ω/□, an extremely low j_{0E} of 28 fA/cm² at 68 Ω/□ was achieved [3]. This for a selective emitter cell comparably low sheet resistance allows for a large finger spacing and therefore a higher short circuit current density j_{SC}. Since in contrast to the gain in V_{OC} part of the gain in j_{SC} is lost after encapsulation due to the short wavelength absorption of the glass, the lower sheet resistance compared to a directly diffused selective emitter can also be used to improve the fill factor instead of j_{SC}, this gain is then completely transferred to the module.

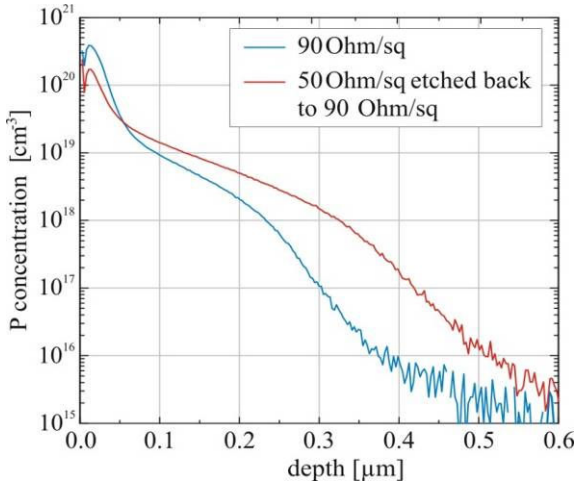

Figure 2 SIMS profiles of a 90 Ω/□ direct diffusion and a 50 Ohm/sq diffusion etched back to 90 Ω/□.

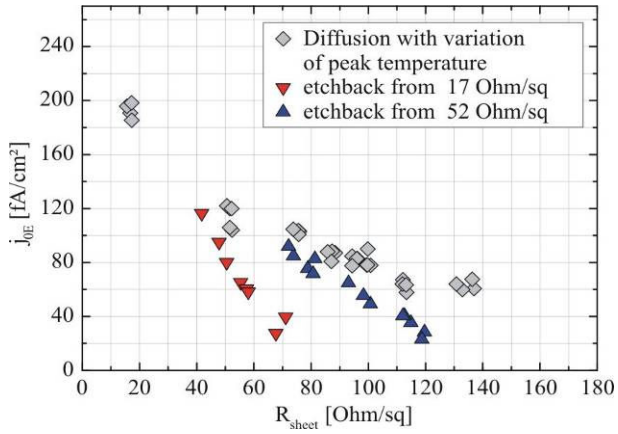

Figure 3 Comparison of j_{0E} from directly diffused QSSPC samples and emitters etched back from 17 and 52 Ω/□.

ETCHING BEHAVIOUR

A limiting factor for using a lower starting sheet resistance may be the increased etchback depth which affects the surface texture and reflection of the solar cell. The etching depth was studied by SEM imaging on random pyramid textured Cz-Si wafers, since this texture provides a well defined surface structure. Images before (see Fig. 4) and after (see Fig. 5) removing the porous silicon show, that the valleys of the texture are rounded by the etchback, while the tips remain sharp. The etchback depth of 265 nm on these wafers was chosen much deeper than the typical depth removed from a solar cell (approx. 60 nm).

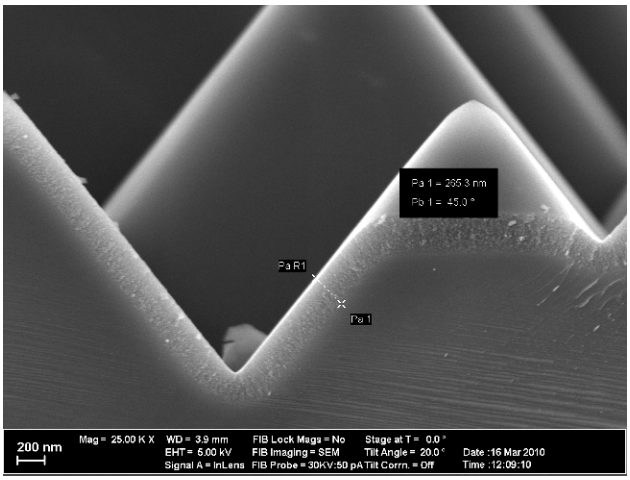

Figure 4 SEM image of a 265 nm layer of porous silicon on a random pyramid textured Cz-Si wafer.

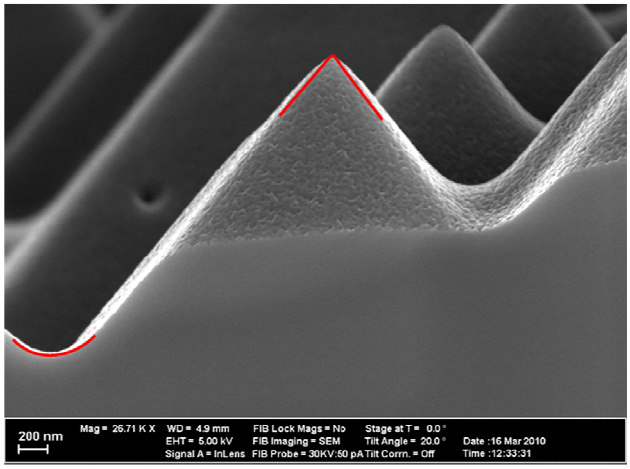

Figure 5 SEM image of a random pyramid textured Cz-Si wafer after removing the 265 nm thick porous silicon layer.

The influence of the increased reflection from the valleys of the texture was investigated by measuring the reflection vs. wavelength of random pyramid textured Cz-Si wafers with PECVD-SiN_X coating. The etchback depth was calculated from the reflection minimum of the porous silicon using n = 1.6. For the calculation of the short circuit current density (loss) a typical internal quantum efficiency of a selective emitter solar cell was used. Although the reflection is also affected by the free carrier absorption and the SiN_X layer was not adapted to the reflexion

properties, this allows an estimation of the upper limit of the current loss (Fig. 6). Since the acidic texture on multicrystalline wafers results in sharp tips and round valleys, a lower current loss can be expected.

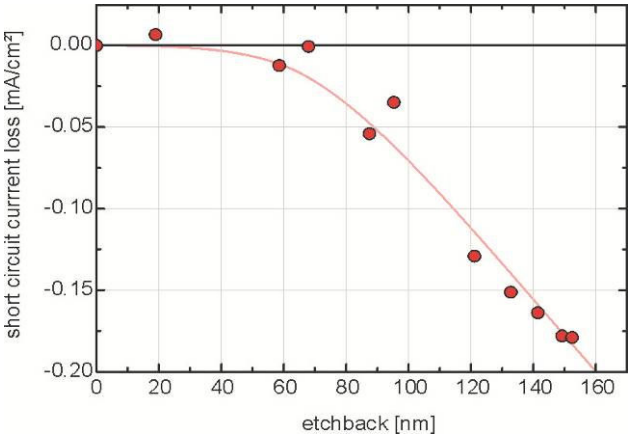

Figure 6 j_{sc} loss vs. etchback depth calculated from measured reflectance data using a typical random pyramid textured selective emitter solar cell IQE. The loss for an etchback of less than 90 nm can be estimated to < 0.05 mA/cm². The red line is a guide to the eye.

For multicrystalline silicon, the etching behaviour at the grain boundaries was studied by SEM imaging on chemically polished samples. It can be observed that on some grain boundaries, the etchback process leads to grooves, while most of them remain flat.

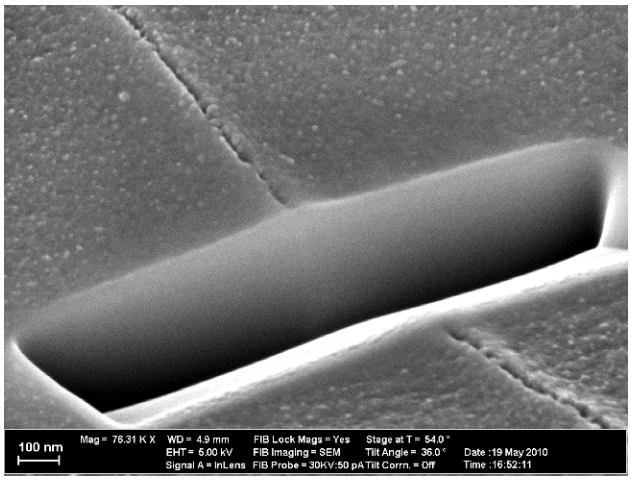

Figure 7 SEM image of FIB cut at an etching groove after an etchback of approx. 60 nm.

Fig. 7 shows the cross-section of such a groove at a grain boundary cut by a focused ion beam (FIB) after an etchback of approx. 60 nm and subsequent removal of the porous silicon. Although the groove is visible from the top view, its depth cannot be determined from the cross-section. In order to obtain a better image of the effect, another sample was etched back by approx. 220 nm. The cross-section of the etched grain boundary now shows a groove of approx. 250 nm depth. From the asymmetry of the groove and the fact that only few grain boundaries are etched, it can be concluded that the increased etching rate only occurs at certain crystal orientations at the grain boundary surface. EBSD imaging could lead to a deeper understanding of this behavior.

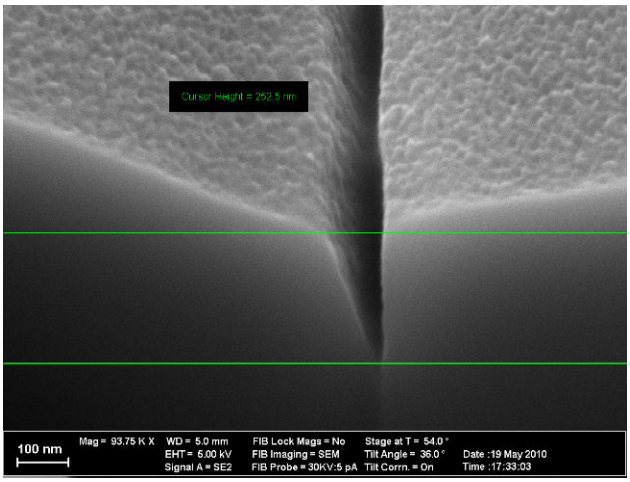

Figure 8 SEM image of an etching groove after an etchback of approx. 220 nm.

The observed grooves could be an explanation of the fact that the open circuit voltage gain achieved by the etchback selective emitter process is much smaller for mc-Si solar cells with a very high density of dislocations and grain boundaries.

SELECTIVE EMITTER SOLAR CELLS

Monocrystalline Silicon

5" solar cells were processed from 2.8 Ωcm Cz-Si according to the scheme in Fig. 1. As a reference emitter, a 45 Ω/□ diffusion was chosen. The selective emitter was etched back from 30 Ω/□ to approx. 65 Ω/□. For all printing steps, a screen-printer was used. A full area aluminum BSF without soldering pads was used for rear side metallization and the edge isolation was carried out with an automatic dicing saw. The average IV results are shown in Table I. The best independently confirmed selective emitter solar cell efficiency was 18.7%.

	FF [%]	V_{OC} [mV]	j_{SC} [mA/cm²]	η [%]
Reference	78.1	629	36.9	18.2
SE	78.1	639	37.5	18.7

Table I Average IV measurement results of 5" Cz-Si solar cells (Average over 9 cells per group).

Multicrystalline Silicon

For the multicrystalline solar cells, we used 5" solar grade material of two different qualities. The process parameters are the same as for the Cz-Si solar cells. For the used low quality material a higher density of grain boundaries can be observed on electroluminescence (EL) images (see Fig. 9).

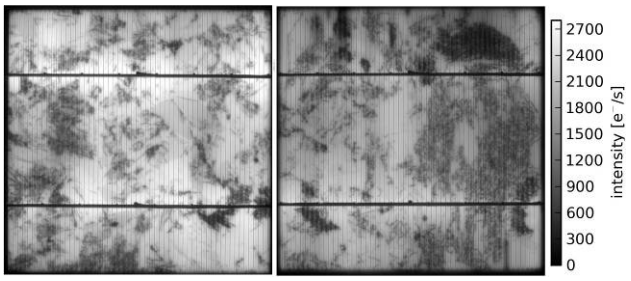

Figure 9 Electroluminescence images of selective emitter solar cells from solar grade mc silicon with a low (left) and high (right) density of grain boundaries.

	Quality	FF [%]	V_{OC} [mV]	j_{SC} [mA/cm^2]	η [%]
Reference	high	79.1	612	33.1	16.0
SE	high	78.2	617	34.1	16.5
Reference	low	77.7	611	33.0	15.7
SE	low	76.2	610	33.4	15.5

Table II IV measurement results of 5" solar grade mc-Si solar cells (Average over 3 – 12 cells per group). The different base materials were not processed in one batch, but with the same processing parameters.

The IV results of Table II indicate that the gain achieved by the etchback selective emitter process strongly depends on the base material quality. The gain in V_{OC} for the first group is 5 mV smaller compared to the monocrystalline cells, although the decreased fill factor and the higher gain in j_{SC} indicate a heavier etchback. The second group with a high density of grain boundaries even shows a loss of 1 mV compared to the reference, the gain in j_{SC} is only 0.4 mA. The reduced cell performance of this group could be explained by the increased etching rate at some dislocations and grain boundaries.

Ingot height dependence of the gain in j_{SC} and V_{OC}

A batch of 6" upgraded metallurgical grade (UMG) mc-Si solar cells was processed from one ingot. A 55 Ω/□ emitter was chosen as a reference, the selective emitter was etched back from 40 Ω/□ to approx. 60 Ω/□. The distribution of V_{OC} and j_{SC} vs. ingot height is shown in Fig. 10. The reference cells show a decrease in wafer quality with increasing wafer number, on EL images (not shown here) a strong increase in density of grain boundaries can be observed. On the selective emitter cells a gain in V_{OC} could only be achieved for low wafer numbers. The gain in j_{SC} is slightly reduced for high wafer numbers.

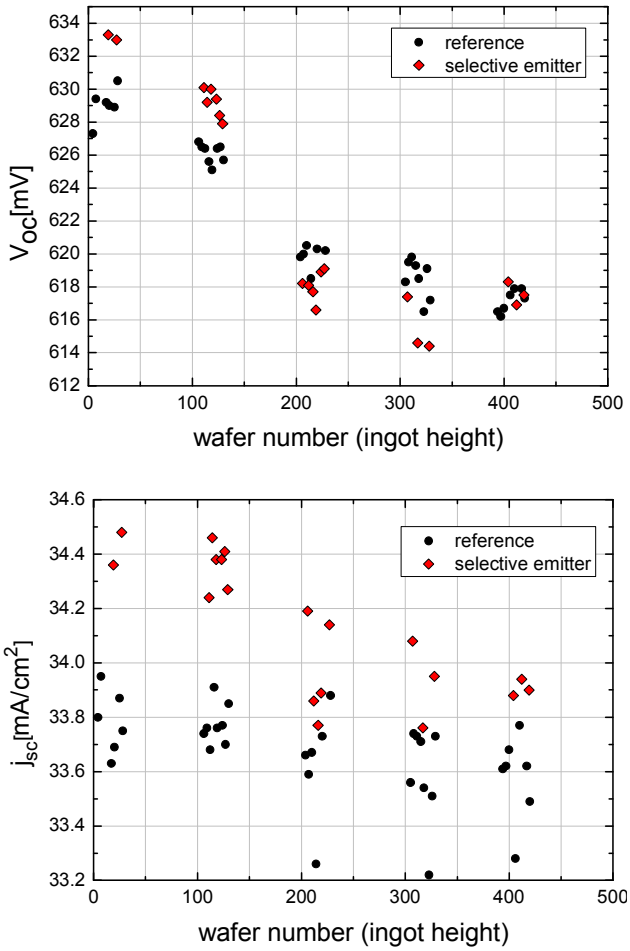

Figure 10 V_{OC} (top) and j_{SC} (bottom) distribution vs. ingot height of a 6" UMG mc-Si ingot. The best selective emitter solar cell resulted in an efficiency of 16.8 %.

Fig. 11 shows the internal quantum efficiency (IQE) of a reference and a selective emitter solar cell processed from neighboring wafers. On each cell measurements were taken from an area of high and low density of grain boundaries visible in the EL image.

The difference in wafer quality has a strong influence of the long wavelength IQE, while in the short wavelength region the IQE of the reference cell is not affected. For the selective emitter a slight reduction can be observed, which is in good agreement to the j_{SC} data from Fig. 10.

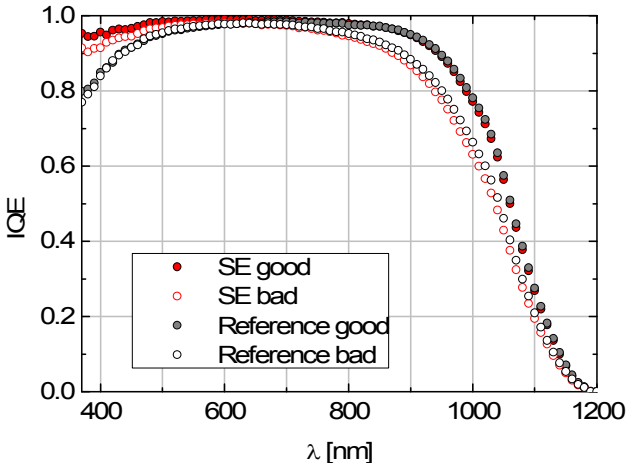

Figure 11 IQE of reference and a selective emitter solar cell. Measurements were taken from an area of low (good) and high (bad) density of grain boundaries.

In order to locally investigate the current generation, high resolution LBIC maps were performed on neighboring reference and selective emitter solar cells from the top region of the ingot at wavelengths of 980 nm and 405 nm (see Fig. 12, 13). The rectangle in Fig. 12 contains areas of high and low grain boundary density which can be well separated at 980 nm. Fig. 13 shows the same area mapped at 405 nm on both cells. The left side with a high density of grain boundaries generates an even higher I_{SC} than the right side. This is caused by the lower reflection in this area due to a better acidic texture. In order to separate this effect, a reflectance measurement would be necessary which is not yet implemented in our setup. The higher I_{SC} of the selective emitter cell between the grid lines as well as the approx. 400 µm wide heavily doped regions underneath the gridlines are well visible.

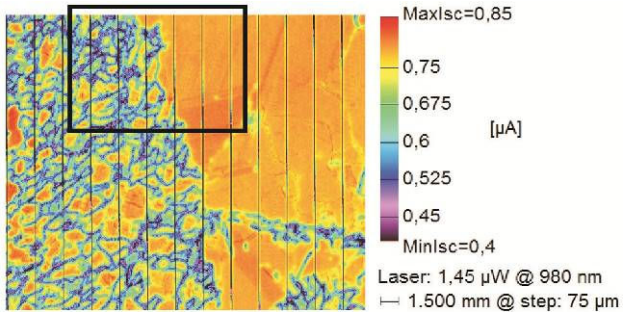

Figure 12 LBIC map of a part of a selective emitter mc-Si solar cell from the top region of the ingot at 980 nm wavelength. The rectangle indicates the area also measured at 405 nm (see Fig. 13).

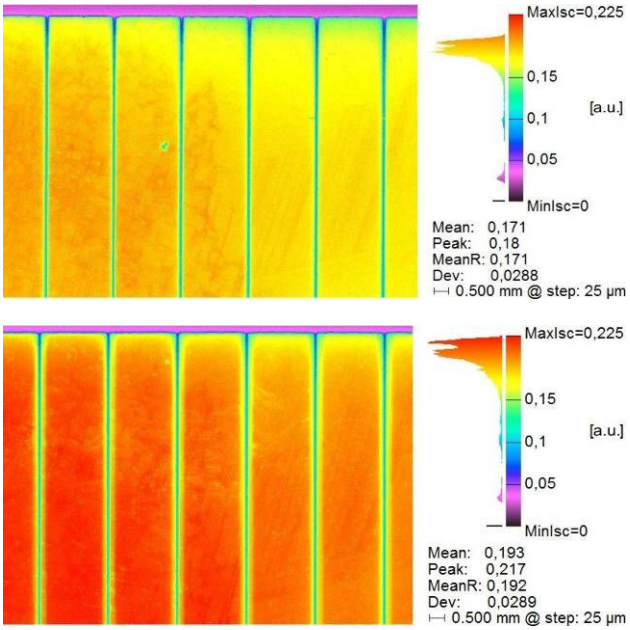

Figure 13 LBIC maps of neighboring mc-Si solar cells from the top region of the ingot. Measurements were taken at 405 nm wavelength from the rectangle marked in Fig. 12.
Top: reference emitter (same cell as in Fig. 12)
Bottom: selective emitter

SUMMARY

The etchback selective emitter process developed at University of Konstanz has resulted in an efficiency improvement of $0.5\%_{abs}$ on large are solar cells from Cz and mc silicon, leading to a highest cell efficiency of 18.7%. During the emitter etchback, the valleys of a random pyramid texture are rounded while the tips stay sharp, the loss in j_{SC} due to this effect can be estimated to < 0.05 mA/cm² for an etchback of less than 90 nm.

For mc silicon, an increased etching rate at some grain boundaries could be observed on SEM images, leading to grooves which are likely to cause a reduction in V_{OC}. The IV results of mc silicon solar cells from material of different quality and position in the ingot indicate that this reduction is correlated to the density of grain boundaries visible in EL images. For base material with a very high density of grain boundaries, the gain in j_{SC} is also slightly reduced.

On high resolution LBIC measurements of areas with a high and a low density of grain boundaries, the improved I_{SC} of the selective emitter cell at 405 nm wavelength is visible. The area with a high dislocation density leads to a higher I_{SC} for the reference and the selective emitter cells due to better reflection properties.

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REFERENCES

[1] H. Haverkamp et al.: *'Minimizing the Electrical Losses on the Front Side: Development of a Selective Emitter Process from a Single Diffusion'*, Proc. 33rd IEEE PVSC, San Diego, 2008

[2] A. Dastgheib-Shirazi et al.: *'Selective Emitter for Industrial Solar Cell Production: a Wet Chemical Approach Using a Single Diffusion Process'*, Proc. 23rd EU PVSEC, Valencia, 2008, 1197

[3] F. Book et al.: *'Detailed Analysis of High Sheet Resistance Emitters for Selectively Doped Silicon Solar Cells'*, Proc. 24th EU PVSEC, Hamburg, 2009, 1719