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Increasing Robustness of EpiWafer Transfer Process Leading to Carrier Lifetimes of 1.6 ms Using Large Scale Production Feasible Substrate Wafers

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Abstract. In the layer transfer process, the appropriate tuning of the porosity and the thickness of the porous silicon layer stack is crucial for the reorganization process und thus for the crystal quality of the epitaxially grown silicon wafer (EpiWafer). In anodic electrochemical etching of silicon, the layer thickness is controlled by the etch duration. For a substrate with a given doping density etched in a given electrolyte, the porosity can be adjusted solely through the applied current density. As this may be a limitation to obtain very different porosities for the layers of the stack, we used different electrolytes to etch the different layers of the stack. This way, higher porosity values can be achieved for the detachment layer while keeping low porosity for the seed layer. By doing so, the range of applicable process parameters is increased. Using a very thick stack of three porous layers, we demonstrate a minority carrier lifetime of about 1.6 ms for an n-type (1 Ωcm) EpiWafer grown on non-polished and not shiny-etched but KOH saw damage etched substrate wafer.

INTRODUCTION

In the layer transfer process as introduced by Brendel in 1997 [1], the properties of the porous silicon stack strongly influence the crystal quality of the epitaxially grown silicon wafer (EpiWafer). This porous layer stack is often a double layer consisting of a low-porosity layer (LPL), on which the silicon is deposited, on top of a high-porosity layer (HPL) for detachment. After the reorganization, the top surface of the porous layer stack has to be completely closed and free of voids to allow a defect-free epitaxial silicon growth. For this, the porosity of the LPL has to be as low as possible [2]. Additionally, after reorganization the detachment layer should then be solely consisting of large extended voids and homogeneously distributed thin pillars connecting the bulk of the substrate wafer to the LPL [3]. The number and diameter of the pillars have to be optimized to prevent the use of large mechanical forces for the detachment that would induce large mechanical stresses in the EpiWafer, which may lead to cracks and micro-cracks that negatively impact minority carrier lifetime. For this, the porosity of the detachment layer has to be high. In addition to the reorganization parameters, the layer thicknesses, the pore size and distribution, as well as the porosities of both

layers play a decisive role for a successful detachment of the EpiWafer. The beginning of the etching process is a random process depending on the electrical and crystallographic conditions at the surface. Up to now, most results published regarding porous silicon etching for the transfer process rely on etching polished or shiny etched wafer surfaces [2, 4, 5]. In contrast, this contribution deals with a study of porous layer etching on rough p-type Cz-Si wafers with a standard saw damage etched in KOH-solution. We focus on the dependence of the porosity on wafer resistivity, applied current and HF concentration in the electrolyte aiming at a large process window for the reorganization and epitaxy process.

EXPERIMENTAL

Porosification

The first step of the above-mentioned layer transfer process is the porosification of the seed wafer. The wafers used are 156.7×156.7 mm² full square, (100)-oriented highly boron-doped (p-type) Cz-Si with a resistivity of about 11 mΩcm. They are not polished, but have a rough surface from standard saw damage etch in KOH solution. The electrochemical etching was performed anodically in a double cell tool from AMMT GmbH using an electrolyte containing HF, water and an alcohol as wetting agent. For a given doping level of the seed wafer and a given electrolyte, the applied current density determines the porosity. The etching duration defines the layer thickness. Pore size and distribution depend mostly on the doping level of the wafer used, the HF concentration in the electrolyte, and the applied current density. Different current densities are applied to obtain a layer stack with different porosity. After etching, the as-prepared layer was characterized by measuring the reflectance in the visible and up to the infrared spectral range. Fitting the reflectance spectra of several points on the wafer yields a spatially resolved representation of the porosity and layer thickness of both the single and double layer [6]. In addition, the layer thickness in cross-section can be determined with a scanning electron microscope (SEM).

Reorganization and Epitaxy

The reorganization and the epitaxial Si growth were carried out at Fraunhofer-Institute for Solar Energy Systems (ISE) in an atmospheric pressure chemical vapor deposition (CVD) epitaxy reactor [7]. The reorganization was performed for several minutes under hydrogen ambient at temperature around 1090°C. The epitaxial Si growth took place at the same temperature under trichlorosilane ($SiHCl_3$) and hydrogen (H_2) as precursor gases and phosphine (PH_3) for the doping [7]. The Si deposition rate was about 1 µm/min [7] and a ~140 µm thick n-type Si (EpiWafer) with a resistivity of ~1 Ωcm was grown. The detachment of the EpiWafer from the seed wafer was carried out by NexWafe GmbH using an automatic tool after defining a 125×125 mm² full square surface using a dicing saw.

Lifetime Sample Preparation

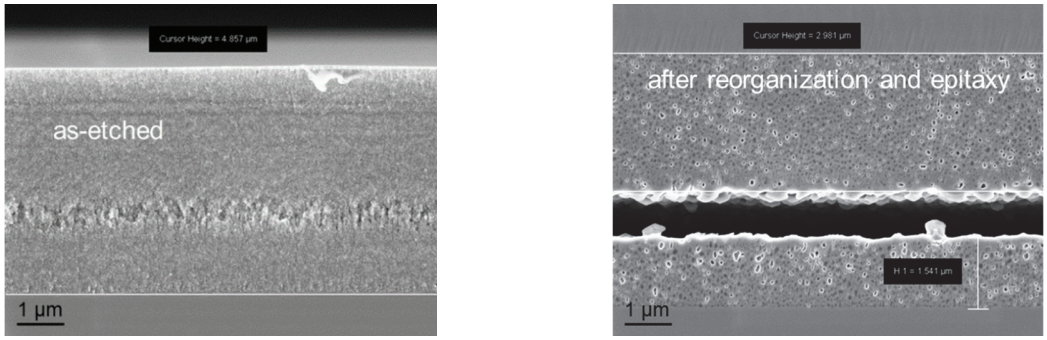
The lifetime measurement was performed on 50×50 mm² samples cut from the 125×125 mm² full square EpiWafers by laser. The residual porous layer and the parasitic, diffused boron-doped layer on the backside were removed in a KOH solution. Afterwards, the surface was cleaned in an ozone solution followed by a Piranha solution and then passivated with ~30 nm thick Al_2O_3 by plasma assisted Atomic Layer Deposition (ALD). Subsequently, an annealing process was performed at ~420°C under nitrogen atmosphere to activate the passivation, and the minority carrier lifetime was measured by photoconductance decay (PCD) and photoluminescence (PL). After this first lifetime measurement in the as-grown state, the passivation layer was removed in an HF solution. The surface was then cleaned as described above and a phosphorus gettering step was applied by means of a $POCl_3$ diffusion. It is a standard $POCl_3$ diffusion process as used in the solar cell process with a temperature plateau at 837°C and no holding step at a lower temperature at the end to improve the gettering efficiency, as usually reported in the literature [4, 5]. Afterwards, the phosphosilicate glass layer and the highly phosphorus-doped layer were removed in an HF solution and in a KOH solution, respectively. Another cleaning step of the surface as described above was performed and the surface was passivated again. Then a second lifetime measurement was carried out after a similar annealing step as described above.

INCREASING THE ROBUSTNESS OF THE TRANSFER PROCESS BY USING A THREE LAYER STACK

We develop a layer stack, which is very stable and robust regarding the detachment after reorganization and subsequent epitaxial silicon growth. The particularity of this layer stack is that the LPL is very thick (over 3.5 µm). This causes the HPL to grow within the LPL, as shown in Fig. 1 (a) and appears as if the layer stack consists of three different layers. This is due to the decrease of the HF concentration in the pores and at the pore tips, as the HF diffusion through the pores of the already etched layer is hindered. The detailed explanation for this behavior is beyond the scope of this paper and will be presented in another contribution. During the reorganization, pillars are formed in the HPL which are only a few hundred nanometers thin and widely spaced (over several micrometers), as can be seen in Fig. 1 (b). This leads to a detachment of the EpiWafer from the parent wafer applying only small mechanical forces. The SEM image of the sample shown in Fig. 1 (b), was prepared by ion milling and the remaining pillars of the HPL connecting both LPL sides were broken during the sample preparation so that the EpiWafer is almost detached. This highlights the robustness of this layer stack regarding the detachment after the epitaxial growth. 100% detachment yield is achieved on an area of 125×125 mm² defined with the dicing saw and over 90% on the whole wafer area of 156.7×156.7 mm².

In Fig. 3 (a) the injection level dependent minority carrier lifetime and the spatially resolved lifetime distribution of an n-type silicon sample (1 Ωcm) grown on such a porous layer stack are shown. The minority carrier lifetime at an injection level of $1 \cdot 10^{15}$ cm^{-3} is about 1.1 ms before phosphorus gettering and above 1.6 ms after phosphorus gettering. For all seven processed samples, the average minority carrier lifetime is about 800 µs before and around 1.4 ms after gettering. This is a very promising result considering the fact that the seed wafer used for the porosification was not polished but had a rough surface from standard saw damage etch in a KOH solution. The highest minority carrier lifetime in the millisecond range reported in literature is on EpiWafers grown on electrochemically etched, mirror polished monocrystalline Cz-Si wafers [4, 5].

As can be seen on the photoluminescence image in Fig. 3 (b), there are some regions with very low lifetime compared to the surrounding regions even after gettering. This indicates that the lifetime at such areas is limited by structural defects. Reducing the density of structural defects would therefore further increase the minority carrier lifetime.



(a) (b)

FIGURE 1. Cross-sectional SEM view of a sample as-etched (a) and after reorganization and epitaxy (b) of an n-type Si EpiWafer of about 40 µm thickness in this special case. The sample after the reorganization and epitaxy was prepared by ion milling. It can be seen that the remaining pillars of the HPL connecting both LPL sides were broken by the sample preparation.

It is, however, to be remarked that the residual stress in such a thick LPL as described above after reorganization will be higher than in the thinner one, leading to an increased density of structural defects such as dislocations and stacking faults during the epitaxial growth [2]. In addition, it has been observed by some authors that after reorganization, the thicker the LPL layer, the rougher the template surface, which also leads to an increase in density of structural defects [2, 8]. Reducing the LPL thickness to values around 1 µm would therefore lead to smoother template surface with reduced residual stress and hence to decreased density of structural defects and even improved minority carrier lifetimes.

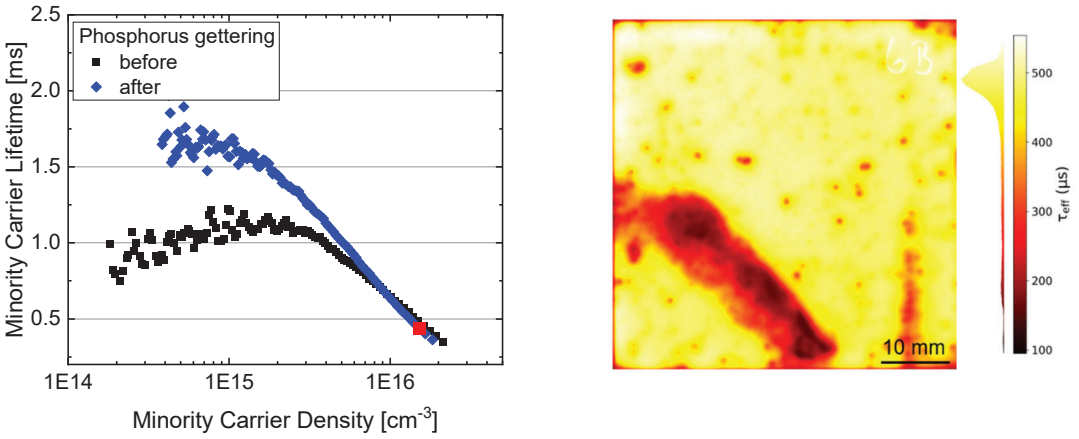


FIGURE 2. Injection level dependent minority carrier lifetime measured using PCD before (black squares) and after (blue squares) $POCl_3$ gettering in (a). In (b) the spatially resolved lifetime distribution at an average injection level of $1.5 \cdot 10^{16}$ cm^{-3} (red square in the left graph) resulting from the analysis of the photoluminescence measurement after $POCl_3$ gettering.

INCREASING THE TUNABILITY OF THE TRANSFER PROCESS

Parameters Affecting the Porosity

In the anodic electrochemical etching of silicon, the porosity depends primarily on the applied current density, the substrate doping density (resistivity) and the concentration of the hydrofluoric acid (HF) in the electrolyte. As shown in Fig. 3 (a), the porosity drops with increasing HF concentration. An increase in the HF concentration leads to a reaction rate increasing at the pore tips while decreasing at the pore walls. Therefore, the pore size decreases and the porosity drops, whereas the etch rate increases. The porosity increases with the applied current density as shown in Fig. 3, which is related to an increase of the pore size due to an increase of the electric charge flow. With increasing substrate doping concentration (lower resistivity), the porosity rises as depicted in Fig. 3 (b). This is due to a reduction of the width of the space charge region at higher doping concentrations, therefore reducing the thickness of the walls between adjacent pores.

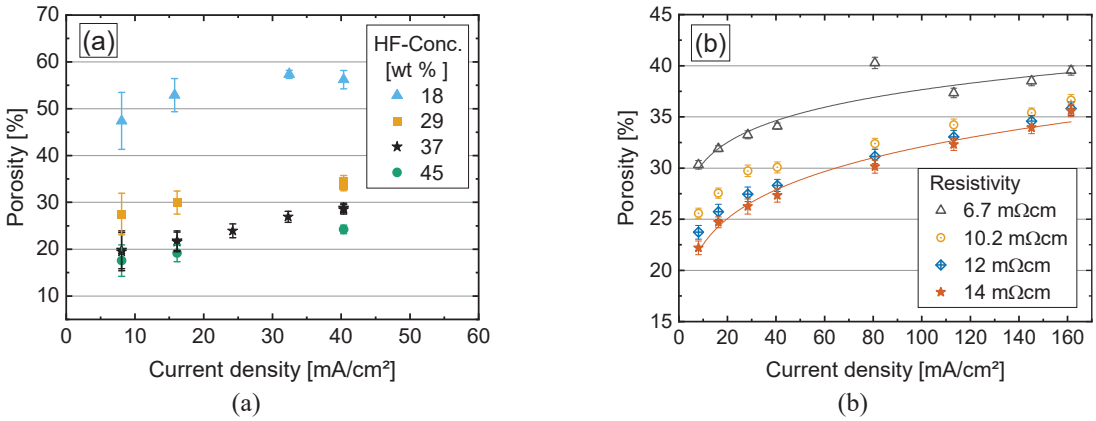


FIGURE 3. Porosity as a function of current density for different HF concentrations (a) and for various substrate doping densities (resistivity) using a 37 wt% HF electrolyte (b).

Thus, there are three possibilities to increase the porosity: Enhancing the substrate doping concentration, reducing the HF concentration in the electrolyte, and increasing the applied current density. With the applied current densities, the porosity saturates towards a maximum of about 40% for a 37 wt% HF electrolyte and the maximal applicable

current density of the used generator of 162 mA/cm² using a highly p-doped substrate of 6.7 mΩcm (see Fig. 3 (b)). This may not be high enough for a suitable detachment layer. Considering also that the minimum porosity for this substrate doping and electrolyte is about 30%, this may be too high for a suitable seed layer for epitaxy. By reducing the HF concentration in the electrolyte, one can achieve porosity values above 55% even with limited current densities (see Fig. 3 (a)) because of the higher resistive loss in the electrolyte. However, a lower HF concentration will also imply a relatively high porosity at lower current densities that may be not suitable for achieving a fully closed surface layer after the reorganization. This shows the large extension of the process window by using two different electrolytes for the different purposes of the porous layer stack. In case of an inline etching tool for porosification, two or more electrolytes can easily be integrated.

Range of Porosity and Thickness of Porous Layer Stacks Using Two Electrolytes

Fig. 4 shows spatially resolved maps of layer thicknesses and porosities of a two-layer stack consisting of LPL and HPL obtained from a fit of reflectance spectra for two samples etched either in one or in two different electrolytes. For better comparability, the LPLs of both samples were prepared under the same conditions (same electrolyte, current density and etching duration). The one-solution sample (Fig. 4 top) shows a HPL porosity mean value of 50.7%. This corresponds to a porosity difference of about 32%abs between HPL and LPL. In contrast, the two-solution sample (Fig. 4 bottom) shows a HPL porosity mean value around 59.9%, which is about 10% higher compared to the one-solution sample. For this sample, the difference between the HPL and LPL porosity is in the range of 38%abs.

Note that for the two-solution sample, the HPL was etched applying a moderate current density value of only 69 mA/cm² mainly because of generator limitations with a more resistive electrolyte. Using the same current density for the HPL as for the one-solution etching would further increase the gap between the porosity of both layers.

For the two-solution etching, the LPL porosity is slightly higher (about 3%abs) compared to the one-solution etching. This could be explained by the fact that in the diluted electrolyte during the formation of the HPL, the built-in potential of the contact between the electrolyte and silicon decreases due to the decrease of the chemical potential of the solution. Therefore, the width of the space charge region in the LPL is reduced leading to a further etching of the LPL and to an increase in its porosity.

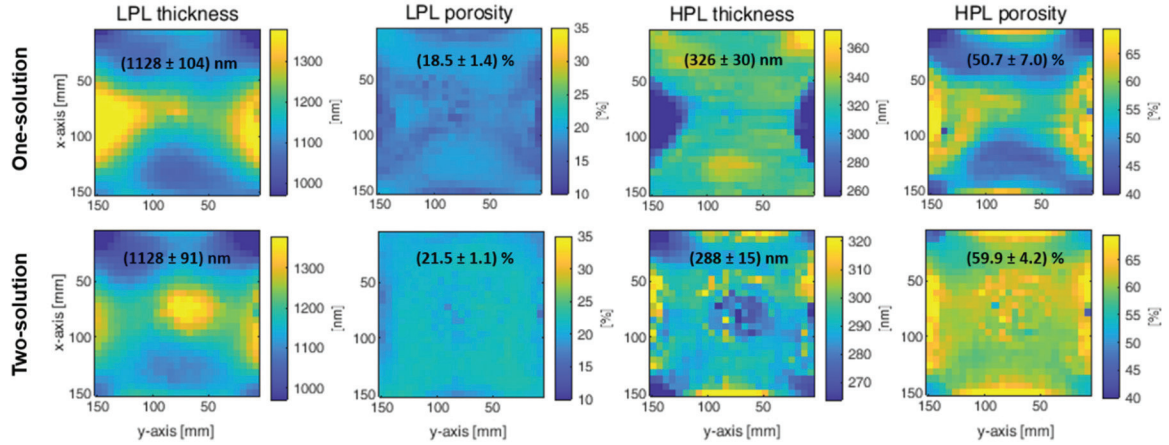


FIGURE 4. Spatially resolved maps of thickness and porosity of the low-porosity layer and the high-porosity layer. On top a sample etched with one electrolyte (HF concentration: 37.5 wt%) and bottom with two electrolytes (HF concentration: 37.5 wt% and 19.5 wt%). The LPLs of both samples were etched in the same conditions (same electrolyte, applied current and etch time). The reflectance spectra were recorded over 25×25 points. Also shown are the error-weighted mean values and the standard deviations.

Figure 5 shows porosity and thickness of LPL and HPL of a sample etched in one diluted solution with an HF concentration of 25.2 wt%. The LPL porosity rises by about 5% absolute by applying the same current density as for the LPL in the more highly concentrated solution. At the same time, the HPL porosity does not increase. This means that it is difficult to achieve the improvements described above (increasing the porosity gradient between HPL and LPL while keeping the LPL porosity as low as possible) by using a slightly diluted, but only one, solution.

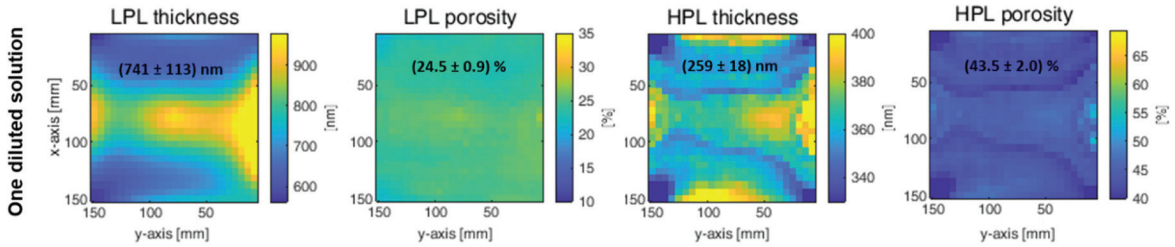


FIGURE 5. Spatially resolved maps of thickness and porosity of the low-porosity layer and the high-porosity layer of a sample etched with one electrolyte with diluted HF concentration (25.2 wt%). The LPL was etched with the same applied current density as for the samples shown in Fig. 4, but with a different duration. The reflectance spectra were recorded over 25×25 points. Also shown are the error-weighted mean values and the standard deviations.

CONCLUSION

We developed a very stable and robust layer stack regarding the detachment after the reorganization and the subsequent epitaxial silicon growth. Using this layer stack for the epitaxy leads to a detachment yield of 100% on an area of 125×125 mm² in the center of the EpiWafer. For EpiWafers grown on this template, minority carrier lifetimes up to 1.1 ms were achieved before and 1.6 ms after phosphorus gettering. This is a very promising result regarding the fact that the EpiWafer was grown on a porous Si seed layer on a KOH saw damage etched rough, but not polished wafer surface.

We demonstrated that by using two different electrolytes for the porosification of seed layer (LPL) and detachment layer (HPL), it is possible to significantly increase the porosity difference between the two layers while keeping the LPL porosity low. This represents an important extension of the process window for the reorganization and the subsequent epitaxy.

By reducing the thickness of the layer stack and increasing the porosity of the detachment layer, we expect detachable, smoother templates with lower stress that would result in a lower density of structural defects and thus even improved minority carrier lifetimes for the next runs.

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