Erschienen in: Proceedings of the 28th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC 2013) ; Paris, France ; conference 30 September - 04 October 2013. - München : WIP, 2013. - S. 937-940. - ISBN 3-936338-33-7
https://dx.doi.org/10.4229/28thEUPVSEC2013-2CO.2.6

TOWARDS 18% EFFICIENCY ON BELOW 100µM THICK MULTICRYSTALLINE SILICON WAFERS FROM THE RST PROCESS

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ABSTRACT: The RST process is a ribbon process aimed at producing low cost and very thin multicrystalline silicon wafers, with a wafer cost perspective down to 10 €-cent/Wp, provided high conversion efficiency can be reached. A general approach has been identified for the achievement of 18% conversion efficiency on solar cells made out of the RST material. This approach firstly relies on the implementation of high efficiency solar cell processes adapted to the <100 µm RST wafers. The necessary improvement of the material quality is expected through (i) the reduction of the density of SiC inclusions at the cell surface for the achievement of high FF values, and (ii) the increase of the minority carrier lifetime by both the reduction of the metallic contamination and the control of the crystalline texture of the silicon ribbon.

Keywords: Ribbon silicon, cost reduction, silicon solar cell

1 INTRODUCTION

The growth of the PV industry and the oversupply context have taken the module sale price below 60 €-cent/Wp, with perspectives below 50 €-cent/Wp in a near future. Among the different ways of improvement leading to lower module production costs, one of the most important issue is the wafer production cost, which still represents above 40% of the module cost [1]. Several technologies are presently under advanced development, which reduce the silicon consumption by avoiding kerf losses and by producing very thin wafers: proton implantation to split thin wafers from a single crystalline ingot, epitaxial growth technologies, and e.g. the RST ribbon process. To overcome the heterogeneity of the material defect density, leading to limited efficiencies on ribbon technologies [2], the manufacturing of very thin wafers with the RST process [3], based on a vertical growth of a composite Si/C/Si ribbon with a high productivity, is a promising way.

The first step of this study is the analysis of the current conversion efficiency results, to find out in which conditions, in terms of material quality and thickness, the implementation of a high efficiency solar cell process can lead to 18% conversion efficiency on <100 µm thick wafers. Two main routes are investigated to improve the material quality and the solar cell efficiency. Firstly, the FF limitation and possible improvement are investigated. The second crucial field of study is the increase of the minority carrier lifetime, through (i) the reduction of the transition metal contamination in the RST process, with the fabrication of purer carbon sacrificial template, and (ii) the optimization of the growth regime.

2 CONVERSION EFFICIENCY: OVERVIEW

The increase in maximal conversion efficiencies since the RST wafers R&D production has started in Solarforce at Bourgoin-Jallieu, France, is shown in Fig. 1. The cells are fabricated on 1–3 Ωcm, 80–140 µm thick wafers. This progress reflects the constant improvement of the quality of the RST material. With the implementation of a high efficiency cell architecture using an Al_2O_3/SiN_x stack as rear surface passivation, conversion efficiencies up to 15.5% [4] were obtained on 1–2 Ωcm, 80 µm thick wafers, exhibiting still limited QSSPC minority-carrier lifetime values below 10 µs under one sun illumination. The results also show reproducible V_{OC} values around 600 mV and J_{SC} values above 33 mA cm^{-2}. The present record efficiency of 16% was achieved with the implementation of a double layer anti-reflection coating (DARC). These results show the relevance of the passivated emitter and rear cell (PERC) concept for solar cell fabrication on the very thin multicrystalline RST wafers, mainly due to the higher reflectivity and the lower recombination velocity of the back surface.

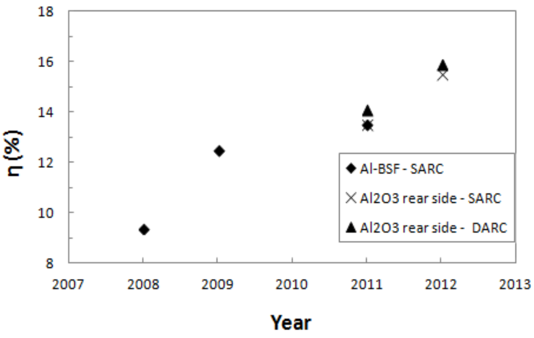

Figure 1: Best conversion efficiencies obtained on a yearly basis since the RST R&D program has started at Solarforce. Cells are fabricated on 1–3 Ωcm, 80–140 µm wafers, using an aluminum back surface field (Al-BSF) or rear side passivation with an Al_2O_3/SiN_x stack, with single (SARC) or double (DARC) anti-reflection coating.

3 18% CONVERSION EFFICIENCY WITH THE IMPLEMENTATION OF A HIGH EFFICIENCY SOLAR CELL PROCESS ON BELOW 100µM THICK WAFERS

The conversion efficiency loss due to the relatively low average minority-carrier lifetime of ribbon materials can be overcome by the use of very thin wafers for the solar cell fabrication. This requires the recombination velocity of the charge carriers on the backside to be lowered. This can be achieved with an advanced cell fabrication process based on the use of dielectric layers to passivate the surfaces (PERC architecture). This process is now mature for industrialization [5, 6].

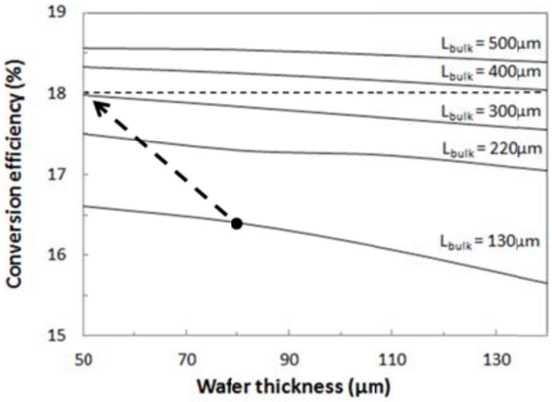

Figure 2: PC1D simulation of the conversion efficiency potential for solar cells made from RST material with an advanced solar cell process.

The results in the first paragraph confirm the pertinence of the PERC architecture for cell fabrication on very thin RST wafers. On the basis of these first promising results, PC1D simulations were performed to evaluate the conditions leading to 18% conversion efficiency. The plot in Fig. 2 shows the conversion efficiency potential as a function of the wafer thickness, for several averaged bulk diffusion length values. The reference (black dot in Fig. 2) corresponds to the potential of the present best cell (SARC), assuming the implementation of advanced emitter passivation (front surface recombination velocity is assumed to be 3000 cm s^{-1}) and a FF value of about 0.79. The 18% efficiency target is achieved for bulk diffusion lengths between 300 and 400 µm, depending on the wafer thickness. This corresponds to values 2 to 3 times larger than that of the present value in the RST material.

3 MATERIAL QUALITY IMPROVEMENT

3.1 FF improvement above 0.78

Presently, the main limitation preventing the achievement of high FF values is the presence of SiC crystals on the wafer surface, which act as shunts of the p/n junction. The correlation between the SiC crystal surface density and the obtained FF values is shown in Fig. 3. One cause of the occurrence of these crystals has been found to be the reactivity between molten silicon and local defects of the pyrocarbon coating of the carbon sacrificial template. This reactivity leads to the infiltration of molten silicon in the soft carbon ribbon, and in turn to the rapid growth of SiC dendrites on the surface of the template (Fig. 4). Some of these SiC dendrites eventually expand up to the surface of the silicon wafers. The ongoing optimization of the carbon template, and in particular of the pyrocarbon coating, has led to a huge decrease of the infiltration dots from about 500 to <10 cm^{-2}. As a consequence, a FF value of 0.778 has recently been obtained, thus pushing the potential for conversion efficiency close to 16.5%. Moreover, some recent results show an important reduction of the surface density of SiC crystals below 0.1 cm^{-2}. Thus, the demonstration of FF values above 0.78 is expected on future solar cells.

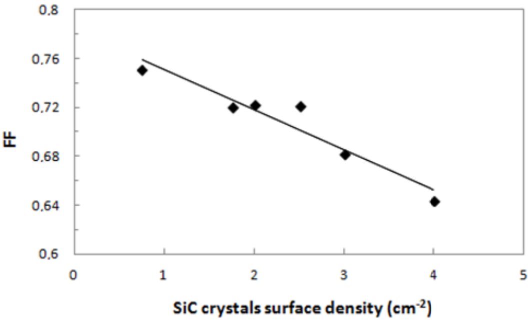

Figure 3: FF dependance on the SiC crystal surface density.

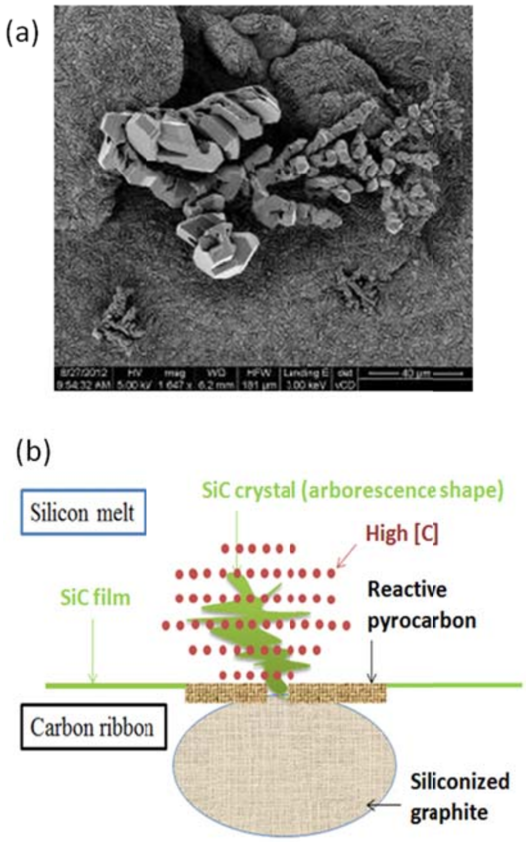

Figure 4: Top view of the RST ribbon after complete dissolution of the silicon layer in HF/HNO_3, showing the growth of SiC dendrites on the carbon template (a), and cross section representation of the Si/C interface showing the occurrence of SiC dendrites above reactive areas of the pyrocarbon coating (b).

3.2 Minority-carrier lifetime improvement

On the one hand, the reduction of the concentration of transition metals in the RST process is an important task to increase the RST-Si quality. This contamination is suspected to arise from the carbon template. SIMS profiles (Fig. 5) show examples of the concentration of transition metals in the CVD deposited pyrocarbon layer which is in contact with the silicon melt during the ribbon growth. The strong reduction of the concentration of these metals close to the surface has led to the present conversion efficiency results up to 16%. Fig. 6 shows an associated photoluminescence (PL) lifetime mapping on a 50x50 mm^2, 2 Ωcm RST wafer, after phosphorous diffusion, SiN_x:H firing, junction removal and Al_2O_3 deposition for surface passivation. The associated QSSPC lifetime value under one sun illumination is around 12 µs, which is still a limiting factor for the achievement of high conversion efficiencies. PL mapping also shows quite weak values for the best grains, below 30 µs, suggesting that impurity limitations remain.

For further improvements, the pyrocarbon deposition process is currently under optimization to obtain: (i) a stronger reduction of the concentration of detrimental transition metals at its surface, by at least one order of magnitude, and (ii) a reduction of the reactivity between the molten silicon and the pyrocarbon surface. This improvement of the carbon template quality is done together with a study of the segregation mechanisms in the RST process, to further reduce the incorporation of impurities in the ribbon and significantly enhance the minority-carrier lifetime.

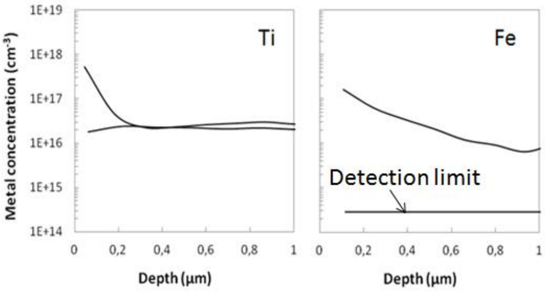

Figure 5: SIMS profile of the surface of the pyrocarbon coating of two carbon sacrificial templates, showing the decrease of the near surface contamination.

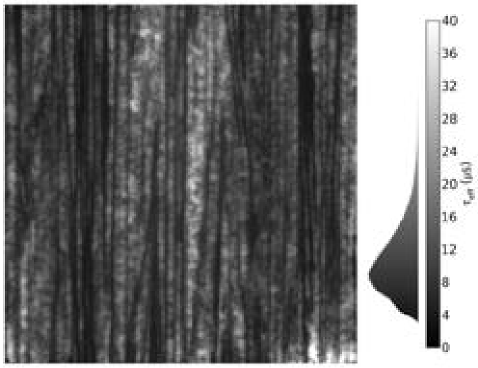

Figure 6: PL lifetime mapping ($\Delta n \approx 5\times10^{14}$ cm^{-3}) of a RST wafer after phosphorous diffusion, SiN_x:H firing, emitter removal and Al_2O_3 deposition for passivation of surfaces.

On the other hand, the growth texture of the wafers has to be optimized in order to obtain a more homogeneous quality of the material. Fig. 7 shows a picture of a Secco etched RST wafer, revealing areas with high density of structural defects, probably correlated with low lifetime regions visible in the Fig. 6. The image of Fig. 8 shows how the growth texture can be modified to reduce disorder, without significantly changing the pulling rate. This is achieved thanks to an optimization of the growth conditions and due to an improvement of the quality of the carbon sacrificial template. The reduced reactivity between the molten silicon and the carbon template leads to less disorder in the growth texture.

Figure 7: 30x30 mm^2 Secco etched sample. The grey level is correlated with the structural defect density. High disorder is visible at the center of this sample.

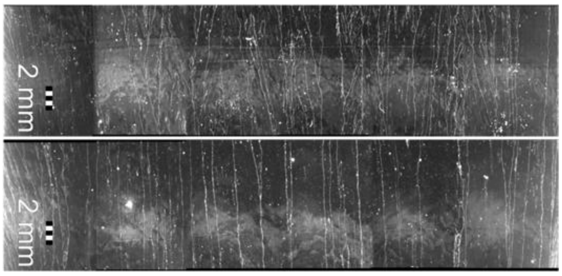

Figure 8: Optical image of the surface of as-grown RST ribbon showing the control of the crystallographic texture with adjusting pulling conditions. Pulling speed and silicon thickness remain almost constant, respectively 4.5 cm min^{-1} and between 80 and 100 µm.

Recently, a first level of optimization has led to slightly better lifetime values, above 20 µs under one sun illumination using the QSSPC technique. A PL lifetime mapping is shown Fig. 9. The lifetime values in the best grains have been raised suggesting a possible reduction of the impurity content, and the homogeneity has been slightly improved.

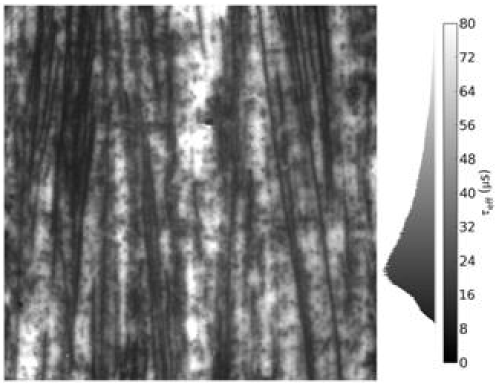

Figure 9: PL lifetime mapping ($\Delta n \approx 2\times10^{14}$ cm^{-3}) of a RST wafer after phosphorous diffusion, SiN_x:H firing, emitter removal and Al_2O_3 deposition for passivation of surfaces, after a first level of optimization.

4 A WELL SUITED PROCESS FOR THE INDUSTRIAL PRODUCTION OF ULTRA-THIN MULTICRYSTALLINE SILICON WAFERS

Fig. 2 clearly shows the interest of the production of very thin wafers in the case of limited bulk lifetime values. With the use of a carbon sacrificial template, the RST process has proven its capability to produce very flat multicrystalline silicon wafers over a wide range of thicknesses, typically between 60 and 120 µm [3]. Recently, 50x50 mm^2 wafers down to 40 µm thickness were successfully produced (Fig. 10), with a wafering yield above 50%, showing the large potential of the RST technology as a reliable process for the production of ultra-thin crystalline silicon wafers.

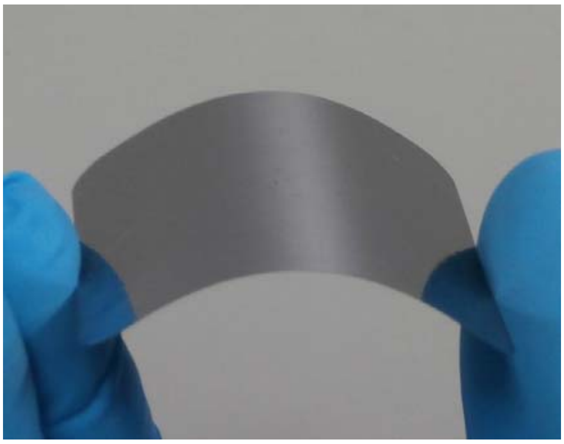

Figure 10: 40 µm thick RST wafer (50x50 mm^2) after the carbon burn-off and the etching steps.

5 CONCLUSION

The RST process is a promising technology for the production of very thin, low cost multicrystalline silicon wafers with a high productivity. In this study, wafers down to 40 µm in thickness have been produced to demonstrate the potential of the process.

High conversion efficiencies have to be obtained in order that the technology can be cost competitive, in spite of the comparatively high density of structural defects typical for ribbon technologies. The approach to reach high efficiencies is to: (i) improve continuously the RST material quality, (ii) make solar cells on thin wafers (<100 µm), and (iii) adapt a PERC solar cell structure, with an advanced back surface passivation layer, which can now be achieved on industrial equipments.

Up to now, conversion efficiencies up to 16% have been obtained on 80 µm non optimized RST wafers. On this basis, PC1D simulations have been used as a guideline to identify the path to the achievement of higher conversion efficiencies up to 18%. The necessary increase of the shunt resistance and of the bulk minority-carrier diffusion length has been evidenced. A first level of improvement has been achieved with (i) the reduction of the silicon carbide crystal surface density below 0.1 cm^{-2} and (ii) the increase of the bulk minority-carrier lifetime above 20 µs under one sun illumination. Thus, conversion efficiencies up to 17% are expected very soon.

6 ACKNOWLEDGEMENTS

This work is supported by the French government “Investment for the future” program supervised by the ADEME (DEMOS project). We would like to thank Y. Delaup, E. Benedetti and S. Kempf for the technical assistance.

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