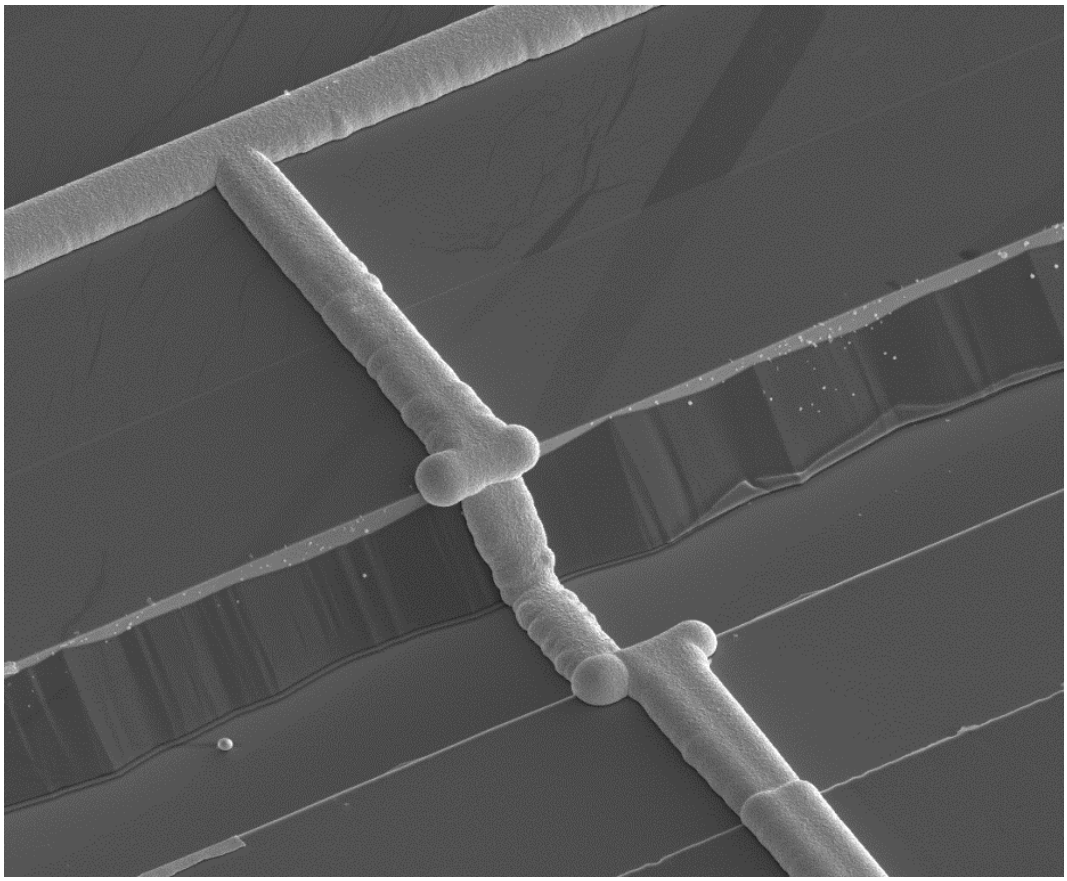
Process Development for Crystalline Silicon Thin-Film Modules with Integrated Interconnection

Regina Erika Pavlović



Cover picture: SEM picture of interconnection of two cell strips.

Process Development for Crystalline Silicon Thin-Film Modules with Integrated Interconnection

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CONTENTS

CONTENTS **3**

1 INTRODUCTION **7**

2 CRYSTALLINE SILICON THIN-FILMS **9**

2.1 RECRYSTALLIZED WAFER EQUIVALENT (REXWE) 9

2.2 POROUS SILICON LIFT-OFF 11

2.3 SUBSTRATE, INTERMEDIATE LAYER AND ATTACHMENT LAYER 13

2.4 LARGE AREA PROCESSING 13

3 THE MODULE CONCEPT **15**

3.1 ABSORBER MATERIAL 16

3.2 GENERAL PROCESSING STEPS 17

3.3 CELL STRIP WIDTH 18

3.3.1 Active module area fraction 18

3.3.2 Series resistance 19

3.3.3 Doping profile simulations 23

3.3.4 Edge effects 24

3.3.5 Optimum cell strip width 33

4 PLASMA TEXTURE **35**

4.1 TEXTURING METHODS 37

4.1.1 Wet chemical texturing 37

4.1.2 Alternative texturing methods 38

4.1.3 Plasma texturing 38

4.2 CHARACTERIZATION OF A TEXTURE 39

4.3 PLASMA TEXTURING TOOLS 42

4.4 PLASMA TEXTURING PROCESSES 43

4.4.1 Plasma texturing process at SI 600 43

4.4.2 Plasma texturing process at Plasmalab System 133 49

4.4.3 Selective plasma texturing 55

4.5 PLASMA TEXTURED SOLAR CELLS 56

4.5.1 Wafer solar cells with SI 600 texture 56

4.5.2 Thin-film solar cells with SI 600 texture 59

4.5.3 Thin-film solar cells with rear side reflector and SI 600 texture 63

4.5.4 Wafer solar cells with Plasmalab System 133 deep and shallow texture 64

4.5.5 Thin-film solar cells with Plasmalab System 133 deep and shallow texture 69
4.6 SUMMARY 72

5 SILICON STRUCTURING 75

5.1 SEPARATION OF CELL STRIPS 75
5.1.1 Laboratory realization 75
5.1.2 Industrial realization 79
5.1.3 Summary – separation of cell strips 83
5.2 EMITTER STRUCTURING 83
5.2.1 Plasma etching for emitter structuring 84
5.2.2 Summary – Emitter structuring 86

6 INTERCONNECTION 87

6.1 LABORATORY REALIZATION 87
6.1.1 Properties of SiN_x layer 88
6.1.2 Metallization 91
6.1.3 Intermediate oxide layer 95
6.1.4 Contacting metal 96
6.1.5 Summary – Laboratory realization 98
6.2 SCREEN-PRINTED INTERCONNECTION 98
6.2.1 Preparation of samples 99
6.2.2 Adhesion and isolating properties 100
6.2.3 Firing parameter optimization 101
6.2.4 Print image of fingers 104
6.2.5 Summary – Screen-printing interconnection 105

7 SOLAR CELL RESULTS 107

7.1 MODULE LAYOUT 107
7.2 THE FIRST MODULE BATCH 110
7.2.1 Effect of sintering 111
7.3 CONSECUTIVE MODULE BATCH 113
7.3.1 Effect of cell strip width 115
7.4 MODULE ENCAPSULATION 118
7.5 SUMMARY – MODULE RESULTS 120

8 SUMMARY 121

DEUTSCHE ZUSAMMENFASSUNG 125

ABBREVIATIONS.....**128**

ACKNOWLEDGEMENTS.....**130**

PUBLICATIONS.....**131**

REFERENCES.....**133**

1 INTRODUCTION

The development of renewable energy resources is vital to reduce CO_2 emissions and protect natural resources. Over the last 25 years the share of renewable energies in energy production has considerably increased. In 1990 in Germany, the share of renewables in the gross electricity generation was 3.6 % [1] with photovoltaic energy below 0.0 %. By 2013 it increased to 24.1 % with photovoltaics alone providing 4.9 % of the gross electricity generation [1]. In Figure 1.1 a more detailed illustration of the energy mix in Germany in 2014 (preliminary data) is shown and the substantial contribution of photovoltaics to electricity production is clearly visible. Increase in efficiency of solar cells and modules as well as cost reduction in the production have made this increase in photovoltaic installations possible.

Figure 1.1: Share of different technologies in gross electricity generation in Germany in 2014 (preliminary data). Left: Overall gross electricity generation mix. Right: Composition of renewable energies. Data source: [1].

The technology most widely installed is wafer based crystalline silicon photovoltaics. Research in this field is targeted at reducing costs to be competitive with other energy generation technologies. Cost reduction is possible by increase of conversion efficiency while barely increasing production cost or by reducing material or production cost without causing losses in efficiency. The development of crystalline silicon thin-film technology focuses on the second approach by reducing silicon wafer material cost. The cost of the wafers in a crystalline silicon photovoltaic module accounted for 32 % of the total module cost in January 2014 [2]. The use of thinner wafers can reduce that share, but the kerf loss during wafering remains high. Different kerf-less wafering technologies are being investigated by several research groups. The focus of this work will be on crystalline silicon thin-film on foreign substrates. Research on this topic has been

focused on the fabrication of so called wafer equivalents which could be processed as a standard wafer. The development of tools that allow the fabrication of large area thin crystalline silicon films enables concepts beyond wafer technology. In this thesis a module concept is presented which combines crystalline silicon wafer technology with the classical thin-film approach to take advantage of both concepts.

A brief introduction in crystalline silicon thin-films on foreign substrates and their fabrication is given in **Chapter 2**.

The core of this work is the integrated interconnected crystalline silicon thin-film module (iSiMo) concept which is presented in **Chapter 3** along with necessary processing steps and considerations about the module design. A more detailed description of the relevant processing steps and their developments are given in the following chapters.

Chapter 4 describes the development of plasma texturing processes for crystalline silicon thin-film solar cells. As illustrated in this section, light-trapping is crucial for every crystalline silicon thin-film concept. The plasma texture was not applied to iSiMo modules, but to wafer and thin-film cells, whose results are also included.

Silicon structuring is required for defining the cells in the module and for emitter structuring. **Chapter 5** introduces the processes used for mini-module fabrication as well as industrially feasible options using lasers for these processing steps.

The metallization, which includes the interconnection of the cells, is discussed in **Chapter 6**. Again, two approaches are presented: The laboratory realization using photolithography and evaporated contacts as well as the industrial realization via screen-printing.

Results of the fabricated mini-modules are shown in **Chapter 7**. Effects of sintering and cell strip width on cell performance are reviewed and results of encapsulated mini-modules presented.

A summary of the work is given in **Chapter 8**.

2 CRYSTALLINE SILICON THIN-FILMS

A short introduction into crystalline silicon thin-film concepts will be given in this chapter. Focusing on concepts on foreign substrates, the fabrication of recrystallized wafer equivalent and porous silicon lift-off foils will be presented.

The crystalline silicon thin-film (c-Si TF) concepts discussed here use chemical vapor deposition (CVD) for silicon deposition [3-5]. In order to obtain multi or mono crystalline silicon a crystalline seed layer is needed. A crystalline silicon substrate, which cannot be directly used for solar cell production due to impurities, provides such a seed layer. The active high-purity silicon layer is grown epitaxially on the silicon wafer to generate a so called epitaxial wafer equivalent (EpiWE) [3-5]. Here, the substrate provides not only a crystalline template for the epitaxial growth but also mechanical stability and conductivity and the EpiWE can also be processed to a solar cell as a conventional silicon wafer. In order to reduce not only high-purity but also overall silicon consumption, a foreign substrate can be used [6]. Different materials are possible as substrates, depending on the concept for the seed layer. Two concepts for the fabrication of thin films on foreign substrates will be introduced, the recrystallized wafer equivalent (RexWE) and the porous silicon lift-off approach.

2.1 Recrystallized wafer equivalent (RexWE)

In Figure 2.1 a schematic of the RexWE can be seen. A detailed description of the RexWE can be found in [6-10], in the following a short introduction of the fabrication processes will be given.

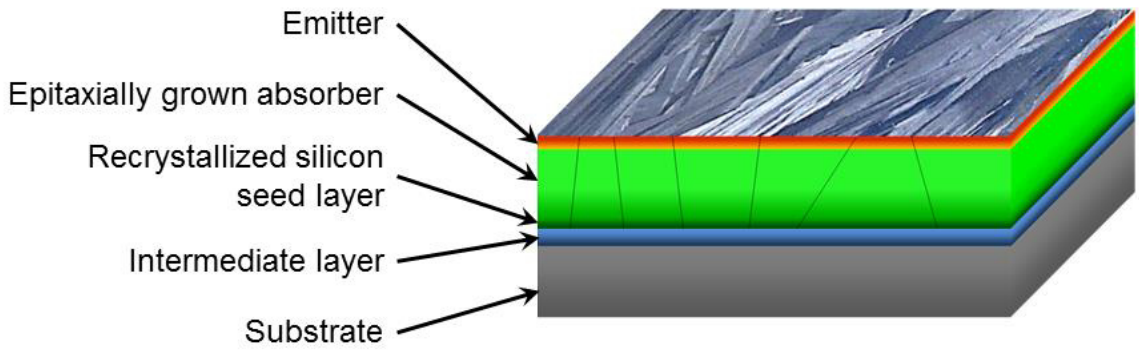

Figure 2.1: Schematic of a recrystallized wafer equivalent.

In the RexWE approach a 3 to 10 µm thick silicon layer is deposited by atmospheric pressure CVD (APCVD) on a foreign substrate with an intermediate layer. The intermediate layer is introduced as a diffusion barrier to prevent impurities from leaving the substrate and if necessary seal pores of the substrate. This layer can for example consist of plasma enhanced chemical vapour deposited (PECVD) amorphous SiO_x or SiC [7, 8], microcrystalline APCVD SiC [9] or a combination thereof. As the intermediate layer does not provide a crystal structure to epitaxially grow silicon, the thin, deposited silicon film is microcrystalline. To generate larger crystal sizes in the millimeter to centimeter range, a zone melting recrystallization (ZMR) step is added, with the antecedent application of a SiO_x capping layer on the silicon film to prevent the formation of silicon droplets during the process. In the process, the sample is mounted in a rectangular quartz tube around which a moveable optically heated furnace is arrayed, which heats the sample close to the melting point of silicon. A focused melting lamp is located above the sample to melt the silicon film in one line across the sample and silicon crystals grow out of the melt zone. The melt zone is scanned across the sample by moving the furnace and the silicon layer is recrystallized forming grains of several millimeters in width and several centimeters in length. A picture and schematical drawing of the ZMR tool are displayed in Figure 2.2.

Typically the recrystallized seed layer is highly doped so it may later form the back surface field (BSF) of the solar cell while the absorber layer is grown epitaxially by CVD onto the seed layer. The resulting RexWE can be processed into a solar cell using standard wafer technologies.

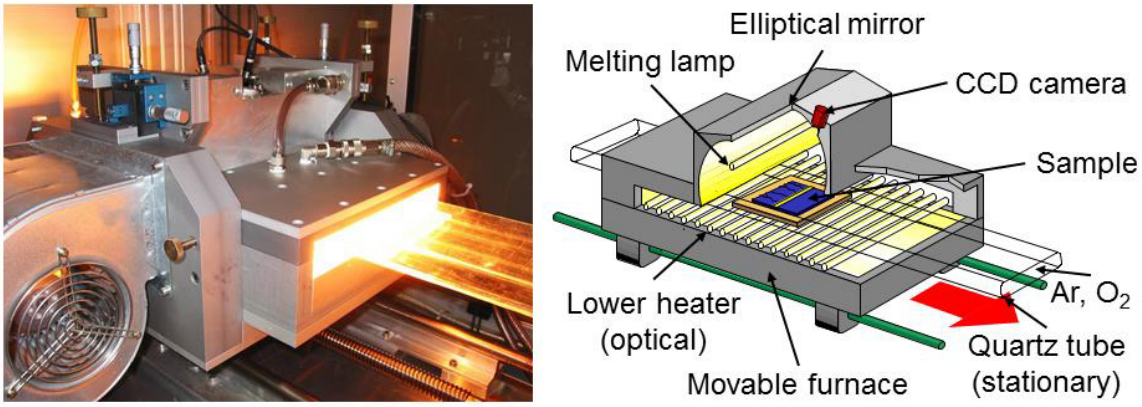

Figure 2.2: Picture and schematical drawing of the laboratory type ZMR tool used to recrystallize the seed layer in RexWE process [9].

2.2 Porous silicon lift-off

The porous silicon (PorSi) lift-off approach has been investigated by several research groups in recent years. For example, a review of different lift-off technologies can be found in [11] and information about the porous silicon lift-off process for solar cell application in [12-14]. An introduction to the PorSi approach using electro-chemical etching is given below.

Two porous layers are formed in an electro-chemical etching process in a monocrystalline silicon wafer. A low porosity layer sits on top of a high porosity layer, which is the weak layer that allows for the lift-off. Two approaches are possible and shown in Figure 2.3: Lift-off after reorganization or lift-off before reorganization.

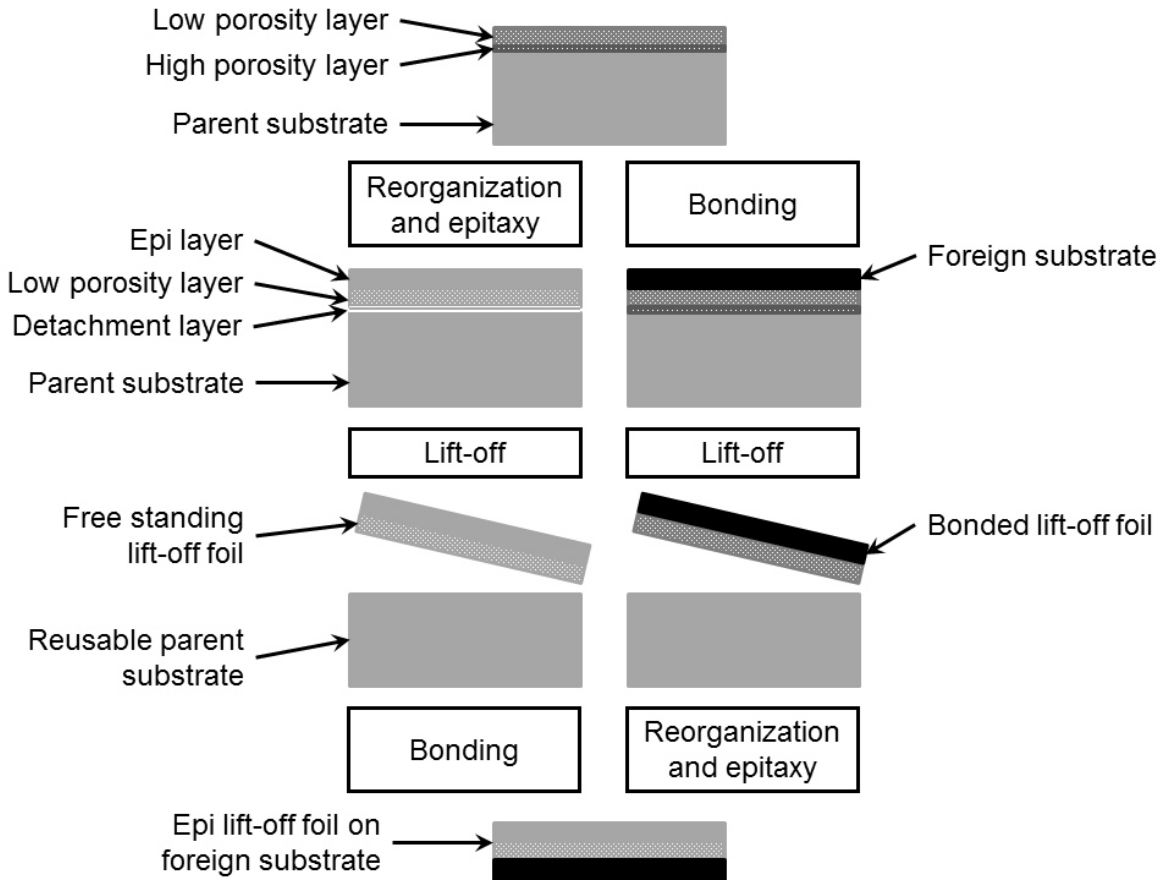

Figure 2.3: Schematic of porous silicon lift-off approach. After porosification the double porous layer is either reorganized and epitaxially thickened and then lifted off and bonded on a foreign substrate (left route) or a foreign substrate is bonded to the porous layer and it is lifted off prior to reorganization and epitaxy (right route).

In the first case, the wafer with double porous layer is reorganized at temperatures up to 1100 °C [12] in hydrogen ambient. During the reorganization, the structure of the porous layers changes, forming pores with diameters of tens to hundreds of nanometers in the low porosity layer. The high porosity layer forms a weak layer where only pillars remain as bond between parent wafer and low porosity layer. The pores on the surface of the low porosity layer close to form a thin silicon layer, which is the template for the following epitaxy process usually done in the same reactor as the reorganization. Figure 2.4 shows a porous silicon double layer after reorganization and epitaxial thickening. The stack is still attached to the parent substrate.

Following epitaxy, the foil can be lifted off and processed further free-standing or bonded onto a foreign substrate. The layer can also be processed further on the parent substrate, and lifted after processing of one side is finished [15]. For lift-off before reorganization the porosification parameters need to be adjusted to form a high porosity layer that is weak enough for lift-off already after etching. The low porosity layer is then bonded to a foreign substrate on which the film is reorganized and epitaxially thickened. The resulting lift-off wafer equivalent can be processed into a solar cell. Lift-off before reorganization was to my knowledge not yet performed on large areas. In the EU project “Roll to Module processed crystalline Silicon Thin-Films” (R2M-Si) [16] it could be demonstrated on areas in the square centimeter range at Fraunhofer ISE.

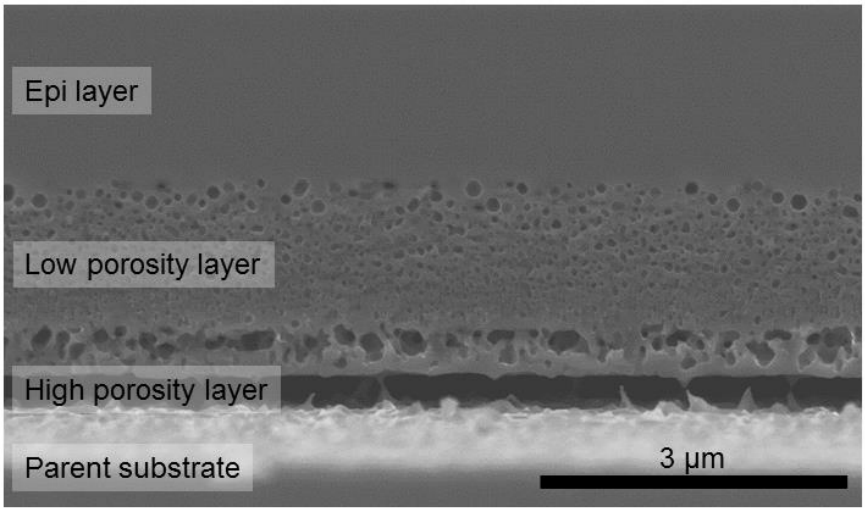

Figure 2.4: Reorganized and epitaxially thickened porous silicon layer stack on parent substrate.

2.3 Substrate, intermediate layer and attachment layer

The RexWE approach and the PorSi lift-off concept have various requirements for the substrate as well as the intermediate layer and, in the case of PorSi lift-off foils, the attachment layer. Additionally, the applied cell and module concepts can require a highly conductive or isolating substrate. Independent of the technical requirements, the substrate, attachment method and material all have to be cost-effective. PorSi lift-off foils that are lifted off after reorganization, epitaxial thickening and solar cell processing of one side are often bonded to glass substrates using glues that cannot withstand high temperatures as e.g. silicone [17]. For PorSi foils with detachment prior to reorganization and RexWE, a high temperature stable substrate is needed, up to approximately 1200 °C and at above 1400 °C, respectively. It is also crucial that no harmful contaminants diffuse out of the substrate and into the active silicon layer during any of the processing steps. Ceramics are a promising option for the high-temperature approach. In order to close pores and trap contaminants inside the substrate, encapsulation with silicon carbide is possible [18].

2.4 Large area processing

High-throughput tools for large areas are needed to industrialize the RexWE and lift-off concepts. At Fraunhofer ISE inline tools for the fabrication of crystalline silicon thin films are being developed.

For zone melting recrystallization the ZMR400con was built [19], which functions similarly to the laboratory type ZMR tool. The furnace is stationary and the samples are transported through the reactor on 410 mm wide quartz carriers that allow samples of up to 400 mm width.

For silicon growth, the ConCVD and ProConCVD were developed [20]. Both tools work in inline configuration and samples are processed upright in carriers. In the ProConCVD three 156 x 156 mm² wafers can be loaded vertically into a carrier and the tool has three tracks of deposition chambers which can not only be used to deposit silicon, but also silicon carbide. It would also be possible to not just use wafers of 156 x 156 mm² in a carrier, but directly processa large area substrate on which silicon is deposited.

A little bit more future-oriented is the idea of an inline porosification and lift-off process, which was investigated in the EU project “Roll to Module processed crystalline Silicon Thin-Films” (R2M-Si) [16].

In order to use the potential of large area crystalline silicon thin-films an efficient module interconnection is required. One approach is the iSiMo (integrated interconnected crystalline silicon thin-film module) which will be introduced in the next chapter.

3 THE MODULE CONCEPT

A concept for integrated interconnection of crystalline silicon thin-film modules is introduced in the following chapter. The general idea of the module concept as well as the necessary processing steps are presented in this chapter. The focus lies on the detailed design such as cell strip width, the doping profile of the silicon layer and their effects on the module performance.

The iSiMo concept aims to combine a thin-film approach with crystalline silicon wafer processing technology and was patented by Fraunhofer ISE [21]. Thin crystalline silicon films are separated into individual cell strips and interconnected directly on the substrate. Metallization and interconnection are done in one processing step leading to a soldering free interconnection which simplifies the production process of the module. A module schematic using screen-printed contacts can be seen in Figure 3.1. Another advantage of the module concept is the adjustability of cell areas in order to set the optimal current to voltage ratio. Using serially interconnected cells with small areas a solar module with comparatively high voltage and low current can be designed, which reduces series resistance losses.

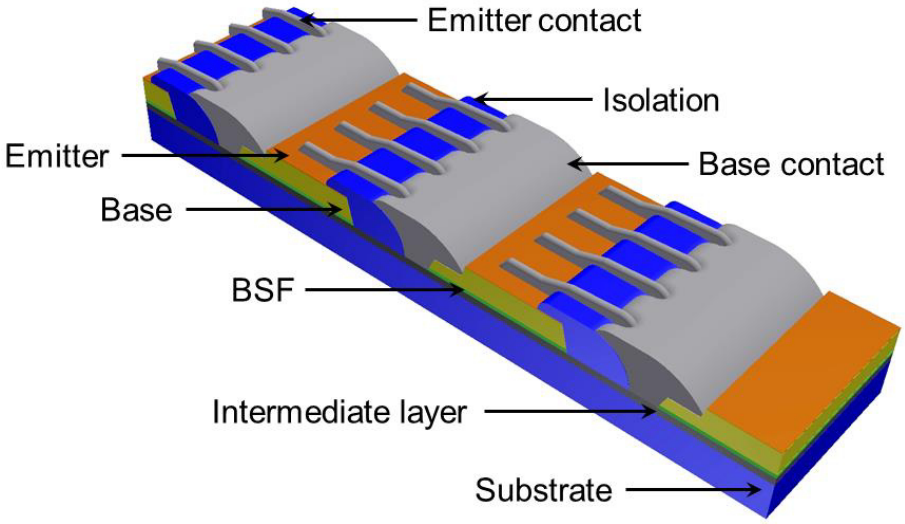

Figure 3.1: Detail of integrated interconnected module scheme. Not to scale.

Different interconnection concepts for crystalline silicon thin-film solar cells have been developed by various groups and several will be presented below. For all concepts, the thin film is – as in the iSiMo concept – divided into cell strips which are then interconnected serially. Green et al. [22] presented a device structure for crystalline silicon on glass in 2004, which was used in industrial pilot production at CSG Solar. Fabricating the polycrystalline silicon on glass, a superstrate configuration was used with interdigitated contacts on the rear. Also using poly-crystalline silicon and interdigitated contacts, Gordon et al. [23] proposed an interconnection scheme in 2006. In that case, the thin film is created using aluminium-induced crystallization and subsequent high-temperature epitaxial thickening, which means that glass cannot be used as a substrate and the contacts lie on the front side. Terheiden et al. [24] published a module concept for monocrystalline silicon thin-films (c-Si TF) in 2006. The monocrystalline silicon thin-film was created by the porous silicon layer transfer process to form a seed layer which was epitaxially thickened. A bifacial module was built as the cell was glued to a glass substrate after the high-temperature steps and then detached from the mother wafer. In [25] Rentsch et al. presented a screen-printed concept with interdigitated front contacts for c-Si TF modules. In this case the multicrystalline silicon film is formed by ZMR and subsequent epitaxial thickening.

In the iSiMo concept, the contacts lie on the front side, as the rear side is not accessible. The main difference to previous concepts is that no interdigitated metallization is used, but a base contact on one side of the cell parallel to the trench is applied to minimize shading losses and simplify the alignment.

In this chapter the structure of the module will be discussed. This includes cell strip width, metallization layout and doping concentration of the thin-film layer as well as the general processing steps.

3.1 Absorber material

The integrated interconnected module concept was originally developed for recrystallized silicon films, but in principle it is transferrable to other crystalline silicon thin-film technologies e.g. lift-off films. For the mini-modules processed in the frame of this thesis, silicon on insulator (SOI) wafers were used to evaluate the processing steps and structure. Possible issues of the material including detachment of foils or steps and edges in a recrystallized and epitaxial thickened

layer were avoided by using SOI wafers. These wafers have a 1.5 µm thick silicon seed layer on a 1 µm thick SiO_2 insulating layer and the BSF and base are epitaxially grown by CVD on the seed layer.

3.2 General processing steps

The processing steps necessary to fabricate integrated interconnected modules can be undertaken in various ways. A detailed description of the individual steps can be found in the following chapters while this section will give an overview of the processing sequence.

In order to establish a reliable process in which the cell structure could be investigated, a laboratory process was developed with photolithographic structuring processes on small areas for epitaxially grown thin films on SOI wafers. Additionally, processes for industrial applications were investigated that could be applied to recrystallized or lift-off films on foreign substrates. Techniques such as lasering for structuring and screen-printing for metallization were tested.

The process is schematically depicted in Figure 3.2 and starts with the active layer stack of BSF, base and if desired an epitaxially grown emitter on the substrate. First the cell strips need to be separated and the emitter applied and structured, or in the case of the epitaxial emitter only structured. It would also be possible to use a diffusion barrier to generate a structured emitter directly as well as implement a selective emitter. The structured emitter leaves an open pn-junction next to the trench which the metallization has to cross; therefore an isolating layer has to be applied to prevent shorting of the cells. The last step is the metallization which is also the interconnection. Isolating layer and metallization material and technique have to match as not all isolating layers are suitable in every case. A texture is not necessary for the interconnection but can easily be implemented in the process to enhance the efficiency. Depending on the detailed processing sequence and used steps, texturing would be implemented at different stages.

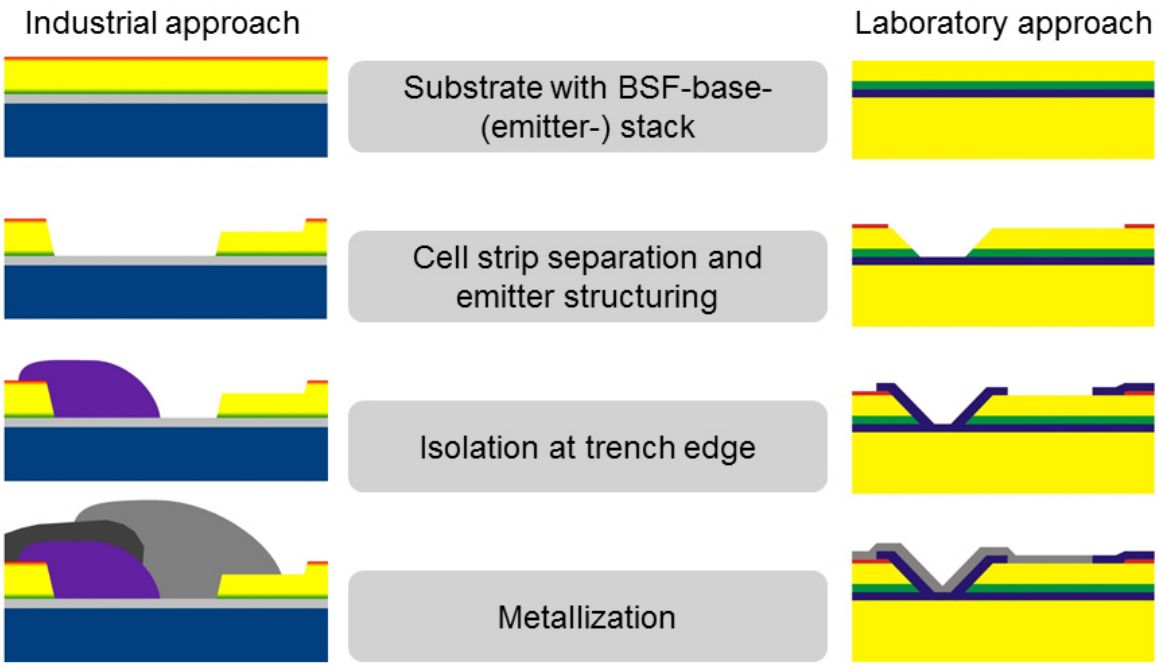

Figure 3.2: General processing steps of integrated interconnected module concept (not to scale). On the left the industrial approach on ceramic substrate with screen-printing metallization and the laboratory approach on SOI wafers on the right.

3.3 Cell strip width

The contacting of the base on only one side without metal on the rear leaves the silicon and especially the BSF to provide sufficient lateral conductivity. The BSF thickness and doping concentration mainly define the lateral conductivity which in turn plays a major role for the series resistance. Another factor for the series resistance is the cell strip width: With increasing cell strip width, the series resistance also increases which in turn leads to a reduction in fill factor. The cell strip width is also a dominant factor for the active module area. As the trench between the cells is independent of the cell strip width, it proportionally takes up more space with decreasing cell width and the active module area decreases. Additionally narrower cell strips exhibit a higher edge to area ratio which might have a negative effect. To achieve high module efficiencies, the cell strip width needs to be optimized while taking all these effects into account.

3.3.1 Active module area fraction

The active module area in this concept equals the module area reduced by the gap between the individual cell strips. Shading losses and the module frame were not taken into account for the following calculations. In Figure 3.3 the active

module area fraction is plotted against cell strip width for different gap widths. As one would expect, the influence of the gap width is high for narrow cell strips and decreases with increasing cell strip width. The achievable gap width for an industrial feasible screen-printed interconnection was estimated to be 200 to 300 µm, due to width of the contacts and necessary safety margins. For the laboratory process a gap width of approx. 120 µm was reached.

Considering the active module area with a 100 µm gap, it is already larger than 90 % at 1 mm cell strip width and increases to 99 % at 10 mm cell strip width. For larger gap sizes it drops heavily, especially at small cell widths. At a cell strip width of 3 mm the active module area is larger than 90 % for gap widths up to 300 µm. As these gap widths are in the achievable range with industrial processes, the minimum cell strip width is considered 3 mm.

3.3.2 Series resistance

The series resistance (R_{tot}) of one cell of the integrated interconnected module can be estimated by accumulating the respective resistance contributions of the cell as described in [26]. In the evaluated structure the following could be identified (see Figure 3.4): BSF and base resistance (R_1), resistance in the emitter (R_2), contact resistance of emitter contact (R_3), resistance in the metallization (R_4), contact resistance of base contact (R_5) and the resistance of the BSF along the width of the cell (R_6).

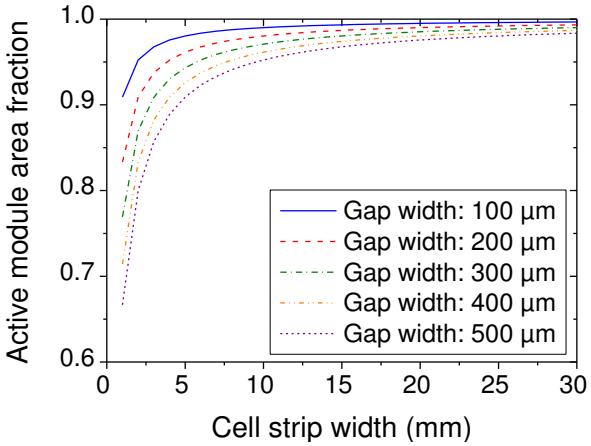

Figure 3.3: Active module area fraction in dependence of cell strip width for different gap sizes.

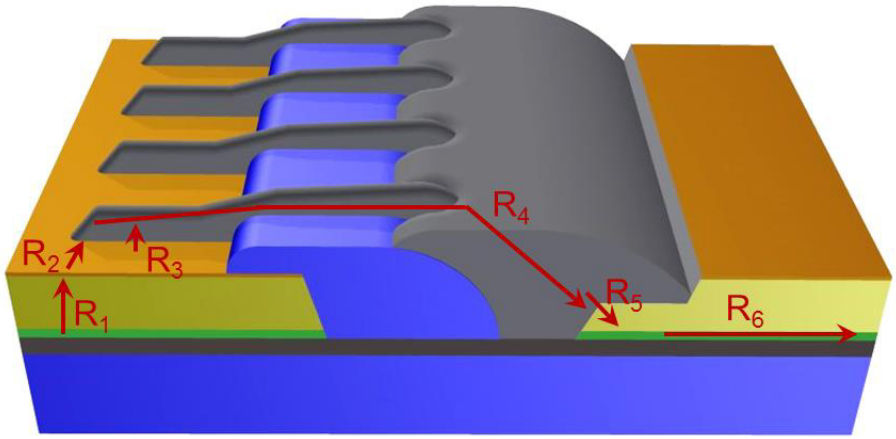

Figure 3.4: Schematic of interconnection (not to scale) with respective resistance contributions.

According to [26], these resistances can be calculated from equation (3.1) to (3.6):

$$R_1 = (\rho_{base} \cdot d_{base}) + (\rho_{BSF} \cdot d_{BSF}) \quad (3.1)$$

$$R_2 = \frac{1}{6} \cdot R_{ShEm} \frac{x_d - x_w}{x_l} \quad (3.2)$$

$$R_3 = \frac{\sqrt{\rho_{cEm} \cdot R_{ShEm}}}{W} \cdot \coth\left(x_w \sqrt{\frac{R_{ShEm}}{\rho_{cEm}}}\right) \quad (3.3)$$

$$R_4 = \frac{1}{3} \rho_M \frac{x_{ltot}}{x_w \cdot x_h} \quad (3.4)$$

$$R_5 = \frac{\sqrt{\rho_{cBSF} \cdot R_{ShBSF}}}{x_d/_2} \cdot \coth\left(\frac{x_d}{2} \sqrt{\frac{R_{ShBSF}}{\rho_{cBSF}}}\right) \quad (3.5)$$

$$R_6 = \frac{1}{6} \cdot \frac{R_{ShBSF} \cdot W}{x_d} \quad (3.6)$$

With $\rho_{base/BSF/M}$ the resistivity of base, BSF and metallization respectively in Ωcm, $\rho_{cEm/cBSF}$ the contact resistivity between contact and BSF or emitter in Ωcm² and $R_{ShEm/ShBSF}$ the sheet resistance of emitter and BSF in Ω/□. Thickness of BSF and base are notated $d_{base/BSF}$ and finger distance, width, length and height are $x_{d/w/l/h}$ while x_{ltot} is the total metallization length and W the cell strip width. If two different metals are used for contacting p- and n-type silicon equation (3.4) has to be adapted to include the resistance for each metal with the respective conductivity and the contact resistance between the metals.

The finger distance was set using GridSim [27], a tool used to calculate the optimum finger spacing for H-pattern solar cells [28]. Even though the intended cell structure is very different from a H-pattern structure, an estimation for an adequate finger distance could be found with 1.5 mm.

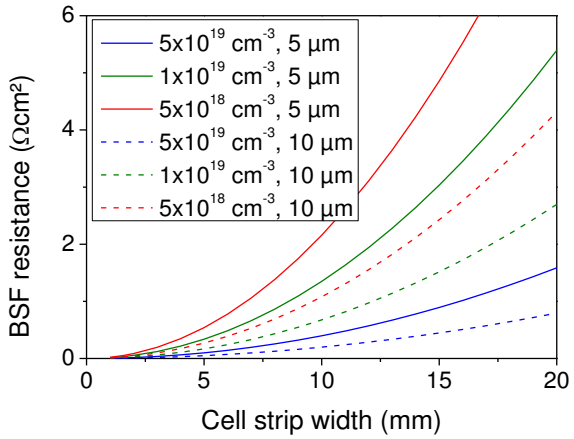

Figure 3.5: BSF resistance for different doping concentrations and thicknesses dependent on cell strip width.

Especially for broadening cell strip width, the series resistance is influenced strongly by the conductivity of the BSF. Varying its thickness and doping concentration has a significant impact on the series resistance contribution of the BSF (R_6). In Figure 3.5 the BSF resistance R_6 is shown for different doping concentrations and thicknesses assuming a finger distance of 1.5 mm. The steep increase of BSF resistance with increasing cell strip width can clearly be seen for a 5 µm thick BSF with doping concentration of $5 \cdot 10^{18}$ - $1 \cdot 10^{19}$ cm^{-3}. A thicker BSF can reduce the resistance considerably as well as a higher doping concentration. As a high doping concentration (> $1 \cdot 10^{19}$ cm^{-3}) increases auger recombination as well as free carrier absorption an optimum needs to be found. The optimum doping profile of the active silicon layer will be discussed in section 3.3.3.

The total series resistance R_{tot} was estimated using equations (3.1) – (3.6) with a BSF of 5 µm thickness and a doping concentration of $5 \cdot 10^{18}$ cm^{-3} using a 30 µm thick absorber with a conductivity of 0.5 Ωcm. The finger spacing was set to 1.5 mm and the finger widths of base and emitter contacts were set equal to each other. Screen-printing and evaporated contacts were assumed as metallization, taking into account the differing geometries of the contacts and therefore assuming a width of 80 µm for screen-printed and 30 µm for evaporated contacts. For the screen-printing metallization the formation of an Al-BSF under the aluminum base contact was assumed and the contact resistance between two different metal pastes was not taken into account.

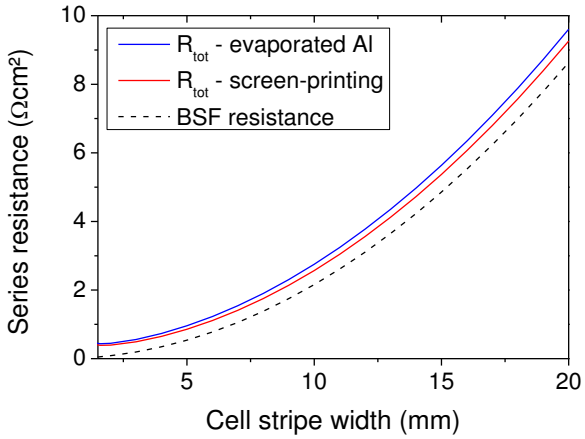

Figure 3.6: Total series resistance estimated dependent on cell strip width for screen-printing metallization and evaporated aluminum metallization. The BSF resistance is indicated by the dashed line.

The cell strip width was varied between 1.5 and 20 mm. As the finger distance was set to 1.5 mm, a cell strip width equal or smaller than 1.5 mm would not require any fingers perpendicular to the base contact (parallel to the trench). In this case a different metallization geometry would be used; contacting the emitter on one side and the base on the other side of the cell, similar to [29]. The calculated total series resistance R_{tot} is displayed in Figure 3.6 in dependence of cell strip width. The series resistance was estimated for the two different metallization concepts: Screen-printing metallization and evaporated aluminum. Additionally the BSF resistance is indicated by the dashed line. It can be seen that the BSF resistance is the determining factor for the series resistance dependence on cell strip width. In case of evaporated aluminum contacts, the series resistance increases slightly more with wider cell stripes than screen-printed contacts. This effect originates in an increase in base contact resistivity. The widths of base and emitter fingers were set equal and relatively narrow fingers were assumed for evaporated contacts. The base contact area should be increased with increasing cell strip width to account for the larger cell area and in turn higher generated current.

For a cell strip width of 10 mm the series resistance is already higher than 2 Ωcm², which is most likely already too high to achieve an acceptable fill factor and high efficiency. The cell strip width should therefore be not higher than 10 mm.

3.3.3 Doping profile simulations

In the frame of the EU project R2M-Si [16], simulations were done to determine the best suited doping profile for the given cell structure [30]. All the simulations shown in this section were done by the photovoltaic division of the University of Constance by G. Micard. The results are included in this work as the simulated cell concept matches, with some limitations, the structure of the mini-modules fabricated in the frame of this thesis.

The optical simulation to obtain the generation profile was conducted with SUNRAYS [31]. Excellent light-trapping was ensured by a pyramidal texture on the front side combined with a reflective rear side. Assuming optimal surface passivation and a selective emitter the 40 µm thick cell was simulated using Synopsys Sentaurus 3D. The finger distance was fixed at 1.5 mm, the finger width at 30 µm and the trench gap was 120 µm. Other parameters concerning geometry were set as well to the ones used in the fabricated mini-modules (see chapter 7). The cell strip width was set to 3, 5 and 10 mm, as discussed before. Due to high losses in the case of 10 mm wide cells simulation problems occurred and the largest cell width that was simulated is therefore 8 mm. The simulation results can be found in Table 3.1. The doping profile is the same for all cell strip widths. The optimum BSF thickness is 29 µm, but the difference between 15 and 30 µm negligible. The thick, medium doped ($1 \cdot 10^{18}$ cm^{-3}) BSF provides sufficient lateral conductivity without significant increase in Auger recombination due to high doping concentration.

For the IV parameters, V_{OC} is not dependent on the cell strip width as all surfaces are assumed to be optimally passivated. J_{SC} increases with increasing cell strip width, due to decreased shadowing. The increase in series resistance with widening of the cell strips can be seen in the reduced fill factor by 4.1 % abs. from cell strip widths of 3 to 5 mm and an additional 11.3 % abs. to 8 mm cell strips. The resulting efficiency drop is relatively small (0.4 % abs.) from 3 to 5 mm cell strips, but with 2.3 % abs. high from 5 to 8 mm. It is therefore expected, that mini-modules with 10 mm cell strips will not perform as well as with 5 mm or smaller.

Table 3.1: Simulation results for cell strip widths of 3, 5 and 8 mm from [30].

Cell strip width	**3 mm**	**5 mm**	**8 mm**
Base doping (cm^{-3})		$3 \cdot 10^{16}$	
BSF doping (cm^{-3})		$1 \cdot 10^{18}$	
BSF thickness (µm)		29 (15-30)	
V_{OC} (mV)	672	672	672
J_{SC} (mA/cm^2)	34.1	35.0	35.8
FF (%)	80.9	76.8	65.5
η (%)	18.5	18.1	15.8

3.3.4 Edge effects

Lifetime samples were processed to evaluate the effect of cell strip width on effective carrier lifetime as a reduced effective lifetime can limit the V_{OC} of a cell. The processing sequence for the samples can be found in Figure 3.7. On 4 inch float zone wafers with 10 Ωcm four areas were defined with differing density of trenches. Trench distances of 1, 3, 5 and 10 mm were used. The trenches were created by KOH etch using SiO_2 as mask (for details see section 5.1.1). The 10 µm wide opening lines in the SiO_2 layer resulted in 20 µm wide trenches after 60 min KOH etching. The $POCl_3$ diffusion formed a 40 Ω/□ emitter on the front side (FS), but no emitter on the rear side (RS) due to the SiO_2 layer acting as diffusion barrier. The RS SiO_2 was removed together with the phosphorus silicate glass (PSG) after emitter diffusion. The emitter was structured by plasma etching using photoresist as mask (as described in section 5.2.1). A band of 310 µm width aligned symmetrically around the trench was etched, as can be seen in Figure 3.8 schematically and in the SEM pictures in Figure 3.9. As photolithography masks, plastic sheets were used on which the structure was plotted. The resolution of these photoplots is not as high as for conventional photolithography masks, but sufficient for this experiment. A side effect of the use of the sheet-masks is the forming of frayed edges, as can been seen in Figure 3.9 on the right.

The samples were passivated by a 70 nm thick silicon nitride (SiN_x) deposited by plasma enhanced chemical vapor deposition (PECVD) on both sides (see section 6.1.1).

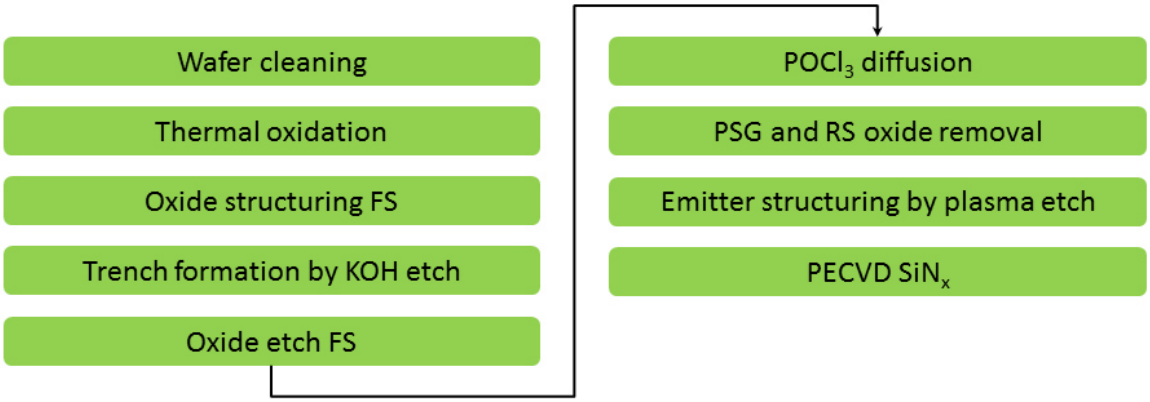

Figure 3.7: Processing sequence for lifetime samples to investigate influence of cell strip width on surface recombination velocity.

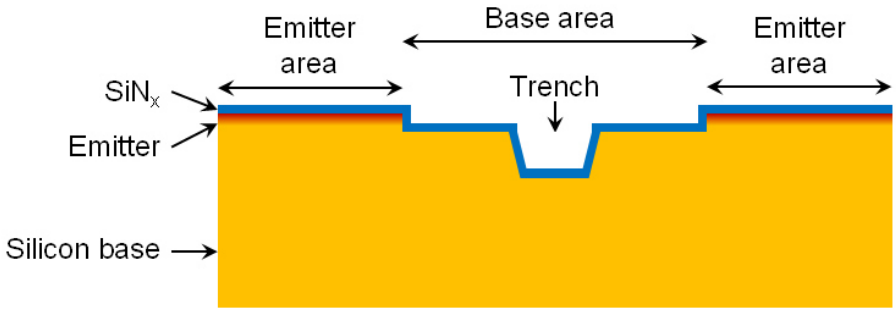

Figure 3.8: Trench structure of the samples used to determine the influence of the trench density on the effective carrier lifetime.

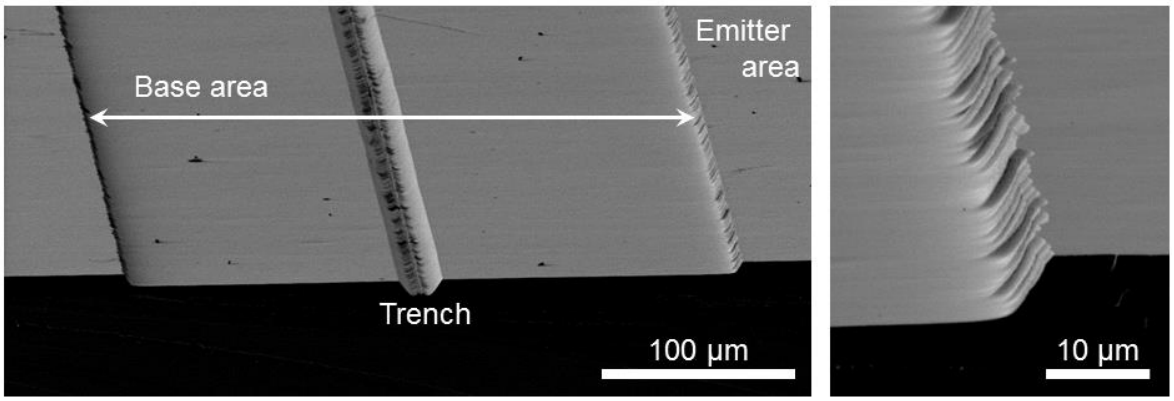

Figure 3.9: SEM pictures of a structured sample. The base area around the trench is clearly visible. Right: A close up of the step defining the base area.

The effective lifetime of the samples was measured by microwave photoconductance decay (µPCD). The effective lifetime τ_{eff} is composed of the bulk lifetime τ_b and the surface lifetime τ_s:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s}$$

An approximate solution for τ_s is

$$\frac{1}{\tau_s} = \left[\frac{W}{2S} + \frac{1}{D}\left(\frac{W}{\pi}\right)^2\right]^{-1}$$

where *S* is the surface recombination velocity, *W* the wafer thickness and *D* is the diffusivity. An overview about carrier lifetime, surface recombination and diffusion length can for example be found in [32].

A map of the effective carrier lifetime of a sample before the application of the passivating SiN_x layer can be seen in Figure 3.10. The influence of the structuring can clearly be seen. The horizontal line in the middle of the sample with very low lifetime is the base area, where the emitter was removed. As would be expected, the emitter areas have a higher effective lifetime τ_{eff} than the base areas due to the passivating effect of the emitter, which reduces the surface recombination velocity *S* and therefore enhances the surface lifetime τ_s. Strikingly, the influence of the base area is about 2 mm wide and therefore exceeds its actual width (310 µm) by far, which is due to lateral diffusion of minority carriers in the sample. The minority carrier diffusion length L_{Diff} can be calculated from the effective lifetime τ_{eff} and the diffusivity *D* by following equation:

$$L_{Diff} = \sqrt{D \cdot \tau_{eff}}$$

As this effect is even more pronounced in passivated samples it will be discussed in more detail with their results.

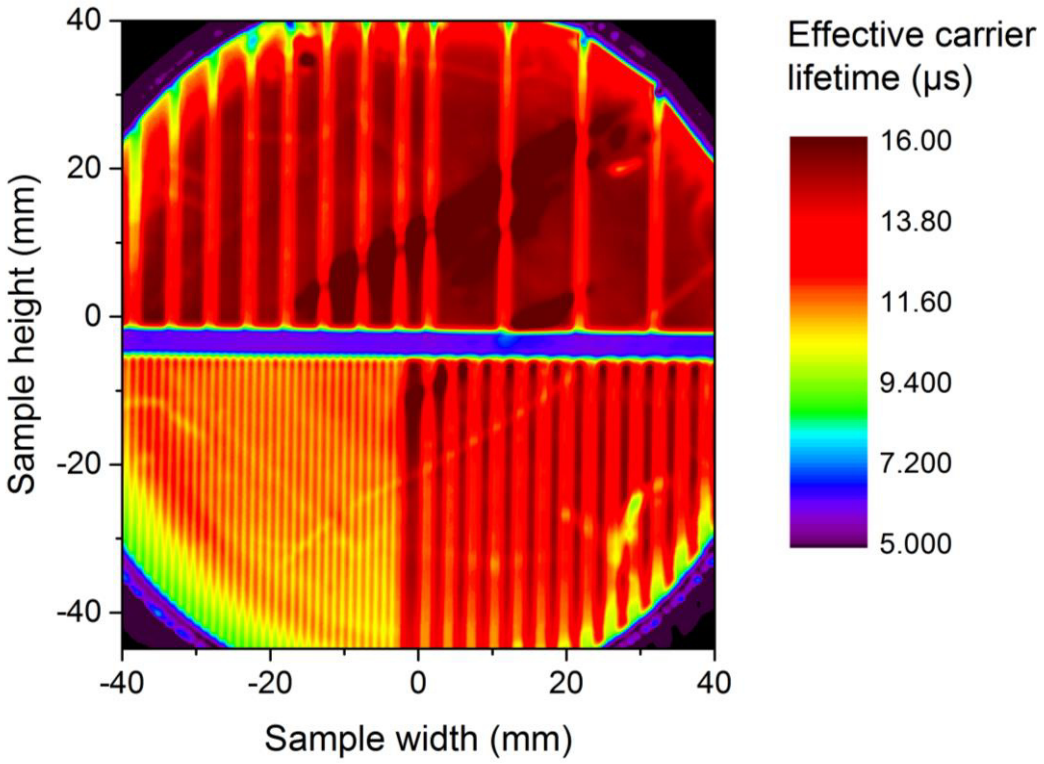

Figure 3.10: Effective carrier lifetime map before application of the passivating SiN_x layer.

Samples without any structuring and with emitter on the front side were fabricated as references. A µPCD lifetime map of one reference with SiN_x passivation is displayed in Figure 3.11. Inhomogeneities in effective carrier lifetime originate in handling and processing issues and are commonly observed. The two processed reference samples exhibit a similar average effective lifetime of 250 – 255 µm, which can vary locally.

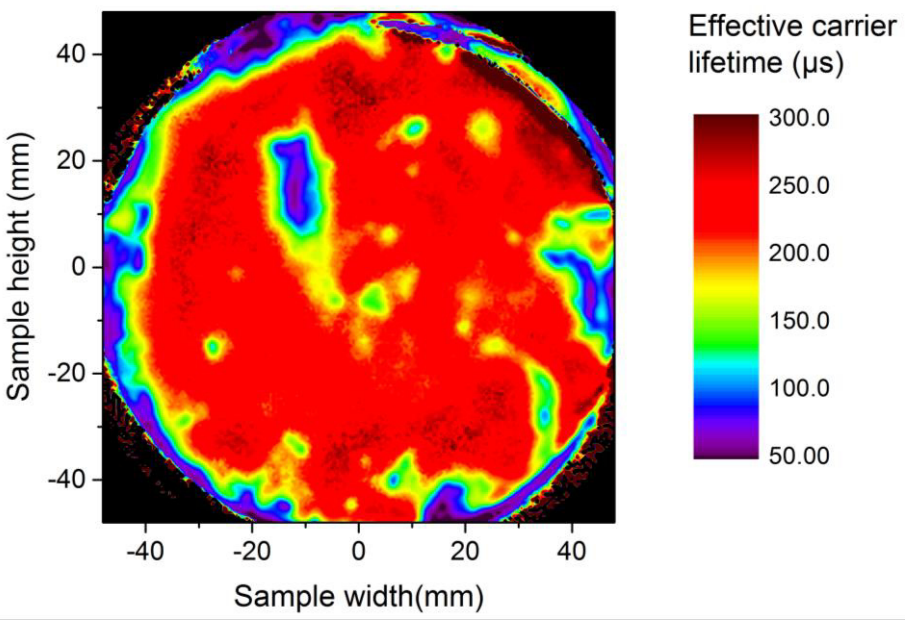

Figure 3.11: Effective carrier lifetime map of reference sample without any structuring after SiN_x deposition.

The effective lifetime of passivated, structured samples shows inhomogeneities as on the unstructured samples and has a different distribution than before application of the passivating layer. As can be seen in Figure 3.12 (especially in the area with 10 mm trench distance), the trench structure has two effects: At the trench edges the lifetime is reduced while it exceeds that of the emitter in the trench center. In the middle of the graph the base area can again be seen, where the emitter was etched. The base area has an increased effective carrier lifetime of approx. 350 – 400 µs on this sample and up to 500 µs on other samples. The increase of lifetime in the trenches can be explained by the higher lifetime of the passivated base area, which should be at 350 – 500 µs. The decrease at the edges is then attributed to the pn-junction, which is created by the emitter structuring.

Looking at the line scan of the area with 10 mm trench distance in Figure 3.12, a lifetime peak of the trench is followed by a dip caused by the pn-junction and increases again to reach the roughly 250 µs of the emitter. Going to smaller trench distances of 5 mm, the lifetime does not reach the 250 µs in the emitter area anymore as the next pn-junction reduces the lifetime again. For the 3 mm trench distance the influence of base area and pn-junction dominates the lifetime. The striped structure can still be seen for trench distances of 1 mm, although not as pronounced.

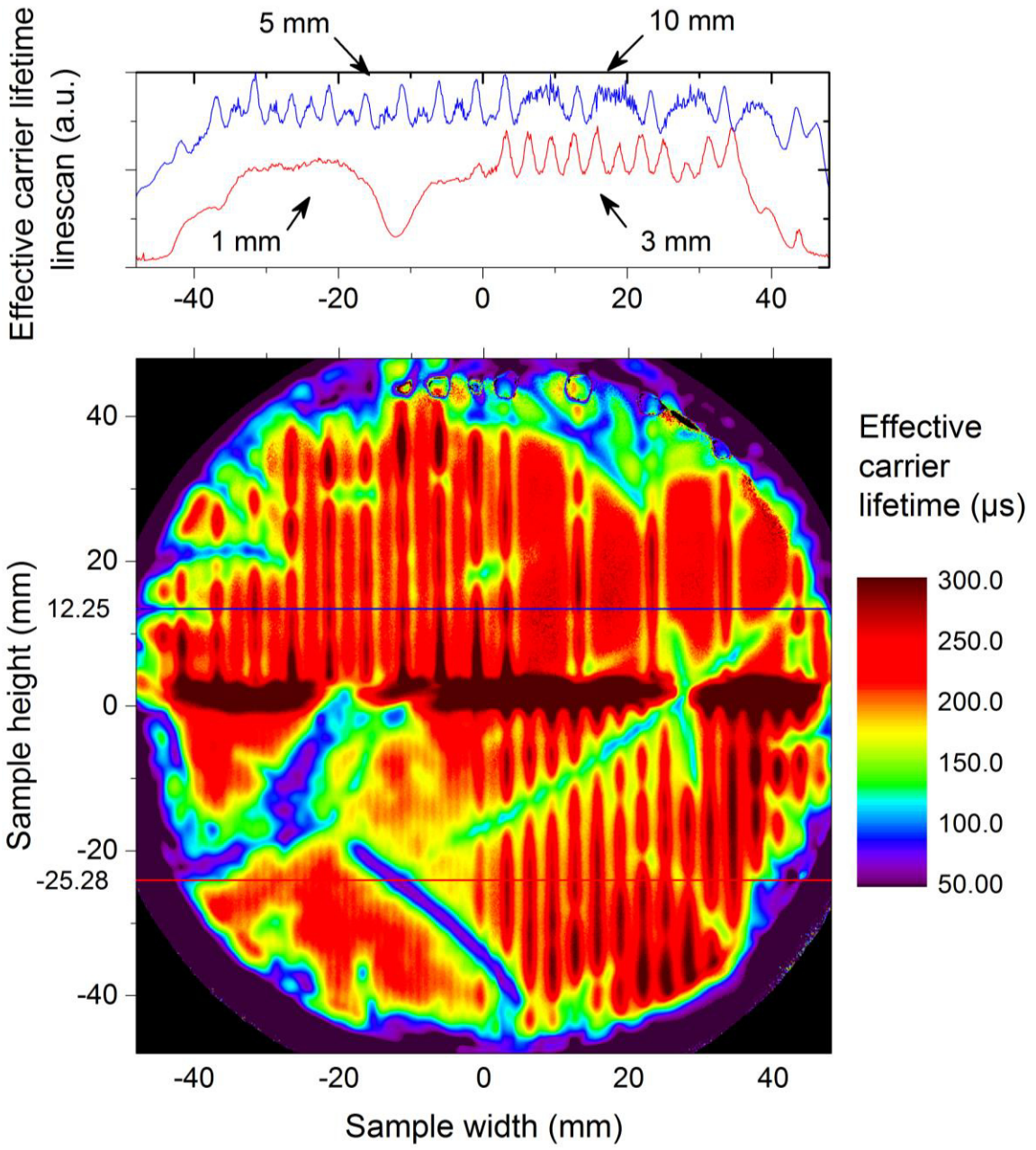

Figure 3.12: Effective carrier lifetime map of structured and passivated sample. Line scans show the lateral lifetime distribution.

The influence of base area and pn-junctions is approx. 5 mm wide, which is again wider than the actual structure size of 310 µm. As in the case of the unpassivated sample, the widening occurs due to the diffusion of minority carriers in the sample. As the passivated samples have a lower surface recombination velocity and consequently overall higher effective lifetime than the unpassivated sample, the diffusion length is larger in passivated samples (see equation (3.9)) and therefore the influence of base area and pn-junctions widens.

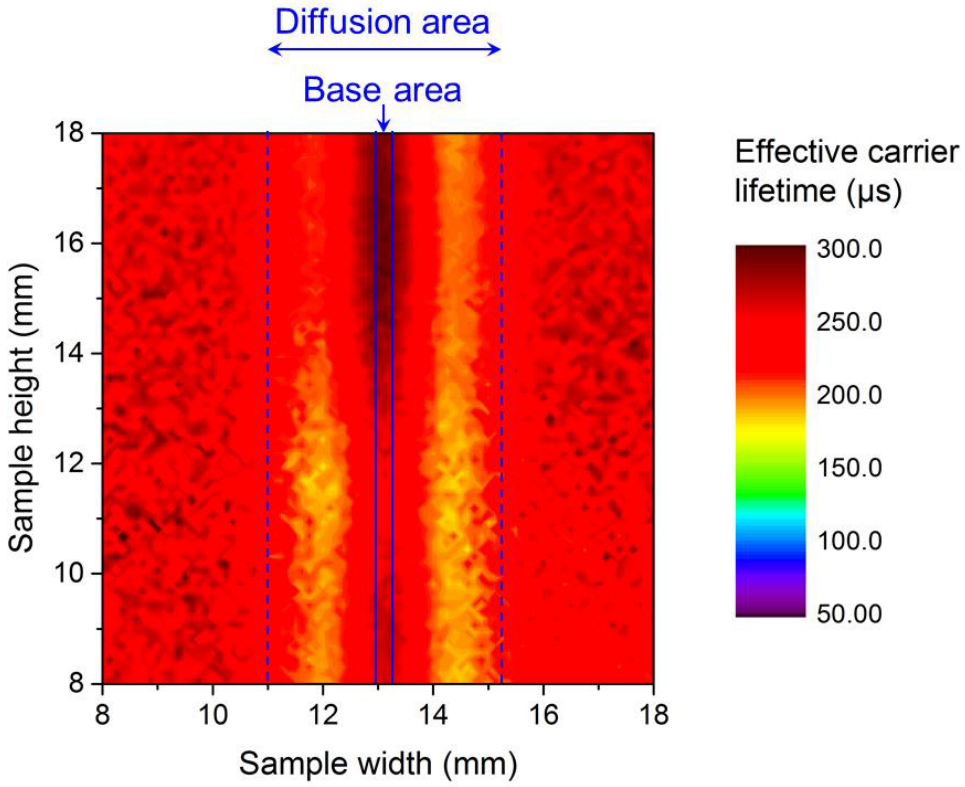

Figure 3.13: Enlargement of measurement displayed in Figure 3.12. The dimensions of base area and diffusion area are indicated by the solid and dashed line respectively.

To cause the structure width of approx. 5 mm in the µPCD map, the diffusion length has to be 2 – 2.5 mm. Figure 3.13 shows the effective lifetime in proximity of a trench; the location of the actual base area is indicated by the solid lines, dashed lines represent the diffusion area for a diffusion length of 2 mm, where the effective lifetime is influenced by base area and pn-junctions.

In order to illustrate how the local minima in effective lifetime at the pn-junctions in proximity to the local maximum of the base area can form a profile as observed in lifetime measurements around the trench, gauss fits of all three extrema and their sum is shown in Figure 3.14. The location of the pn-junctions at the dashed lines corresponds to the minima of the two gauss fits. The resulting minima of the cumulative fit clearly lie further apart than the actual minima of the single fits, as in the lifetime maps.

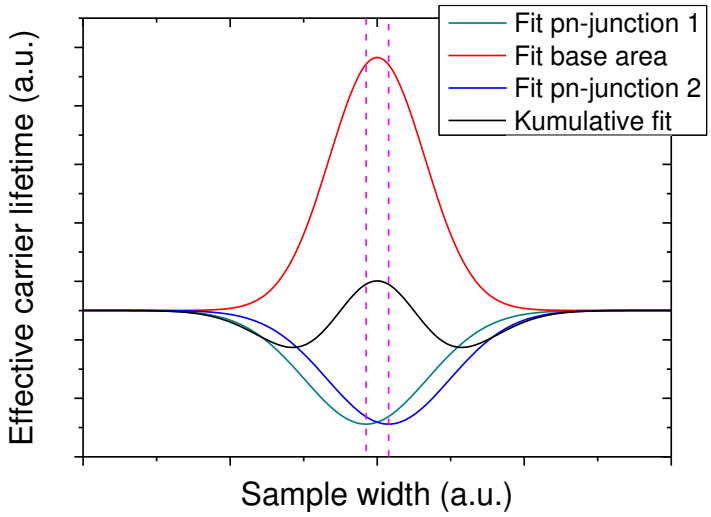

Figure 3.14: Gauss fit of base area and both pn-junctions. Cumulatively they create a profile similar to the measured profile, with a widening of the structure. The dashed pink lines indicate the location of the pn-junctions.

A quantitative analysis of this phenomenon was not done, as the locally varying surface recombination velocities interfere with each other and a more detailed simulation would be required. Furthermore the structure does not resemble the situation in the iSiMo concept, where there is no underlying base area in the trench. The surface recombination velocity at the pn-junctions is nevertheless interesting for the optimum cell strip width. Apart from the pn-junction itself there are several factors that increase the surface recombination velocity:

- The frayed edges of the step defining the base area, which are shown in Figure 3.9, result in an increase of surface area and consequently an increase in surface recombination velocity.
- The middle section of the step at the pn-junction exhibits a rough silicon surface compared to for example the trench edges, as shown in Figure 3.15. The rougher surface increases the surface area which again leads to an increase in recombination velocity.
- The SiN_x layer on rough surfaces is also rougher, as can be seen in Figure 3.15. This leads to local thickness variations in the SiN_x layer, which can influence the surface recombination velocity.

All these factors depend on the structuring of the silicon and the used processes can be optimized to reduce or even avoid rough surfaces that lead to an increase in surface area.

Nevertheless, the influence of the pn-junctions remain and the lifetime measurements suggest that the effective lifetime of 1 mm wide cell strips would be limited by the surface recombination velocity at the pn-junctions. As there is no base area in case of real modules and the rough surfaces at the pn-junctions can be avoided, 3 – 4 mm are assumed to be the minimum width the cell strips should have.

To reduce the negative influence of the pn-junction itself in an iSiMo module, the structure could be altered as shown in Figure 3.16. On the left the structured emitter as used in the iSiMo modules is shown, with a lateral pn-juntion on both sides of the trench, while on the right the emitter was only structured at one side of the trench. The latter solution cannot be realized in combination with an epitaxial emitter, which is grown in situ with BSF and base before the fabrication of the trenches. Additionally the emitter must have a sufficiently high doping concentration to overcompensate the BSF doping concentration and the interface of BSF and emitter could still lead to increased recombination at that spot, which would have to be investigated. The presence of an emitter on the trench slope would have the positive effect, that no shunting due to the metal finger crossing a pn-junction could occur. The first solution for emitter structuring was chosen for the fabricated iSiMo modules, as overcompensating and interface effects were not evaluated. With the increase of surface recombination velocity at lateral pn-junctions on both sides of the trench, the effective lifetime of the whole cell is reduced, when small cell strip widths are used.

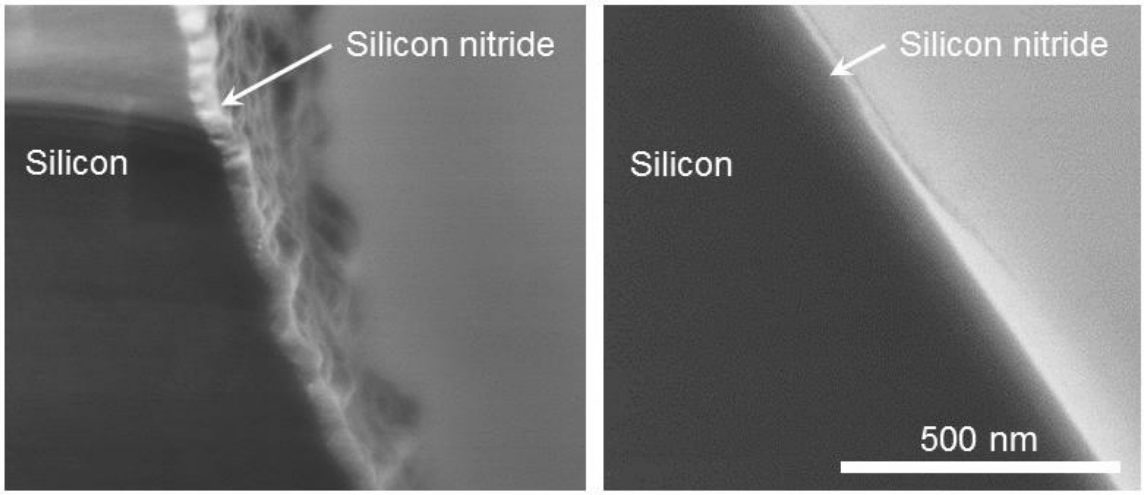

Figure 3.15: SEM pictures of silicon nitride layers on the rough silicon surface at the step of the pn-junction (left) and the smooth silicon surface at the trench edge (right).

Figure 3.16: Schematic of possibilities for emitter structuring with emitter etching on both sides of the trench (left) or only on one side (right). Silicon is depicted yellow and the SiO_2 intermediate layer blue, while BSF and emitter are green and red, respectively.

3.3.5 Optimum cell strip width

As the optimum cell strip width is a compromise between the previously discussed active module area, series resistance and edge effects, it was decided to test the effect in mini-modules. For the active module area as well as concerning the edge effects the minimum cell strip width is considered to be 3 mm, while for the series resistance 10 mm was found to be the maximum. The optimum should therefore lie in this range. To investigate the connection of both effects to the efficiency further, mini-modules were fabricating using 3, 5 and 10 mm wide cell strips. Photolithography masks were designed for all structuring steps for all three cell strip widths. Detailed processing and the results of the mini-modules can be found in chapter 7.

4 PLASMA TEXTURE

In this chapter the development of plasma texturing processes in two different etching tools is described. The textures were optimized for epitaxially grown crystalline silicon thin-films and applied to thin-film and wafer solar cells, which are also discussed.

Texturing of solar cells is used to reduce reflection on the silicon surface and to enhance the optical path length of incoming light. A reduction of the reflectance of the silicon surface can also be obtained by applying an anti-reflective coating (ARC), whose principle is to use the interference of the light reflected at the layer interfaces to transmit as much light as possible into the cell. Thickness and refractive index of the ARC are tuned to meet interference condition $n \cdot d = \frac{\lambda}{4}$, as described in [26], which means that the refractive index n has to lie between that of air (n_{air} = 1) and silicon (n_{Si} = 3.4). The thickness is set so that the ARC exhibits a reflection minimum at 600 nm, as this results in the lowest overall reflection under the AM1.5 spectrum [26]. The reflection can be lowered over a broader wavelength range by using multilayer stacks. The double layer anti-reflective coating (DARC) used for solar cells discussed in this chapter consists of TiO_x with n = 2.2 and MgF_x with n = 1.37. A comparison between the reflections of a solar cell with a planar surface without ARC, a single layer TiO_x ARC and a TiO_x/MgF_x DARC can be seen in Figure 4.1.

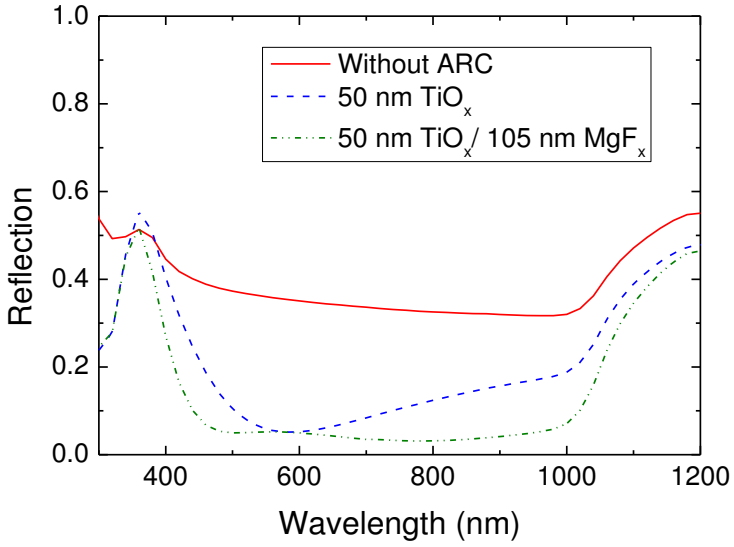

Figure 4.1: Reflection of a solar cell without ARC, with a single layer ARC of 50 nm TiO_x and with an additional 105 nm MgF_x.

A single layer ARC is preferred, especially in industrial processing where a PECVD SiN_x with n ≈ 2 and d ≈ 70 nm is most commonly used.

The implementation of a reflective intermediate layer (IL) on the rear side, which works by the same principles as the ARC, leads to a second pass of the light through the solar cell and therefore an increased absorption of light, especially in the long wavelength range (see Figure 4.2).

In crystalline silicon thin-film solar cells, light trapping is crucial for the solar cell performance, as the typical solar cell thickness is 20 – 40 µm. At this thickness range only light with wavelengths up to 850 – 900 nm is absorbed during one pass through the layer. A textured surface leading to an oblique coupling of the incoming light elongates the optical path length, which, combined with a reflective rear side, can also lead to light trapping. In this case, light that is reflected at the rear hits the front surface again under an angle that allows total reflection (see Figure 4.2).

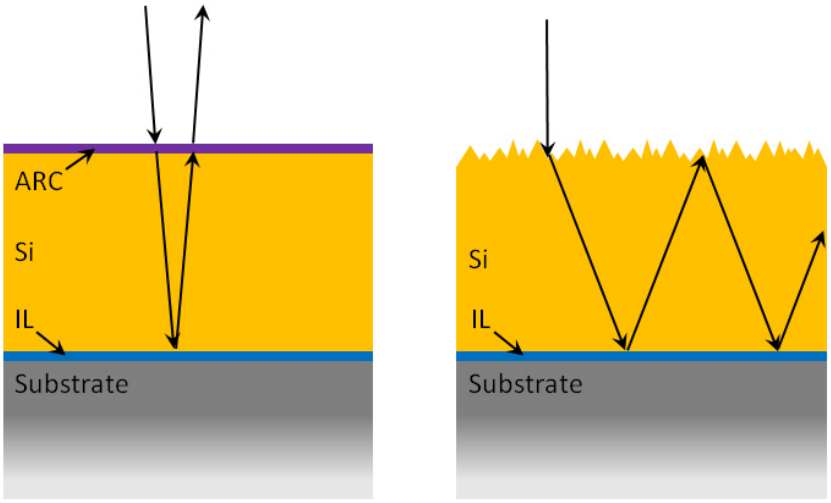

Figure 4.2: Schematical illustration of influence of anti-reflective coating (left) and texture (right) in combination with a reflective intermediate layer (IL) at the rear side of the silicon absorber

4.1 Texturing methods

Several different texturing methods are under investigation for use in solar cells. The most important methods will be discussed here with respect to their application in crystalline silicon thin film solar cell fabrication.

4.1.1 Wet chemical texturing

The random pyramid texture is the most widely used texture for monocrystalline solar cells and can be obtained by alkaline etching typically in potassium hydroxide (KOH) or sodium hydroxide (NaOH) based solutions. They exhibit an anisotropic etching behavior, etching <111> planes slower than other crystal orientations, which leads to pyramids of 5 to 10 µm height with <111> oriented flanks. Combining the alkaline etch with a patterned mask on the wafer (often silicon oxide), inverted pyramids or honeycomb textures can be realized.

As the etching is dependent on the crystal orientation it is not suitable for multicrystalline wafers. On multicrystalline material, the texture would vary widely across different grain orientations, ranging from upright pyramids to tilted pyramids to a polished surface.

For the wet chemical texturing of multicrystalline solar cells, acidic etching solutions are used containing hydrofluoric acid (HF), nitric acid (HNO_3) and in some cases acetic acid (CH_3COOH). The etch mechanism is based on the oxidation of the wafer surface through HNO_3 and subsequent silicon oxide etching through HF. Depending on the composition of the etching solution, polishing or

texturing of the wafer surface can be realized [33]. The texture formation relies on the presence of saw damage. Emanating from an increased etch rates at defects, deep structures are formed which widen and flatten out again during further etching. Consequently the reflectivity of the surface can be controlled by adjusting the silicon removal.

A smoother surface leads to a higher V_{OC}, as the surface can be passivated more easily. A balance between a good reflectivity and a good passivation needs to be found to maximize the solar cell efficiency. The typical reflectivity of silicon wafers after acidic texturing is around 25 – 30 %.

Structures formed by wet chemical texturing lead to a silicon removal during the texturing process of at least 10 µm. All silicon that is removed during cell processing of crystalline silicon thin film solar cells has to be epitaxially grown beforehand. This means, if 10 µm are removed during texturing, a 25 – 50 % thicker silicon layer needs to be grown, which increases the cost.

4.1.2 Alternative texturing methods

Different approaches exist to texture wafers mechanically, e.g. by dicing saw [34] or laser [35], but have not been established in industry. Due to the rather large feature sizes of dicing saw texturing and high amount of silicon removal for laser texturing, mechanical texturing is not considered a good alternative for crystalline silicon thin film applications.

Another alternative is atmospheric pressure dry etching. As described in [36] little silicon removal of 0.35 to 2.9 µm is necessary to create the nanoscale texture. It could therefore also be a good alternative for c-Si thin-film applications, but is still in development and the applicability to epitaxially grown silicon surfaces still has to be shown.

4.1.3 Plasma texturing

Plasma etching can be used to texture silicon wafers in combination with a pre-structured mask or in a self-masking process. Fluorine or chlorine containing processing gases can be used in silicon etching plasmas [37] and depending on the intended effect, different additives are used.

For the etching process with a pre-structured mask, a mask which consists of dielectric layers, like SiO_x or SiN_x, or resists needs to be applied, structured by

lithography or laser and must be removed after the etching step. During this step the texture is formed in the pre-structured pattern. An example is honeycomb texturing through nanoimprint lithography as reported by Hauser et al. [38]. Here, a resist is applied to the silicon surface and structured by nanoimprint lithography. The honeycomb texture is etched into the wafer by a two-step plasma etching process typically forming about 10 µm deep structures. As already discussed for wet chemical texturing, the structure size for c-Si thin-film applications should be smaller to have less silicon removal. In principle smaller structures which lead less silicon removal are also possible and could then be suitable for c-Si thin-films with the drawback of requiring a mask.

In a self-masking process no mask needs to be applied before the etching process. The reactive gas mixture of the plasma itself provides the mask. The reactants form randomly distributed molecules on the surface that passivate against etching. As described e.g. in [39] one possible gas configuration to achieve self-masking is the combination of SF_6 and O_2. SF_6 is a frequently used gas in plasma etching of silicon. While addition of small amounts of O_2 is known to accelerate the silicon etching increasing the O_2 content further leads to a lower etch rate [40]. The increase in etch rate originates in the reaction of Oxygen with SF_x radicals, which increases the F atom concentration. After an even further addition of O_2 the self-masking effect compensates for this and eventually decreases the etch rate by forming $S_xO_yF_z$ and $Si_xO_yF_z$ passivating films on the surface [41]. These films are randomly distributed over the surface and can lead to a randomly textured surface. The structure of the texture is variable by adjusting the relevant process parameters and ranges from inverted pyramid or pyramid structures to bowl structures to black silicon structures [7, 42] .

For self-masked plasma texturing the silicon removal varies depending on the formed structure size. Structure sizes that are discussed in this thesis are in the range of 0.5 µm to 1 µm, which allows a silicon removal of about 3 µm that can be combined with crystalline silicon thin film solar cells.

4.2 Characterization of a texture

There are various properties of a texture that must be investigated in order to assess its applicability in crystalline silicon thin-film solar cells. Important measurements to characterize the plasma textures are reflectance, lifetime, silicon

removal, texture homogeneity and structure of the texture along with solar cell processing and characterization.

Reflection measurements

For the reflectance measurements a Varian Cary 500i was used. Total reflection and diffuse reflection were measured in the wavelength range from 250 to 1200 nm. For the total reflection measurement the sample is fixed on the integrating sphere in an angle of 3 ° 20 min to the tangent plane, which causes all reflected light, the directly reflected light as well as the light reflected under an angle, to hit the walls of the integrating sphere and be reflected into the detector. To measure only diffuse reflection, the sample is fixed on the integrating sphere in a tangent plane. This leads to exiting of the non-diffuse part of the reflected light through the inlet of the beam and therefore only the diffusely reflected light reaches the detector. As stated in [7], a diffuse reflection also means diffuse in-coupling of light and can therefore be used as a parameter of the light-trapping properties of a texture.

Lifetime measurements

Not only the optical but also the electrical properties of a texture are essential for the good performance of a solar cell. Lifetime measurements were made to determine if the texturing process induces damage in the silicon and if the formed structure can be passivated. The measurements were carried out by microwave photoconductance decay (µPCD) and by quasi steady state photoconductance (QSSPC). A detailed description of both methods can be found in [32].

Silicon removal

An important factor for silicon thin-film solar cells is the amount of silicon removal in a texture. The etch rate can also hint at the amount of self-masking in a process. The silicon removal was therefore measured either by weighing or by measuring the step height on a sample that was partially covered during the process.

Homogeneity

The homogeneity of textured samples was not a big issue for small samples up to 5 x 5 cm². Only when attempting to texture large area samples did it become necessary to optimize the process concerning the homogeneity and therefore parameterize the homogeneity. This was done by visually judging the homogeneity and dividing the samples into categories. At this stage, two types of homogeneity were assessed: The homogeneity depending on grain orientation which will be referred to as grain homogeneity and the lateral homogeneity over the whole wafer area, the area homogeneity. Categories range from 1 to 4, and from 1 to 5 for grain homogeneity and area homogeneity respectively, with 1 being the best and 2 still being acceptable.

Another possible method would be to scan the samples and assess the homogeneity by calculating the standard deviation from the histogram of grey scale values. This method was not yet fully established and therefore not used. A significant drawback is that it is not easy to distinguish between the two different types of homogeneities.

Structure of the texture

As the size of the developed textures is in the range of 0.5 µm to 1 µm it is not possible to characterize the structure itself by optical microscopy, instead a scanning electron microscope (SEM) was used. Analyzing the appearance of the texture can yield information about the development of the structure.

Manufacturing of solar cells

The optimization of a texture for solar cells is always a trade-off between low reflection and low surface recombination velocity. The interaction of both in the solar cell can be best evaluated by manufacturing and characterizing textured solar cells. While an effective texture leads to an increased short circuit current (J_{SC}), the open circuit voltage (V_{OC}) should not or at least not significantly drop due to application of a texture. A good fill factor (FF) indicates the cell could be contacted well and the metallization process is compatible with the textured surface. The internal quantum efficiency (IQE) shows that the surface was passivated sufficiently if there is no drop of the IQE in the short wavelength range

compared to planar cells. The light-trapping effect itself can be seen by an enhanced IQE in the long wavelength range, especially in combination with a reflective rear side.

4.3 Plasma texturing tools

Two different plasma etching tools were used in this work. Both are single wafer reactors for wafers with diameters of up to 200 mm and 300 mm, respectively. Smaller samples can be processed side by side on a plate.

The SI 600 from Sentech Instruments for wafers up to 200 mm diameter works in an electron cyclotron resonance reactive ion etching (ECR-RIE) configuration. A description of the tool can be found in [43]. Plasma excitation in this configuration is realized by a capacitively coupled radio frequency (RF) source, by micro wave (MW) excitation or a combination of both. In a capacitively coupled plasma the RF is usually applied between the electrode in which the sample is placed and the chamber walls. As explained in [43], a potential difference accumulates between the plasma and the electrode and accordingly the plate. This so-called bias voltage accelerates the ions onto the plate and causes physical etching on the samples on the plate.

In the Plasmalab System 133 from Oxford Instruments, for wafers up to 300 mm, the plasma is also excited by a capacitively coupled RF source and, instead of MW excitation, an inductively coupled RF source is used and combinations of both are possible. This configuration is called inductively coupled plasma reactive ion etching (ICPRIE). Inductive coupling is achieved by application of the RF to a coil wrapped around the reactor. A more detailed description can be found in [44]. Additionally, a so-called magnetic ring (MR) can be used, which is also a coil wrapped around the reactor. No RF, but a constant current is applied to the coil, inducing a static magnetic field in the reactor chamber. This magnetic field directs the plasma away from the walls of the chamber to minimize interaction of the reactant species with the chamber walls.

Due to the combination of two plasma excitation methods, the plasma density and ion energy can be controlled separately in both tools. While the MW plasma and the ICP are used to control the plasma density, the incident energy of the ions is independently adjusted by the capacitively coupled plasma (CCP).

4.4 Plasma texturing processes

To create a self-masking plasma texturing process SF_6, O_2 and NH_3 were used as processing gases in the SI 600, based on a process that was developed by Lindekugel [7] for a SiNA setup from Roth&Rau. The plasma was ignited by a RF pulse of 10 s and sustained by MW excitation during the process. In the Plasmalab System 133, a process without the toxic NH_3 was developed and only SF_6 and O_2 were used as processing gases. The ignition of the plasma was also realized by a capacitively coupled RF pulse, while it was sustained during the process either by an ICP or a combination of ICP and CCP.

In the following paragraphs, process variations for the texturing process in the SI 600 and the Plasmalab System 133 are shown. At the SI 600 the influence of gas flow rates, processing time, pressure and distance between sample and plasma on the etching result were analyzed, while at the Plasmalab System 133 the gas flow rates, processing time, power of CCP and ICP RF excitation as well as the magnetic ring current were varied.

4.4.1 Plasma texturing process at SI 600

Unless otherwise stated, the processes were carried out at a pressure of 5 Pa, with the plate cooling set to 40 °C, a MW power of 1200 W, electrode height of 130 mm (which defines the distance between sample and plasma) and a processing time of 15 min. After determining the optimal gas flow rates (see section below) 90 sccm SF_6, 20 sccm O_2 and 10 sccm NH_3 were used.

Gas flow rates

The plasma-texturing process using SF_6, O_2 and NH_3 is similar to the process without NH_3. As already described in [7] it is assumed that the ammonia alters the composition of the self-masking layer. It was observed that with a high NH_3 flow, a white layer forms on the wafer surface, which could be scraped off and revealed a still polished silicon surface underneath. The layer was analyzed by scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDX), as shown in Figure 4.3.

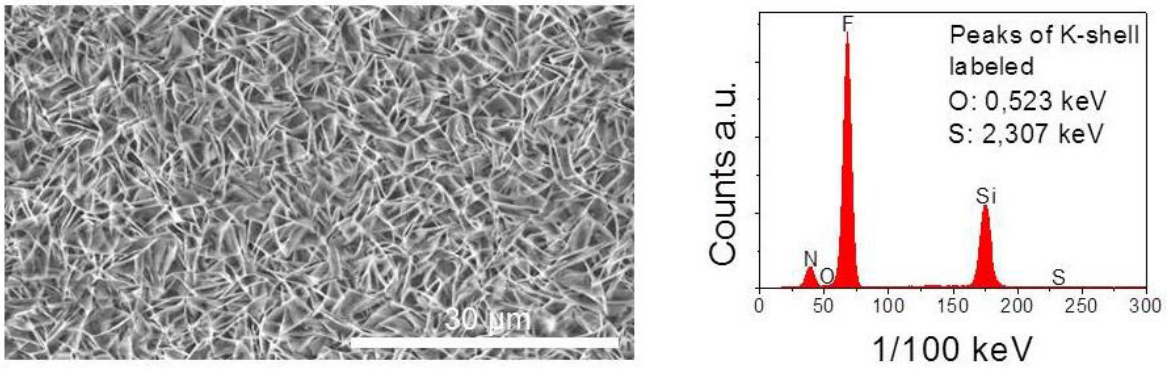

Figure 4.3: Left: SEM picture of deposited layer during process with high NH_3 flow, right: EDX measurement of that layer.

It was found to consist mainly of fluorine, silicon and nitrogen, where the silicon peak could also originate from the substrate below. No oxygen or sulfur were measured in the layer despite of playing the major role in the self-masking process in a SF_6/O_2 etch. These results support the assumption that the composition of the self-masking layer is altered by the addition of NH_3 to the process.

The processing gas flow rates must be adjusted to form a self-masking layer that sufficiently masks the silicon surface against etching but not so thick that etching is completely inhibited. The optimal gas flow rates were found to be 90 sccm SF_6, 20 sccm O_2 and 10 sccm NH_3 leading to a texture with about 15-20 % reflectivity on FZ and mc material. Reducing the oxygen or ammonia flow leads to higher reflectance, which can be expected due to insufficient self-masking. Increasing the oxygen flow leads to higher reflectance but also a lower etch rate, indicating the excessive formation of a masking layer. Higher ammonia flows lead to a deposition of the fluorine containing layer discussed above.

Processing time

Silicon wafers were processed with different etching times to see the development of the structure. Their reflectance was measured and the structure analyzed in the SEM. Lifetime samples were also fabricated with varying etching times. 0.5 Ωcm p-type FZ material was used in this case and the samples were textured and passivated with 60 nm PECVD SiN_x on both sides.

In Figure 4.4 reflection measurements of the first batch with varying processing times can be seen on the left. In the batch of lifetime samples (Figure 4.4, right), the reflections were slightly increased by up to 3 % abs. compared to the samples of the preceding batch. Nevertheless, a trend can be seen in both cases. After

5 min of texturing the reflection is lowest, but the diffuse share at 85 % is lower than after longer texturing processes, where the diffuse part is > 99 % of the total reflection. This might lead to a less oblique coupling in of light. For more than 10 min of texturing, the reflection only slightly increases and saturates below 20 %. The origin of the different reflectivities as well as the formation of the texture can be inferred from the SEM pictures in Figure 4.5. Samples after 5, 15, 20 and 30 min are shown. An increase in structure size can be observed with increasing processing time as small structures of 0.3 – 0.5 µm are initially formed which eventually deepen and widen up to 1.0 – 1.2 µm with increasing processing time. The difference between the samples textured for 20 and 30 min is already comparatively small and the reflection measurements suggest that the structure does not change significantly after 30 min. The carrier lifetime was measured by QSSPC and is depicted on the right side of Figure 4.4. As expected, the planar sample exhibits the highest lifetime. The lifetime decreases with longer processing time, which can be partly attributed to surface area enlargement due to the texturing. It can also be concluded that the process did not damage the surface severely, as textured samples show lifetimes up to 270 µs. As already stated above, the optimum between low reflection and low surface recombination velocity needs to be found and their interaction is best analyzed in solar cells.

As the structure shows the targeted size of about 1 µm after 15 min as well as a low reflection, a processing time of 15 min was used in following processes.

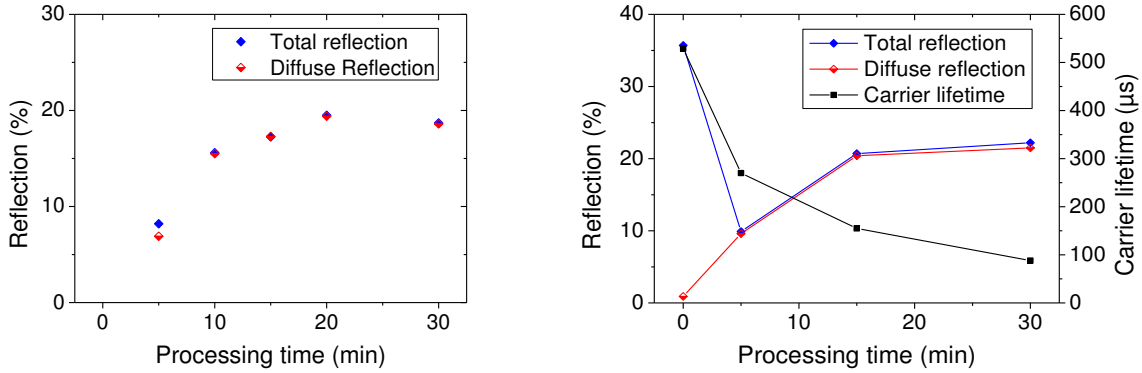

Figure 4.4: Weighted reflection of samples processed for different times. Left: First variation. Right: Batch for lifetime measurements; carrier lifetime for samples textured with different processing times is also displayed.

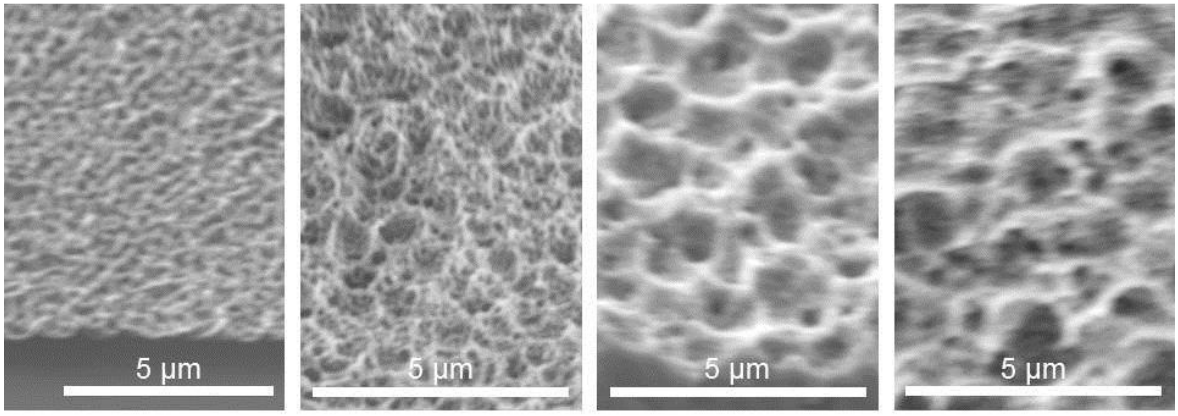

Figure 4.5: SEM pictures of tilted samples after texturing for different processing times. Texturing time from left to right: 5, 15, 20, 30 min.

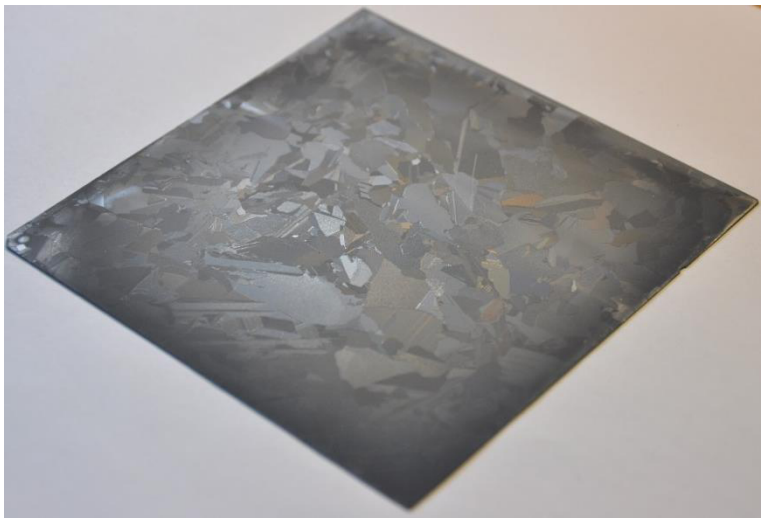

Figure 4.6: Picture of 10 x 10 cm² sample showing a ring structure after texturing.

Texturing of large area samples

The process was optimized for samples of up to 10 x 10 cm². Samples textured with preliminary parameters showed a ring structure with lower reflection in the middle than at the edges of the sample due to the circular reactor geometry, as shown in Figure 4.6. To reduce the influence of the reactor geometry, the electrode was lowered and the pressure reduced to obtain a more uniform distribution of processing gases.

For sample areas of 5 x 5 cm² the pressure was varied between 1 and 9 Pa. A texture was obtained for pressures between 3 and 5 Pa, which can be seen in reflection measurements (Figure 4.7). When texturing 10 x 10 cm² wafers with lower electrode height the pressure was set to 3 and 5 Pa. For an electrode height of 110 mm this resulted in a weighted reflectance averaged over various points of 14.6 % (79 % diffuse share) at 5 Pa and 16.7 % (98 % diffuse share) at 3 Pa. The

total reflection is slightly lower for the wafer processed at 5 Pa and the diffuse share is considerably higher for the wafer processed at 3 Pa. As in a standard cell process, an ARC is usually applied in addition to texturing, the process at 3 Pa is considered more promising in solar cells and was used in all further processes. The total reflection could be lowered even further by choosing a lower electrode height.

The height of the electrode on which the sample is placed defines the distance between plasma and sample. As the tool has a downstream configuration, a higher electrode implies a smaller distance between plasma and sample. It was found that for samples processed with the same process parameters except electrode height, the sample processed at lower electrode height exhibited a lower reflectance, see Figure 4.8. SEM analyses revealed that samples processed at 90 mm electrode height have up to 0.8 µm deep structures, while samples processed at 110 mm electrode height exhibit structures of up to 0.4 µm depth (Figure 4.9). The increase in structure depth while maintaining the same width and therefore increased aspect ratio explains the reduced reflectance.

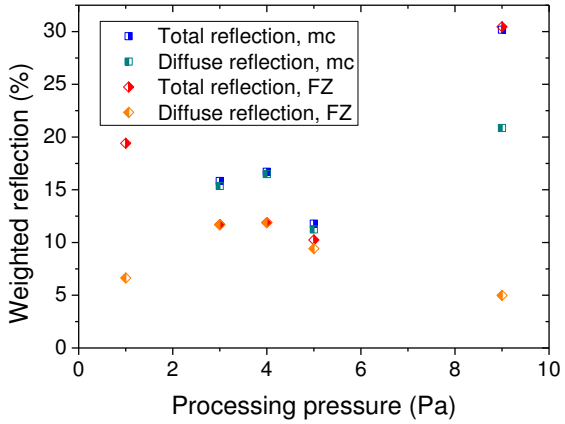

Figure 4.7: Weighted reflection of mc (blue) and FZ (red) samples after texturing at different process pressures.

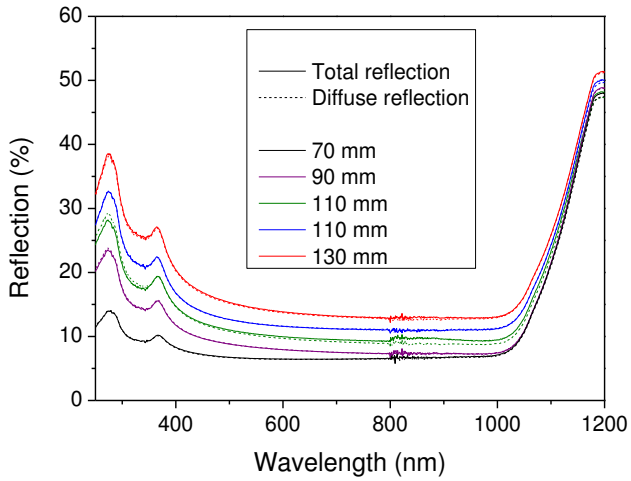

Figure 4.8: Reflection measurements of samples textured at different electrode heights.

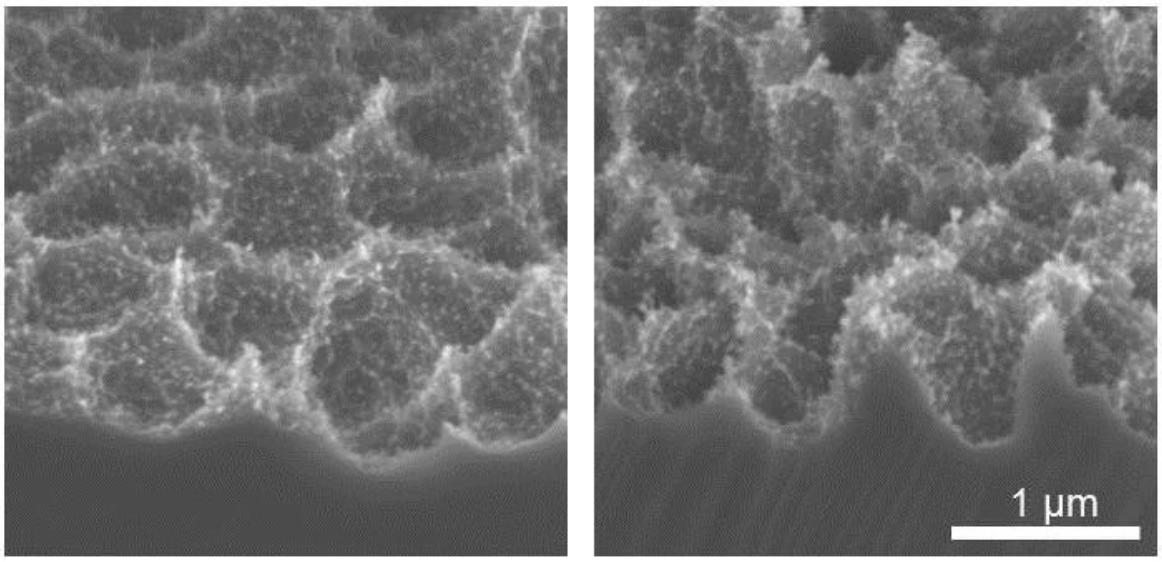

Figure 4.9: SEM pictures of samples after a process with different electrode heights, left: 110 mm, right: 90 mm.

In Table 4.1 processing parameters of the optimized texture that was used for solar cells are summarized. The electrode height was set to 70 or 90 mm as it was evaluated in solar cells.

Summing up, the experiments on 10 x 10 cm² areas always showed inhomogeneities due to reactor geometry. Solar cells were therefore only fabricated on small areas up to 2 x 2 cm² or with several predefined cells on a wafer of up to 4 inch diameter.

Table 4.1: Processing parameters of optimized texture in SI 600.

Standard SI 600 texture			
MW power	Electrode height	Pressure	Temperature
1200 W	70 / 90 mm	3 Pa	40 °C
SF_6 flow rate	O_2 flow rate	NH_3 flow rate	Processing time
90 sccm	20 sccm	10 sccm	15 min

4.4.2 Plasma texturing process at Plasmalab System 133

The plasma texturing parameters were set based on the process developed in the SI 600, as an initial point. A pressure of 22 mTorr equals 3 Pa used in the SI 600, but the plasma could only be ignited at lower pressure in the Plasmalab System 133. The pressure was therefore set to 15 mTorr at which the plasma could reliably be ignited and sustained. The ICP power was first set to 1200 W, as the MW power in the SI 600 and an RF pulse with 300 W was used to ignite the plasma. The plate cooling was also set to 40 °C and the processing time to 15 min. The electrode height cannot be varied in the Plasmalab System 133.

As previously mentioned, in this tool a process without the toxic ammonia was developed, so the gas flow rates for SF_6 and O_2 had to be adapted. In Figure 4.10 weighted reflection and silicon removal are displayed for fixed O_2 flow of 160 sccm and different SF_6 flow rates. Changing the SF_6 flow changes the SF_6/O_2 ratio as well as the total gas flow. It was assumed that the dominant parameter is the SF_6/O_2 ratio, but both were investigated later in more detail.

With increasing SF_6 flow (higher SF_6/O_2 ratio) more silicon is removed during the process, as the amount of self-masking decreases. For an SF_6 flow of 180 sccm the reflection is highest with 23 % due to excessive self-masking inhibiting silicon etching. The reflection is lowered to 12 % for a flow of 220 sccm, because less self-masking allows texturing of the the silicon. Increasing the flow further to 240 sccm the reflection rises again slightly to 14 % because of non-sufficient self-masking. In further experiments a SF_6 flow of 220 sccm and O_2 flow of 160 sccm were used.

The influence of the SF_6/O_2 ratio as well as the total gas flow were investigated in more detail in the frame of the master thesis of D. Gibb [45].

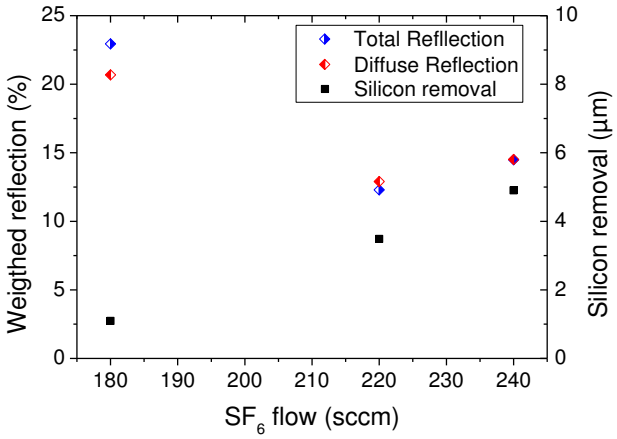

Figure 4.10: Weighted reflection (total and diffuse) and silicon removal of texturing processes with varying SF_6 flow rates and O_2 flow rate of 160 sccm.

In order to decrease the reflection further, the RF source was also used during the texturing process. The RF power was varied between 0 and 20 W, as shown in Figure 4.11. For a RF power of 5 W the reflection increases, compared to texturing without RF, while the etch rate decreases. This might be caused by excessive self–masking via additional excitation through the RF source. Further increase of RF power lead to a steep raise in etch rate due to more physical etching also lowering the reflectance to below 10 %. Further elevation of the RF power increases the etch rate but the reflection also increases as the self-masking is etched too fast. As the most promising processes, the process without RF excitation and the one with an RF power of 10 W were investigated in more detail.

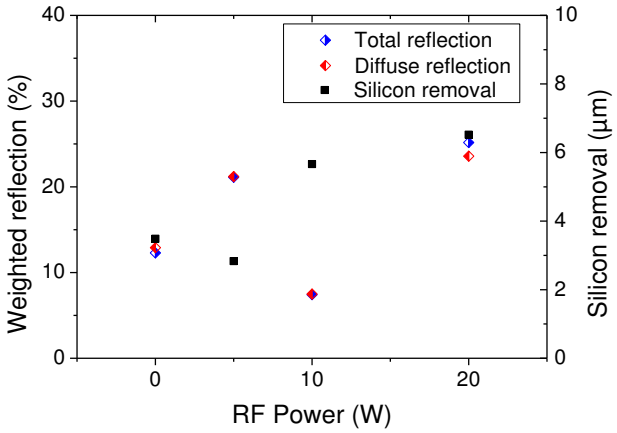

Figure 4.11: Weighted reflection (total and diffuse) and silicon removal of texturing processes with RF power of 0, 5, 10 and 20 W.

Both processes do not exhibit sufficient homogeneity on a multicrystalline wafer of 156 x 156 mm². The homogeneity was determined, as described in section 4.2, by grading into categories.

Homogeneity over different grain orientations can best be assessed by appearance of the wafer and the varying reflection on different grains. SEM pictures reveal the origin of the difference in reflection. In Figure 4.12 SEM pictures are displayed of a multicrystalline wafer after a texturing process with poor homogeneity over different grain orientations. The process used ICP without additional RF excitation and no magnetic ring current. The left grain in the cross section on the left (Figure 4.12) exhibited a lower reflection than the right one. In the grain on the left the texture formed upright structures while in the right grain tilted structures were formed. However, the SEM pictures also show that the etch rate is not higher at defect-rich grain boundaries.

Grain boundaries are difficult to find in SEM pictures following a homogeneous texturing process as the structure is visually similar on different grains. A representative example can be seen in Figure 4.13. The elevation along the grain boundary originates in the previous wet chemical damage etch and the grain boundary itself is indicated by the dashed line in the picture.

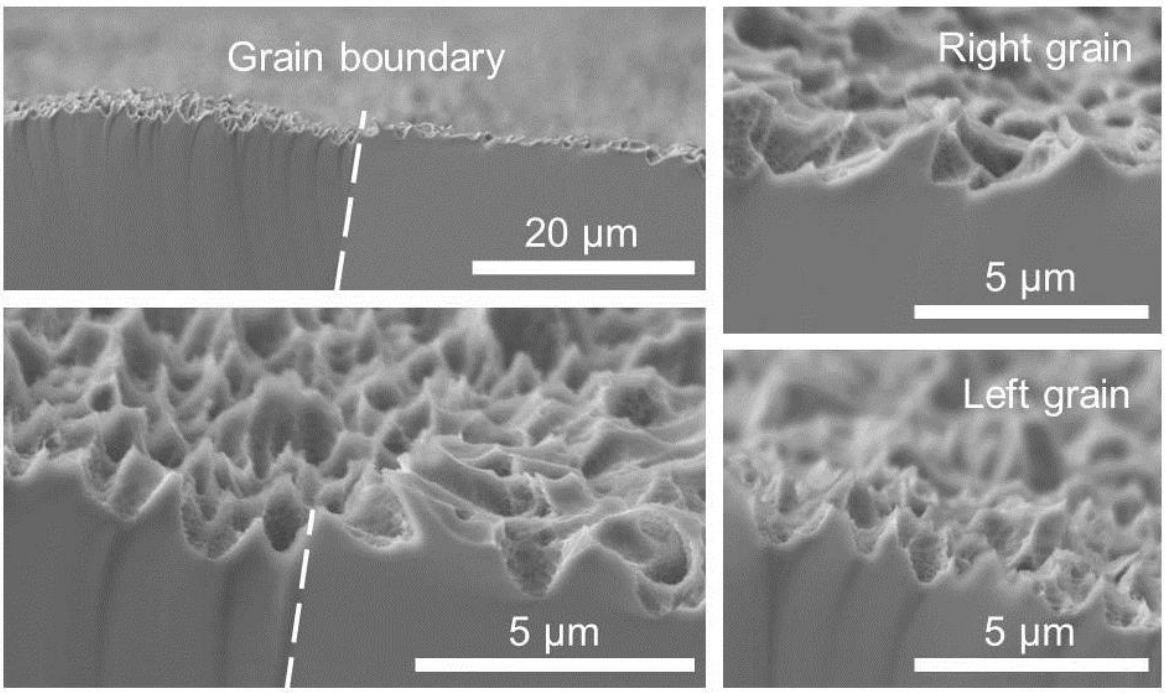

Figure 4.12: SEM pictures of multicrystalline wafer after texturing process with poor grain homogeneity. Left: Wafer cross section at grain boundary (white dashed line as guide to the eye), difference in texture on different grains can be seen. Right: Tilted texture on right grain (top) and upright texture on left grain (bottom).

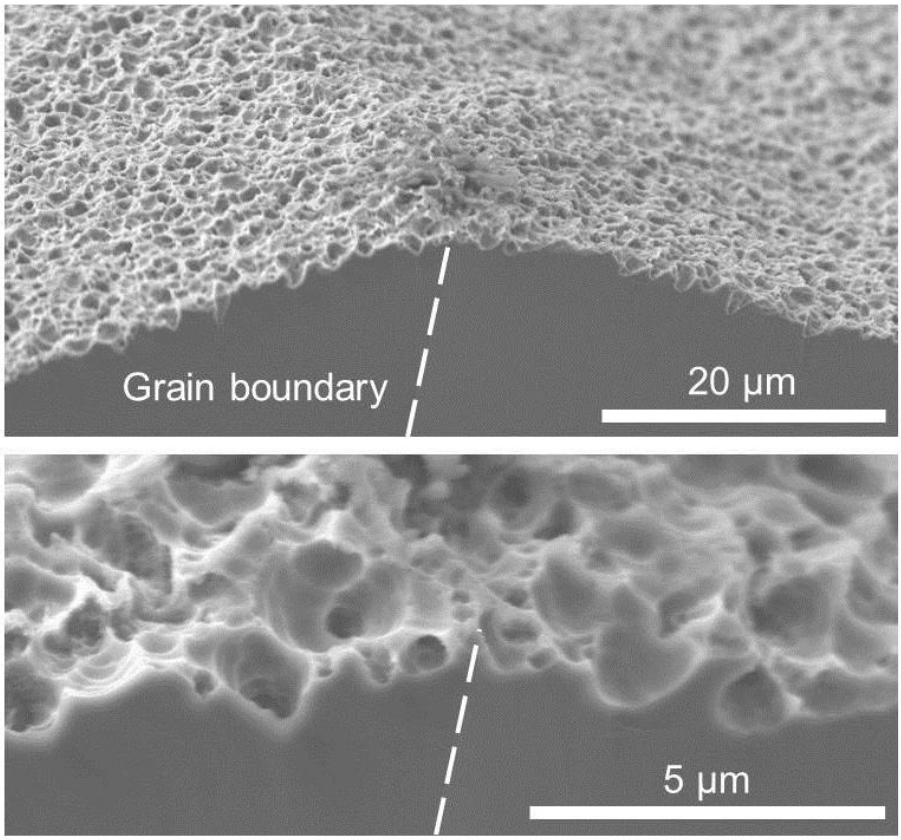

Figure 4.13: SEM pictures of cross section of a multicrystalline sample textured in a process with good grain homogeneity. The white dashed line indicates the position of the grain boundary.

Based on the processes, with RF excitation of 10 W and without additional RF power, the magnetic ring current was varied to improve the homogeneity of the processes. Figure 4.14 shows weighted reflection and homogeneity for processes without RF excitation (left) and processes with 10 W RF power (right). In the case of processes without RF, higher magnetic ring currents improve the homogeneity and, taking the reflectance into account, the optimum lies at a magnetic ring current of 3 A with a reflection of 19 %. In a process with RF power of 10 W, the grain and area homogeneity are only both in the accepted range for a magnetic ring current of 1 A. The change in reflection is relatively small and at 1 A magnetic ring current it is 11 %. It can also be seen, that less silicon is removed in the process as the magnetic ring current increases. A higher magnetic ring current leads to a lower bias voltage which in turn decreases the amount of ion bombardment on the wafer surface and therefore the etch rate.

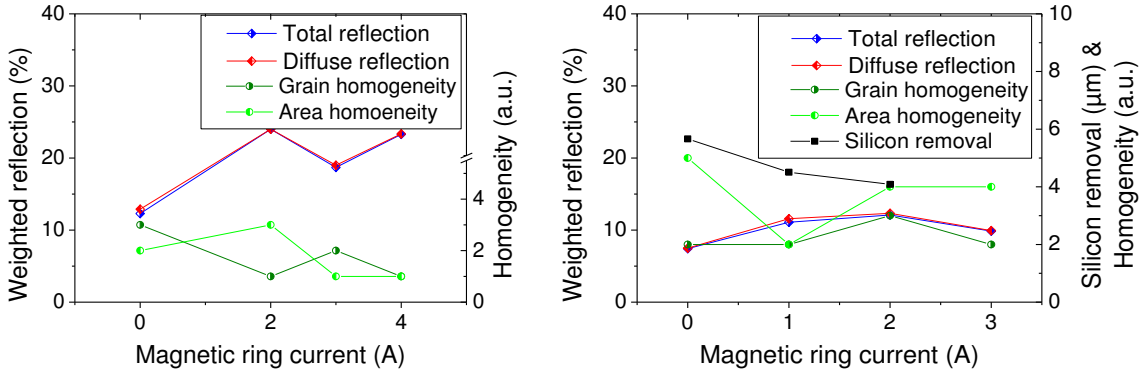

Figure 4.14: Weighted reflection, homogeneity (with 1 being the best) and silicon removal for texturing processes with different magnetic ring currents. Left: Texture without RF. Right: Texture with RF power of 10 W.

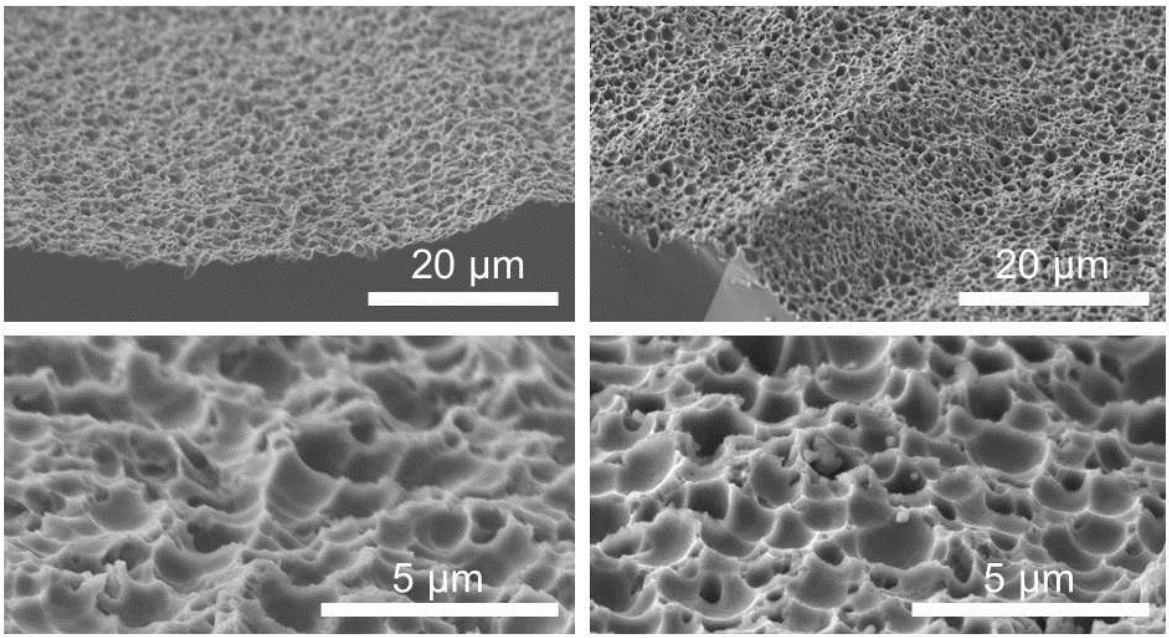

Figure 4.15: SEM pictures of samples textured in a process without RF (left) and with 10 W RF (right).

Textured samples were analyzed in the SEM after adjustment of the magnetic ring current for both processes, with RF excitation of 10 W and without any additional RF power. SEM pictures reveal that additional RF excitation caused the lower reflectance of the texturing process with additional RF excitation: The formed structure is deeper than for the process without RF, see Figure 4.15.

The table temperature was varied for the texturing process without additional RF excitation and with RF power of 10 W. For the solely ICP-powered process 40 and -10 °C and for the process with RF power of 10 W 40 and 80 °C were used. As displayed in Figure 4.16, no significant change in reflection was observed for the different temperatures. The temperature was therefore set to 40 °C.

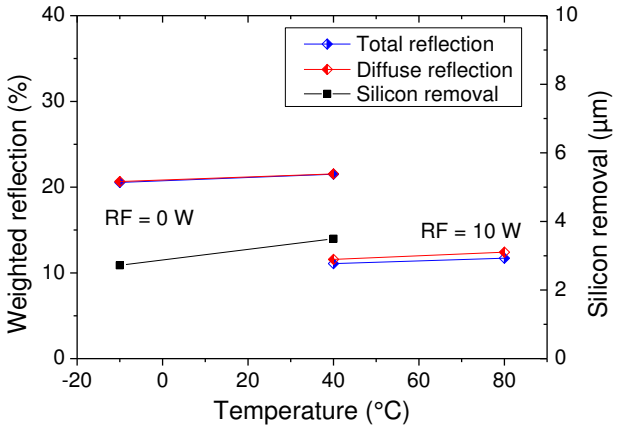

Figure 4.16: Weighted reflection and silicon removal for shallow and deep texture at different table temperatures.

The two optimized processes were investigated further in solar cells and will be referred to as “standard shallow texture” (process without additional RF power) and “standard deep texture” (process with 10 W RF power) due to the difference in structure depth which can be seen in SEM pictures in Figure 4.15. The parameters of the two texturing processes and of the textured samples are summarized in Table 4.2.

Table 4.2: Parameters of process and textured samples of standard shallow and deep texture in Plasmalab System 133.

Standard shallow texture

ICP power	RF power	Magnetic ring current	Temperature
1200 W	0 W	3 A	40 °C
SF_6 flow rate	O_2 flow rate	Pressure	Processing time
220 sccm	160 sccm	15 mTorr	15 min
Total reflection	Diffuse Share	Homogeneity (Grain/Area)	Silicon removal
19 %	> 98 %	2/1	3.5 µm

Standard deep texture

ICP power	RF power	Magnetic ring current	Temperature
1200 W	10 W	1 A	40 °C
SF6 flow rate	O2 flow rate	Pressure	Processing time
220 sccm	160 sccm	15 mTorr	15 min
Total reflection	Diffuse Share	Homogeneity (Grain/Area)	Silicon removal
11 %	> 95 %	2/2	4.5 µm

4.4.3 Selective plasma texturing

Selective texturing of a solar cell can be useful in different ways. It can simplify the cell process - by creating alignment keys during texturing, for example, or leaving the area below fingers untextured if the metallization is best applied on a flat or highly doped surface. The textures developed in this work show a selectivity between etching silicon and silicon oxide of 200 – 300 in the SI 600 and 26 – 35 in the Plasmalab System 133. This means the silicon oxide removal during a texturing process in the SI 600 is only 10 to 15 nm, while in the Plasmalab System 133 it is 100 to 170 nm, depending on the applied process. In combination with an epitaxially grown emitter, the formation of a selective emitter in situ with plasma texturing is possible. Profile and thickness of an epitaxially grown emitter are freely adjustable [46], consequently its thickness can be adapted to exceed the silicon removal of the texture and the area below the fingers can be masked by silicon oxide. During plasma texturing, the highly doped part of the emitter is removed, leaving a lowly doped emitter on the cell area while the area beneath the fingers still exhibits a high surface doping to enable contact formation. In Figure 4.17, a SEM picture of a contact on a selectively textured solar cell is shown. The 3 µm step of the texture can be seen as well as the remaining highly doped emitter area, where the finger is contacting the solar cell.

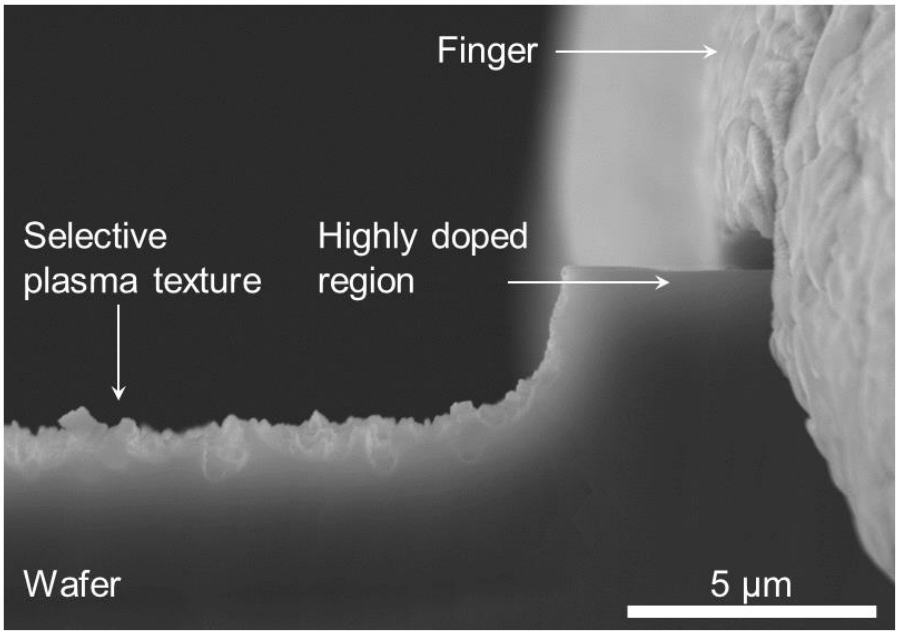

Figure 4.17: SEM picture of the selective plasma texture at a contact. The thick emitter was etched back by plasma texturing in the areas between the fingers, [46].

4.5 Plasma textured solar cells

Texturing of solar cells is always a compromise between improved reflection and increased surface recombination. Textures with a high aspect ratio have the best optical properties, but are often difficult to passivate [39]. Therefore the optimum between optical and electrical properties in the solar cell needs to be found.

To characterize the plasma texture further, wafer solar cells and crystalline silicon thin-film solar cells were processed.

4.5.1 Wafer solar cells with SI 600 texture

Wafer solar cells with 0.5 Ωcm, p-type FZ material were processed. All wafers have a laser fired contact (LFC) rear side (RS) with atomic layer deposited (ALD) Al_2O_3 and plasma enhanced chemical vapor deposited (PECVD) SiO_x. A schematic of the cell structure can be found in Figure 4.18. The cell batch was divided into three groups, one with plasma textured front side (FS), one with inverted pyramid texture and one with a planar front side. Two different plasma texturing processes were chosen for this cell batch using the standard SI 600 process with electrode height of 70 mm and 90 mm. The processing sequence can be seen in Figure 4.19. After a cleaning step the wafers were thermally oxidized and the silicon oxide was structured on the front side. The alignment keys were defined in the structuring step and shaped in the subsequent etching step. For the plasma textured group the structuring also defined the cell area, as 7 cells with an area of 4 cm² were processed on one 4 inch wafer. For the group with inverted pyramids, a structured oxide is necessary to form the pyramids in the etching step, consequently the oxide of the planar cells as well as the inverted pyramid cells had to be structured again to define the cell area before phosphorous diffusion. The residual silicon oxide was etched after $POCl_3$ diffusion, which formed a 120 Ω/□ emitter. As a front surface passivation and anti-reflective layer, a 105 nm thick silicon oxide layer was thermally grown and etched on the rear side. Subsequently, the Al_2O_3/SiO_x passivation stack was deposited and the Al evaporated on the rear side. The front side was contacted by a Ti/Pd/Ag front side grid. Finally, LFCs were formed and the cells were annealed.

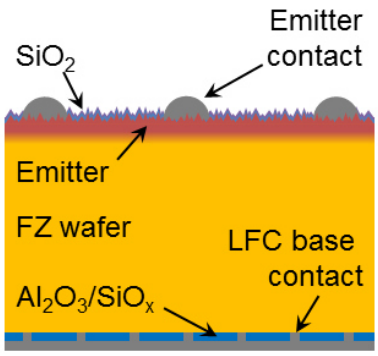

Figure 4.18: Schematic of the cell structure for wafer solar cells with SI 600 texture and LFC contacts.

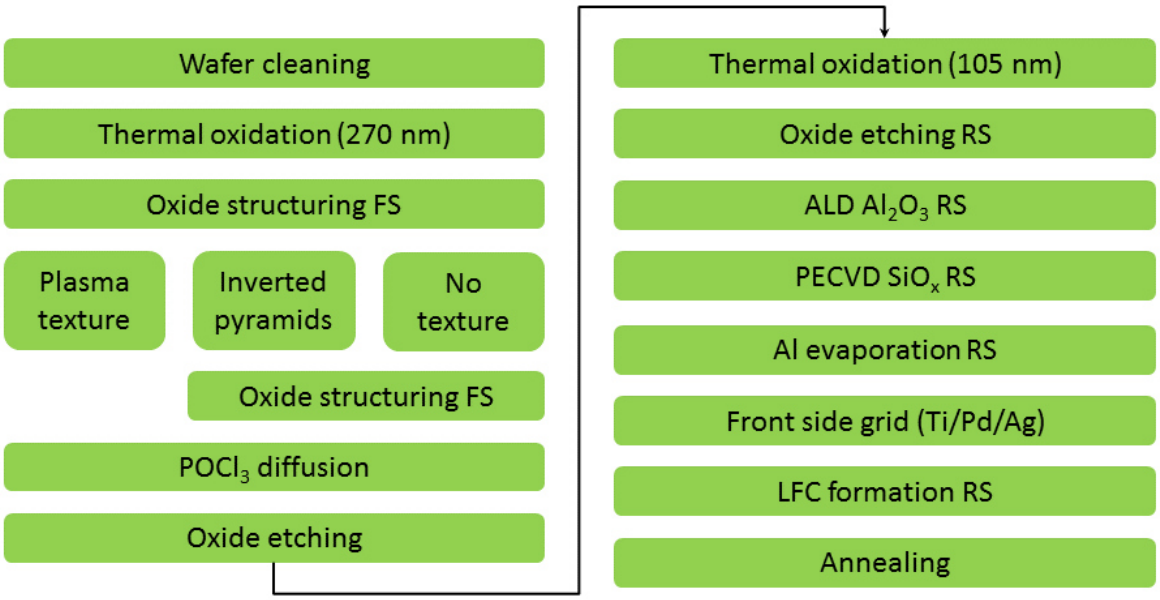

Figure 4.19: Processing sequence of wafer solar cells with laser fired contact (LFC) rear side (RS) and plasma texture, inverted pyramid texture or planar front side (FS).

The solar cell parameters of the cell batch can be found in Table 4.3. The average values are obtained from 21 cells for planar and plasma textured cells and from 84 cells with inverted pyramids. No distinct difference can be seen between the two plasma texturing processes. Comparing the average cell data, a slightly higher V_{OC} but slightly lower J_{SC} can be seen for an electrode height of 90 mm compared to a height of 70 mm. This supports the proposition that the structures become deeper with lower electrode height. The plasma textured cells exhibit a significantly decreased V_{OC} compared to planar and inverted pyramid textured cells. This can be attributed to the increased surface area compared to planar cells and smaller not only <111> oriented structures compared to inverted pyramid textured cells. An increased J_{SC} is visible for plasma textured cells compared to planar cells due to the lower reflection (see Figure 4.20). Inverted

pyramid textured cells have an even higher short circuit current and lower reflectance. The fill factor of the plasma textured cells is as high as that of the planar cells and the best inverted pyramid textured cells, which indicates a good contact formation. The plasma textured cells have in average the same efficiency as the planar cells as the decrease in V_{OC} levels out the increase in J_{SC}.

Table 4.3: Solar cell parameters of cells with planar and textured front side. Average of 21 cells and 84 cells for inverted pyramids.

Texture		**V_{OC} (mV)**	**J_{SC} (mA/cm²)**	**FF (%)**	**η (%)**
Planar	Average	673	32.9	79	17.5
	Best cell	675	33.2	80	18.0
Plasma texture	Average	652	34.2	79	17.6
(70 mm)	Best cell	651	35.0	80	18.1
Plasma texture	Average	655	33.6	80	17.7
(90 mm)	Best cell	646	35.5	80	18.4
Inverted pyramids	Average	665	37.6	74	18.3
	Best cell	670	38.3	79	20.4

The wavelength-dependent internal quantum efficiency (IQE) and reflection of the best cell of each group are displayed in Figure 4.20. In the short wavelength range below 500 nm the IQE of the plasma textured cell is only slightly reduced compared to the inverted pyramid textured cell and higher than the planar cell. This indicates a sufficient passivation of the front side despite the structuring. In the long wavelength range above 1100 nm the light-trapping effect of the plasma texture is slightly visible, but should be more pronounced in thin-film solar cells with a reflective rear side. The IQE of the plasma textured cell at around 1000 nm is reduced compared to the other two cells. This effect was also observed by Grötschel et al. [47] on cells with screen-printed aluminum rear side in combination with thermal oxidation after texturing. Although no definitive explanation for this phenomenon has been found, the effect did not show in thin-film solar cells or wafer solar cells with Al BSF (see section 4.5.2).

The presented cell batch shows that the developed plasma texture can be passivated with thermal oxide and induces light-trapping in cells with reflective rear side.

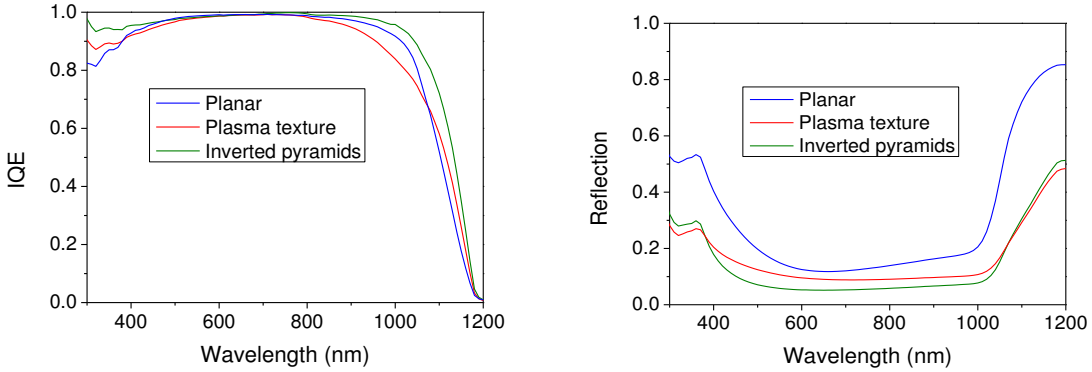

Figure 4.20: IQE (left) and reflection (right) of best cell with planar front side (blue), plasma texture (red) and inverted pyramid texture (green).

4.5.2 Thin-film solar cells with SI 600 texture

Crystalline silicon thin-film solar cells were processed as EpiWE with the sequence displayed in Figure 4.22. Highly doped (conductivity < 0.05 Ωcm) p-type mc and FZ wafers were used as substrates. A schematic of the solar cell structure is shown in Figure 4.21.

After pre-cleaning of the substrates, the active layer consisting of BSF and base was deposited epitaxially. P-type FZ wafers with 0.5 Ωcm conductivity were added to the cell process as wafer solar cell references. Half of the cells were plasma textured with an electrode height of 90 mm and a process pressure of 3 Pa while the other half was left planar. Aluminum was evaporated on the rear side before $POCl_3$ diffusion to form an Al BSF. A 10 nm oxide was thermally grown as passivation of the 120 Ω/□ emitter. As metallization, aluminum was evaporated on the rear and sintered before the front side grid consisting of Ti/Pd/Ag was evaporated and thickened by Ag plating. The cells were measured before and after the application and sintering of a DARC of TiO_x/MgF_x.

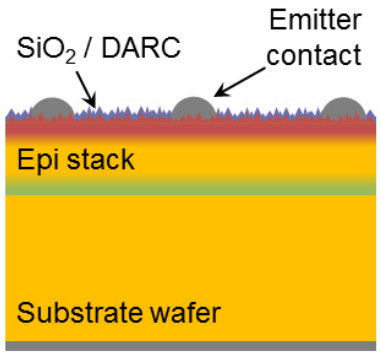

Figure 4.21: Schematical drawing of solar cell structure used for EpiWE cells with SI 600 texture.

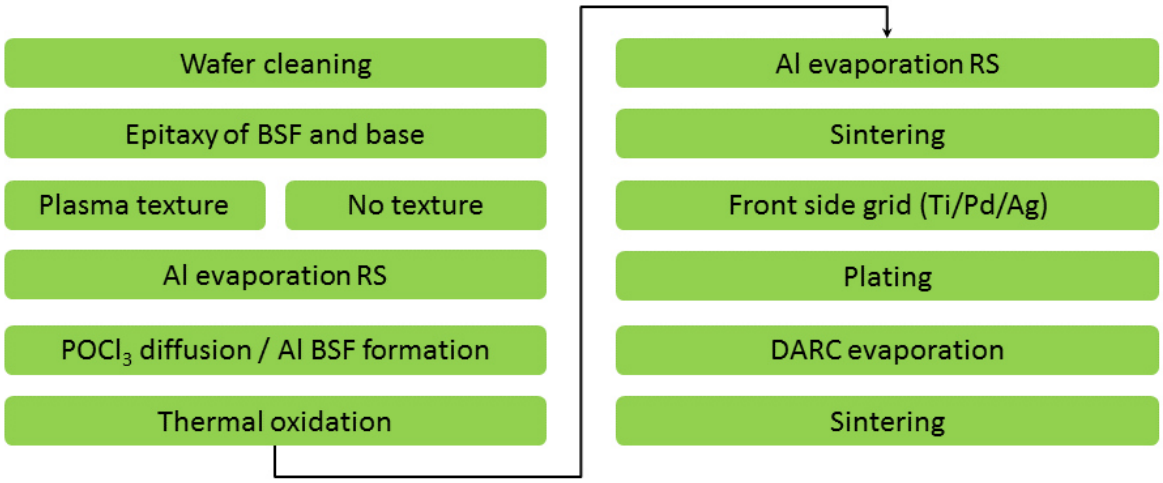

Figure 4.22: Processing sequence of EpiWE solar cells with and without plasma texturing.

The measured cell parameters were averaged for each group and can be found in Table 4.4. There were two cells per group for the reference cells and four cells per group for the EpiWE cells. It can be seen for all cells without DARC that textured cells have a higher J_{SC} than planar cells due to a lower reflection. The V_{OC} is in the same range for monocrystalline EpiWEs and the reference cells, and for multicrystalline the textured cells even have a higher V_{OC}. This leads to a higher efficiency for textured cells than planar cells. However, it should be noted, that for cells with a low J_{SC}, as the planar cells here, the J_{SC} can limit the V_{OC}.

After application of the DARC, the J_{SC} of the planar cells increases to at least the level of the textured cells. It can exceed the J_{SC} of the textured cells as the DARC is optimized for planar cells which results in a lower reflection for planar cells with DARC than textured cells with DARC, see Figure 4.23. With increased J_{SC} the V_{OC} of the planar cells also increases, as it is no longer limited by the J_{SC}. For the EpiWE on mc cells, the V_{OC} of the textured cells is as high as that of the planar cells. On EpiWE on FZ material it is reduced by less than 10 mV. The fill factor is slightly reduced only on textured monocrystalline EpiWE cells, while the reference cells and the multicrystalline EpiWE have the same fill factor on textured and planar cells.

The efficiency is reduced by approximately 1 % for textured monocrystalline EpiWE cells due to the decrease in J_{SC} and V_{OC}, while textured multicrystalline EpiWE cells show the same cell parameters including efficiency as planar ones.

Table 4.4: Solar cell parameters of reference wafer cells and EpiWE cells on FZ and mc substrates. Values are averages of four cells in the case of EpiWE cells and of two cells for the FZ references.

		DARC	V_{oc} (mV)	J_{sc} (mA/cm²)	FF (%)	η (%)
Reference	Textured	No	626	30.7	79	15.2
	Textured	Yes	630	33.3	80	16.6
	Planar	No	628	24.8	80	12.5
	Planar	Yes	636	35.3	79	17.7
FZ – EpiWE	Textured	No	630	31.1	74	14.4
	Textured	Yes	632	34.1	74	15.9
	Planar	No	629	24.3	77	11.7
	Planar	Yes	640	35.2	76	17.1
mc – EpiWE	Textured	No	597	26.0	76	11.7
	Textured	Yes	600	28.3	75	12.7
	Planar	No	588	20.2	76	9.0
	Planar	Yes	599	28.7	75	12.9

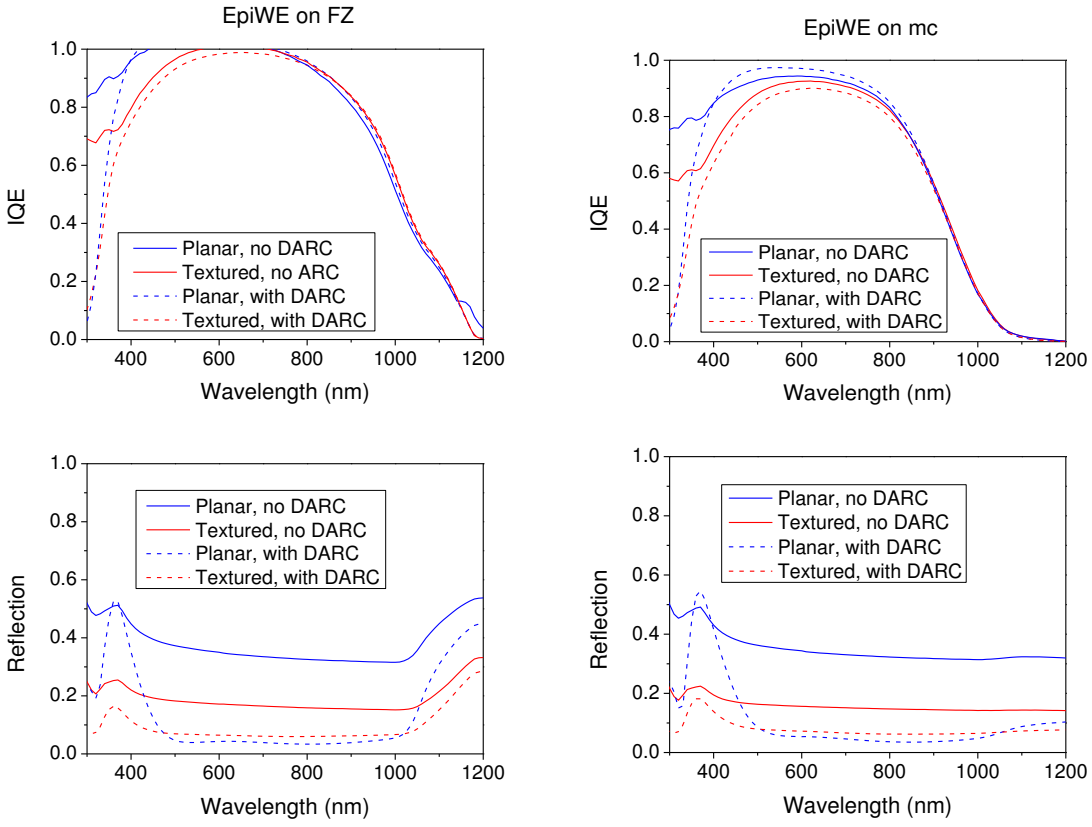

Figure 4.23: IQE and reflection of planar (blue) and textured (red) EpiWEs on FZ and mc material before (solid line) and after (dashed line) DARC application.

Figure 4.23 shows IQE and reflection of EpiWE cells before and after application of the DARC. The IQE of the EpiWE on FZ cells shows a hump above 1000 nm. This represents a contribution of the substrate to the cell current and means the FZ substrates were not sufficiently high doped.

A decrease in the short wavelength range of the IQE can be seen for the textured cells before DARC evaporation. This indicates insufficient passivation of the front side, which leads to a high surface recombination velocity. No light-trapping effect can be seen in the long wavelength range as no rear side reflector was implemented.

As expected, the reflection of the textured cells before application of the DARC is considerably lower than that of the planar cells. The DARC lowers the reflection of both, but as it is optimized for planar surfaces the planar cells with DARC have a lower reflection than the textured ones in the range between 500 and 1000 nm. EpiWE on mc cells do not show an escape peak above 1000 nm, because the light is absorbed in the highly doped substrate. As the substrate of the EpiWE on FZ cells is not as highly doped, it does not absorb the light with wavelengths above 1000 nm, which is then reflected on the rear side of the cell and an escape peak is visible.

In summary, the developed plasma texture leads to a reflection as low as 7 % on epitaxially grown thin-film solar cells with DARC with only a small loss in V_{OC} in monocrystalline EpiWE cells and no V_{OC} loss in multicrystalline EpiWE cells. A decrease in IQE of the textured cells in the short wavelength range was observed. As this effect was not observed in the wafer solar cell batch with 105 nm thick silicon oxide passivation discussed in 4.5.1, it stands to reason that a silicon oxide layer thicker than 10 nm is required.

As the texture considerably lowers the reflection, a SiN_x single layer anti-reflective coating should provide for a sufficiently low reflection on textured cells. Substituting the DARC with a single layer TiO_x was tried in cell batches with textures from the Plasmalab System133 and will be shown in 4.5.4.

4.5.3 Thin-film solar cells with rear side reflector and SI 600 texture

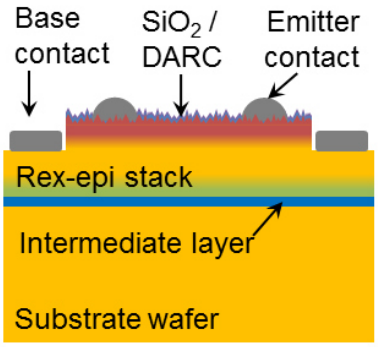

Figure 4.24: Schematical drawing of the recrystallized wafer equivalent solar cell structure.

Recrystallized wafer equivalent (RexWE) solar cells were fabricated with different intermediate layers (IL). A front side contacted metallization scheme was chosen with nine 1 x 1 cm² cells on one 5 x 5 cm² wafer, see Figure 4.24 for a sketch of the RexWE cell structure and Figure 4.25 for the processing sequence.

After fabricating the recrystallized seed layer, which also acts as BSF, the base was epitaxially deposited. Wafers were thermally oxidized and the oxide structured before texturing in a plasma process or KOH. The oxide was used as mask, so only defined cell areas were textured. The $POCl_3$ diffused 120Ω/□ emitter was passivated with a 10 nm thick thermal oxide. Emitter and base contact were both formed by a lift-off process on the front side and a DARC was applied.

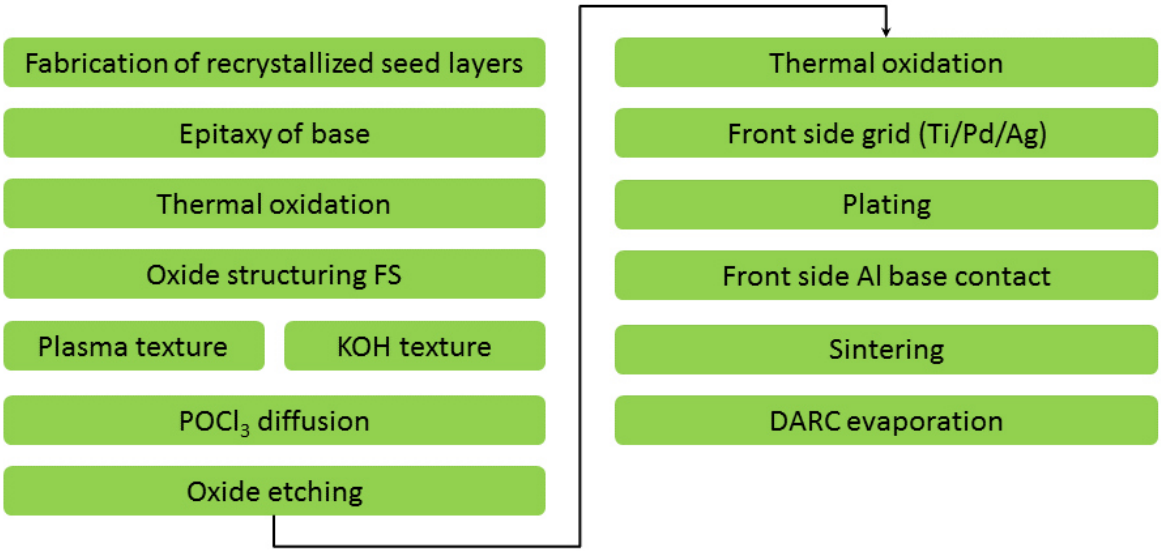

Figure 4.25: Processing sequence of RexWE solar cells on different IL.

The influence of the IL can be seen in Figure 4.26 on the left. IQE and reflection of plasma textured cells with SiO_2 and SiC intermediate layer are displayed. As the SiC absorbs nearly all light, there is no escape peak above 1000 nm in the reflection and the IQE is considerably lower above 600 nm than the IQE of the cell with SiO_2 IL. This light-trapping effect leads to an increased J_{SC} from 23 mA/cm² to 27 mA/cm² for the cells with SiC IL and SiO_2 IL respectively. In Figure 4.26 on the right IQE and reflection of cells with SiO_2 IL and plasma or KOH texture are shown. It should be mentioned that the KOH textured RexWE cell was fabricated in another cell batch, but with the same cell structure. The lower escape peak of the plasma textured cell in combination with an increased IQE in the long wavelength range compared to the KOH textured cell indicates a better light trapping of the plasma texture.

In this cell batch it was shown that the developed plasma texture not only reduces reflection but in combination with a reflective rear side leads to light-trapping in thin-film solar cells.

4.5.4 Wafer solar cells with Plasmalab System 133 deep and shallow texture

Wafer solar cells with the deep and shallow texture of the Plasmalab System 133 described in 4.4.2 and shown in Figure 4.15 were processed in a sequence displayed in Figure 4.27. It is very similar to the one used for thin-film cells with texture of the SI 600 (see section 4.5.2). As material 0.5 Ωcm p-type FZ wafers were used to fabricate 4 cm² cells. A schematic of the cell structure is shown in Figure 4.28.

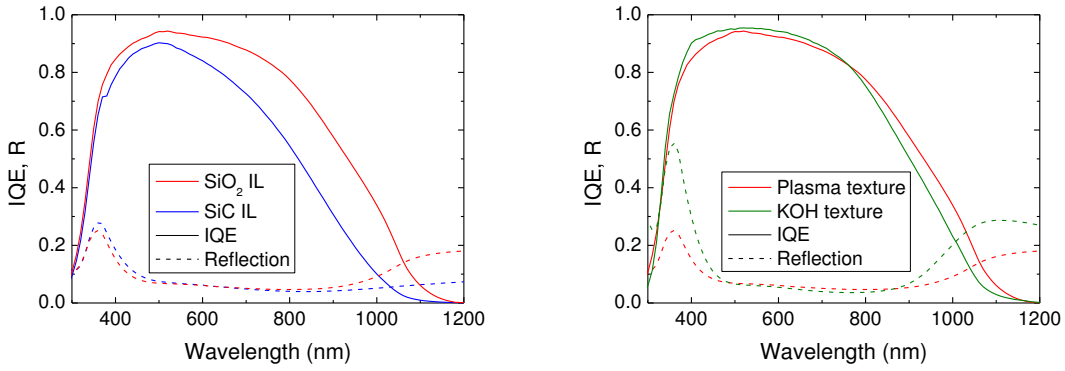

Figure 4.26: Reflection and IQE of plasma textured RexWE cells with SiO_2 and SiC intermediate layer (IL) on the left and RexWE cells with SiO_2 IL with plasma and KOH texture on the right.

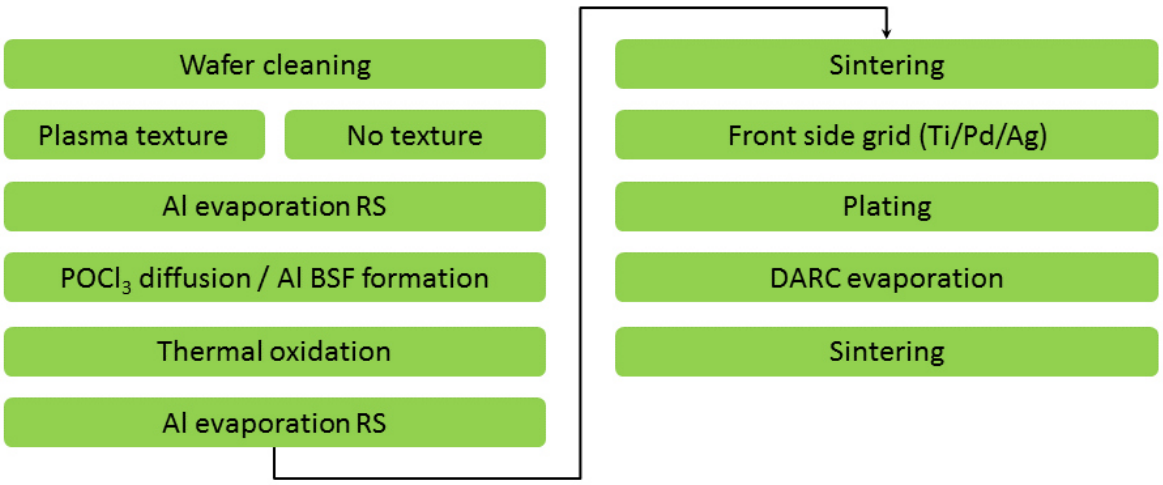

Figure 4.27: Processing sequence of wafer solar cells with deep and shallow texture of Plasmalab System 133.

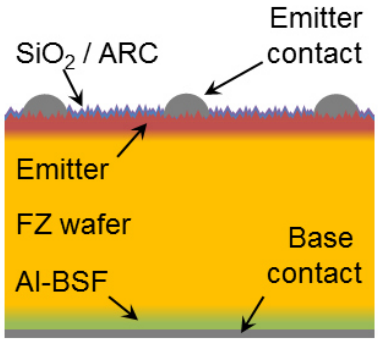

Figure 4.28: Schematical illustration of cell structure of wafer solar cells with Plasmalab Systems 133 texture.

The cells were measured before and after application of the DARC. The parameters of the best cell of each group are listed in Table 4.5. The best planar cell before deposition of the DARC was not the best cell of this group afterwards, therefore the best cell after DARC application is listed additionally. Examining the cells before DARC evaporation, the difference in J_{SC} can be seen. The deep textured cell has a 3 mA/cm² higher J_{SC} than the shallow textured cell, which still has a by 5 mA/cm² higher J_{SC} than the planar cell. The reflection measurements in Figure 4.29 prove that this is due to a reduced reflection of the textured cells. The IQE is also displayed in Figure 4.29. In the long wavelength range a very slight increase can be seen for the textured cells. In cells with a rear reflector this effect is more pronounced, see section 4.5.5. In the short wavelength range the shallow texture exhibits a high IQE indicating a well passivated front surface, while the IQE of the deep textured cells drops below that of the planar cells. The insufficient passivation affects the V_{OC}, which is higher in the shallow textured cells than the

deep textured cells. The even lower V_{OC} of the planar cells is limited by the low J_{SC} and, after application of the DARC, when it is no longer limited by a low J_{SC}, increases to the level of a shallow textured cell before DARC application.

Due to the DARC, the reflection between 500 and 900 nm is reduced to the same level for textured and planar cells even though it is optimized for planar surfaces. Nevertheless, the planar cells have a low J_{SC} compared to usual results with this processing sequence. The reference cells discussed in section 4.5.2 were processed the same way and show similar cell parameters before application of the DARC but considerably higher ones after DARC evaporation. The IQE is also reduced after application of the DARC (Figure 4.29).

Table 4.5: Solar cell parameters of best wafer solar cell of each group before and after application of DARC. In the group of planar cells, the best cell after DARC was a different cell than before, it is therefore also listed.

	DARC	**V_{OC} (mV)**	**J_{SC} (mA/cm²)**	**FF (%)**	**η (%)**
Planar 1	No	624	25.5	79	12.5
	Yes	628	29.3	78	14.4
Planar 2	Yes	631	31.4	78	15.4
Shallow texture	No	630	30.4	79	15.1
	Yes	633	35.5	79	17.6
Deep texture	No	627	33.1	79	16.4
	Yes	627	34.6	79	17.0

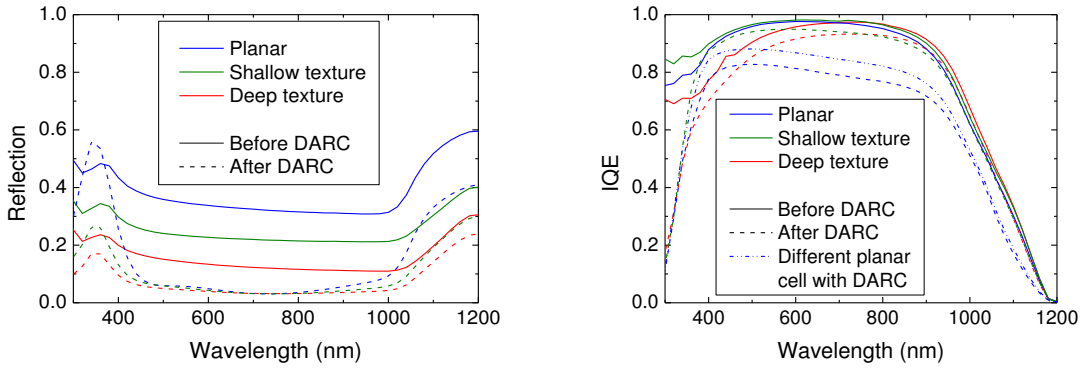

Figure 4.29: Reflection (left) and IQE (right) of the best wafer solar cells of each group before (solid line) and after (dashed line) DARC application.

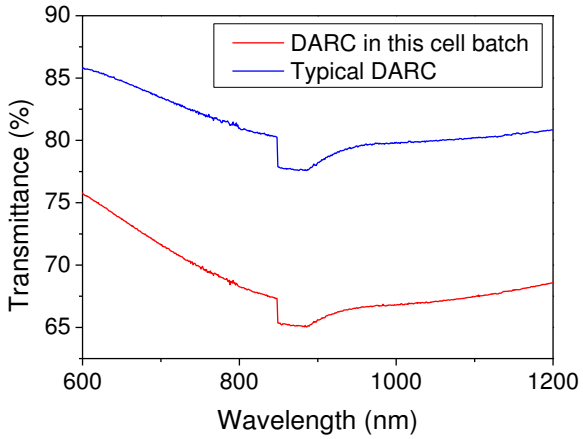

Figure 4.30: Transmittance of DARC in a typical case (blue) and in this cell batch (red).

To explain this difference, in Figure 4.30, the transmittance of the DARC in this cell batch and of a typical DARC are shown. A strong decrease in transmittance can be observed for the DARC of this cell batch, which causes the low J_{SC} and hence the low efficiency of the planar cells compared to other cell batches. The higher absorption of the DARC affects the textured cells as well. Although the IQE is not as much decreased due to the DARC for the textured cells as for the planar cells, a higher efficiency is to be expected for cells with less absorbing DARC.

In a second batch, which was already presented in [45] and [48], cells were processed with a single layer anti-reflective coating (SARC) of 50 nm TiO_x in an otherwise identical fabrication process. After cell characterization, the second layer of the DARC stack (105 nm MgF_x) was applied and the cells measured again.

The IV parameters of the best solar cell of each group are summarized in Table 4.6. With SARC, the J_{SC} of the shallow textured cell is in the same range as of the deep textured cell and 3 mA/cm² larger than the J_{SC} of the planar cell. This can partly be attributed to a slight light-trapping effect and partly to decreased reflection (see Figure 4.31). The reflection measurements show that a planar surface with SARC exhibits a clear reflection minimum near 600 nm while textured surfaces show a reflection reduction over a larger wavelength range. After application of MgF_x the reflection is further reduced especially for planar cells, as can be seen in Figure 4.31. As the difference in reflection is minimized the spread of J_{SC} values is narrowed (see Table 4.6).

A slight trend of V_{OC} reduction with surface roughness can be observed. Comparing the planar cell to the deep textured cell the V_{OC} after DARC application differs by 4 mV, while the J_{SC} is 0.7 mA/cm² higher for the textured sample.

Additionally, the IQE (Figure 4.31) decreases slightly in the short wavelength range for the deep textured cell as in the previous cell batch. The decrease again indicates that the deep texture was not optimally passivated, which fits well to the slightly decreased V_{OC}.

The improvements in J_{SC} and a high V_{OC} and fill factor lead to an increase in efficiency of 1.8 and 0.8 % abs. for the shallow textured cell with SARC and DARC, respectively. The deep textured cell shows an efficiency gain of 1.6 and 0.4 % abs. with SARC and DARC. Due to the increased absorption of the DARC in the first cell batch no further conclusions can be drawn from a comparison of the two batches.

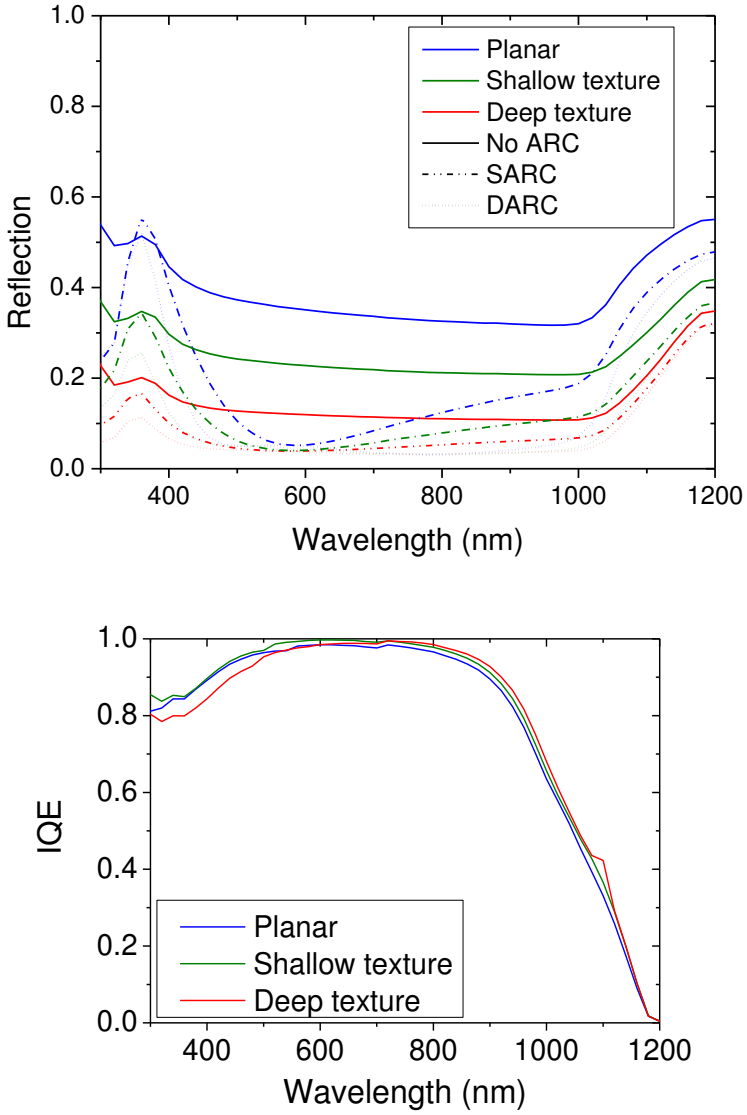

Figure 4.31: Reflection without ARC and with SARC and DARC (above) and IQE without ARC (below) of the best wafer solar cell of each group.

Table 4.6: IV parameters of best wafer solar cell of each group with SARC and DARC.

Best wafer cell	ARC	V_{OC} (mV)	J_{SC} (mA/cm²)	FF (%)	η (%)
Planar	SARC	635	32.2	78	16.0
	DARC	636	35.9	78	17.7
Shallow textured	SARC	635	35.5	80	17.8
	DARC	634	36.8	79	18.5
Deep textured	SARC	633	35.6	78	17.6
	DARC	632	36.6	78	18.1

4.5.5 Thin-film solar cells with Plasmalab System 133 deep and shallow texture

To show the full potential of the texture, thin-film solar cells on silicon on insulator (SOI) wafers with epitaxially deposited active layer were fabricated in the processing sequence shown in Figure 4.32. On 5 x 5 cm² wafers 9 cells of 1 x 1 cm² were manufactured. The SOI wafers with 1.5 µm silicon film on 1 µm thick silicon oxide layer were cleaned and the active layer was deposited epitaxially. As the oxide layer insulates the active layer from the substrate, the SOI wafers can only be contacted on the front side. Figure 4.33 shows a schematical drawing of the fabricated cell structure.

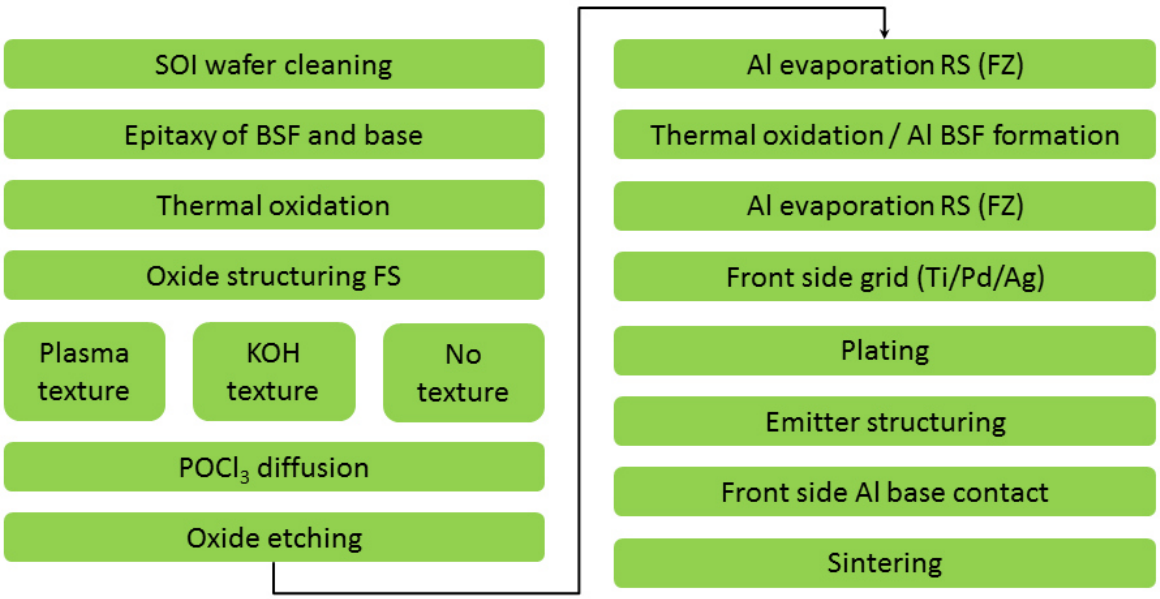

Figure 4.32: Processing sequence of crystalline silicon thin-film solar cells with plasma texture on SOI wafers.

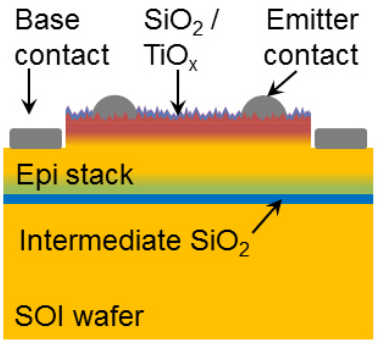

Figure 4.33: Schematic of epi on SOI wafer cells with plasma texture.

The used structure of cells with the base contact surrounding the 1 x 1 cm² cells leads to a similar situation as with iSiMo. In accordance with the simulations done for the integrated interconnected structure (see 3.3.3) a thick BSF of 15 µm with doping of 1 x 10^{18} cm^{-3} and a base of 20 µm with a doping of 4 x 10^{16} cm^{-3} was chosen. All wafers were thermally oxidized and the oxide structured before texturing to act as mask in order to only texture the cell areas. Four groups were formed, with a planar surface, the shallow plasma texture, the deep plasma texture and a reference with KOH texture. The epitaxially grown layer thickness was increased by 10 µm for cells in the KOH textured group to account for the larger silicon loss during texturing. A $POCl_3$ diffusion formed an 120 Ω/□ emitter which was passivated by a 10 nm thick thermally grown oxide. After forming the front side grid in a photolithographic lift-off process and Ag plating the emitter was structured in a plasma etching process using photolithographically structured photoresist. The process for emitter structuring is explained in more detail in section 5.2.1, as it was also used in the fabrication of integrated interconnected thin-film modules. The front side Al base contact was also applied in a lift-off process and the cells sintered afterwards.

Cells of this batch exhibit a reduced V_{OC} and FF, which can be traced back to an elevated J_{02}. Traps in the space charge region e.g. due to in-diffusion of contaminants can cause an increase in J_{02}. As all cells independently of the surface structure have the J_{02} issue, it is not related to the plasma texturing process and will therefore not be discussed here. The reduced V_{OC} and FF of course cause very low efficiencies of nearly 10 %. The influence of the different textures on J_{SC}, IQE and reflection can nevertheless be discussed. The J_{SC} values for one cell of each group is summarized in Table 4.7 and the corresponding reflection and IQE measurements can be found in Figure 4.34. The reflection is, as

in previously discussed cell batches, reduced for the plasma textured cells. The reflectance of the KOH textured cell lies between the reflectance of shallow and deep texture, but shows a higher escape peak. In the IQE the light-trapping effect of all textures is clearly visible in the long wavelength range. The deep texture has a larger light-trapping effect than the shallow texture, but is still exceeded by the KOH texture. In the short wavelength range the IQE is drastically reduced for the deep textured cell. The drop in IQE was confirmed for another deep textured cell as well. Previously discussed cells with the same texture did not show this effect as strongly and the origin of it is not yet known. The idea, that parameters during the plasma etching process were not stable, was proven wrong for at least the monitored parameters. Another reason could be the passivation layer, which consists of 10 nm thermally grown SiO_2. The thickness of the oxide cannot easily be measured on textured surfaces and was checked on a planar planar reference by ellipsometry. It is easily conceivable that the thickness varies depending on the texture and its surface area. Therefore an optimization of the surface passivation could enhance the performance of the plasma textures. Nevertheless a resulting increase in J_{SC} was observed for all textured cells. Despite the drop in IQE in the short wavelength range, the deep texture leads to a higher J_{SC} than the shallow texture. The J_{SC} of the KOH textured cells still exceeds that of the deep texture due to better performance in light-trapping as well as front side passivation.

Table 4.7: J_{SC} of one cell of each group (planar, shallow textured, deep textured and KOH textured) of the epi on SOI cells.

Cell	**J_{SC} (mA/cm²)**
Planar	20.2
Shallow texture	27.2
Deep texture	28.0
KOH texture	31.0

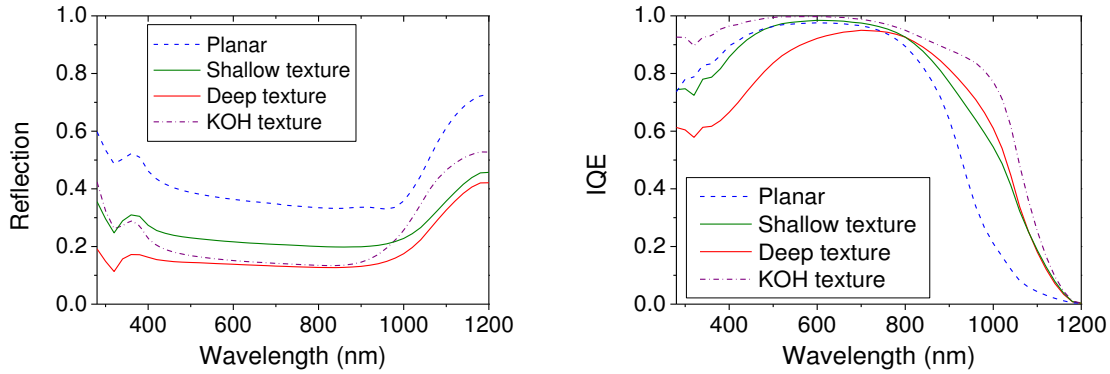

Figure 4.34: Reflection (left) and IQE (right) of fabricated epi on SOI solar cells without texture, with the shallow and deep plasma texture and KOH texture.

4.6 Summary

The absorber of crystalline silicon thin-film solar cells only absorbs a fraction of the incoming light, which can be increased by elongation of the optical path length through the implementation of light trapping. To introduce light trapping a plasma textured front side in combination with a reflective rear side was used. The developed plasma texturing processes meet the requirements of epitaxially grown multi- and monocrystalline silicon thin-film solar cells: The texturing process has little silicon removal, below 5 µm. Also, texture formation occurs on saw damage free surfaces, which was ensured by using either epitaxially thickened wafers or wafers that were chemically polished to remove the saw damage. Lastly, it was verified by reflectance measurements and SEM analysis that the texture forms independently of the grain orientation.

Texturing processes were developed in two different etching tools in a self-masking process based on SF_6, O_2. In the SI 600 the plasma was sustained by MW excitation, while a combination of CCP and ICP was used in the Plasmalab System 133, forming hemispherical structures with a reflection of approx. 7 – 20 %, depending on the process.

For the SI 600 textures, wafer solar cells with reflective rear side and ARC could be improved slightly by the application of the texture. For multicrystalline EpiWE cells, the textured cells showed the same efficiency as planar solar cells. In RexWE cells with reflective intermediate layer the plasma texture lead to light-trapping and therefore an increased cell performance compared to planar cells.

The plasma textured cells from the Plasmalab System 133 performed better than planar cells in case of wafer as well as thin-film solar cells. It was shown that

the texture not only reduces reflection but also permits light-trapping due to oblique in-coupling of light. In thin-film solar cells on SOI wafers light trapping lead to an increase in J_{SC} from 20.2 mA/cm² for planar cells to 27.2 mA/cm² and 28.0 mA/cm² for cells with shallow and deep texture respectively. The use of a single layer anti-reflective coating in combination with the plasma texture proved very effective in reducing the reflection over a broad wavelength range and lead to an increase in efficiency for wafer solar cells with shallow texture of 1.8 % abs. compared to planar cells. The application of commonly used PECVD SiN_x was not yet tested but is expected to achieve similar results.

Although only small area solar cells up to 4 cm² were fabricated, the texturing processes in the Plasmalab System 133 were optimized for 156 x 156 mm wafers. They can not only be applied to thin-film solar cells but could also be an alternative for multicrystalline wafer solar cells instead of wet chemical texturing. As plasma texturing is a single side process, it is most convenient to be combined with advanced rear side concepts that require a planar rear surface.

5 SILICON STRUCTURING

The iSiMo concept requires different silicon structuring processes whose realization is the subject of this chapter. Structuring processes such as waterjet guided and dry laser structuring or masking combined with wet chemical or plasma etching are evaluated in relation to their application.

In most standard wafer solar cells silicon structuring is done for edge isolation and can be avoided in some cases through application of a diffusion barrier. In other solar cell concepts additional structuring of silicon can be necessary, e.g. in selective emitter solar cells, single side contacted solar cells or integrated interconnected thin-film cells.

Two silicon structuring steps are included in the processing sequence for iSiMo modules. One is the separation of the cell strips and the other the structuring of the emitter.

5.1 Separation of cell strips

The silicon thin-film must be divided into cell strips that can be interconnected. The 20 to 30 µm thick silicon layer has to be completely separated to ensure electrical isolation. Compared to structuring steps in other cell concepts, where the emitter is often structured, this is a rather deep structuring. Here, two approaches will be discussed: One for a laboratory scale realization including wet chemical etching of silicon and one for industrial implementation with laser structuring. In the mini-modules, which were fabricated in the frame of this thesis, the laboratory process was used.

5.1.1 Laboratory realization

As a laboratory process for cell strip separation, trenches were etched using a KOH etch and silicon oxide as a mask. The processing sequence is displayed in Figure 5.1.

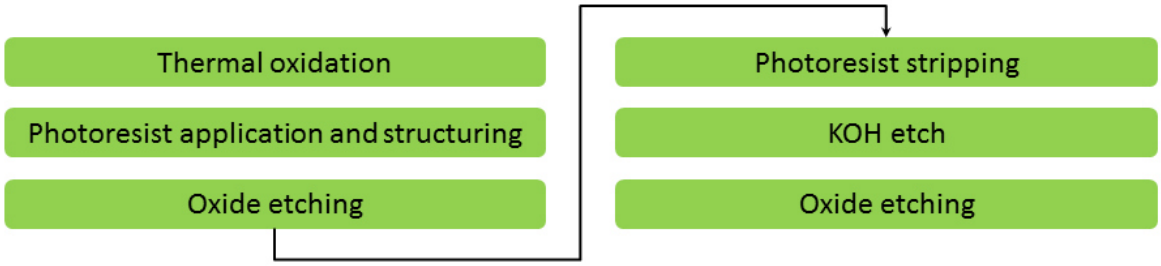

Figure 5.1: Processing sequence for trench etching with KOH through a silicon oxide mask.

An approximately 280 nm thick silicon oxide layer was thermally grown on the silicon surface and structured with a photolithography process that used a positive resist, which means the exposed part of the resist is removed during its development. The structuring itself was done in SiO etch, a buffered HF solution, where 10 µm wide lines were opened. After stripping the resist, the trenches were etched with 8 % aqueous KOH at 80 °C using the SiO_2 as mask, which formed trenches approximately 120 µm wide. The layer below the silicon film should be either an etch stop for KOH or exhibit a much slower etch rate than silicon. In the case of the SOI wafers the intermediate oxide fulfilled this requirement.

In Figure 5.2 microscopy pictures of samples with structured photoresist after oxide etching can be seen. In a), b) and c) the photoresist was structured as intended, opening lines of approximately 10 µm. In a), the oxide was only etched where the photoresist was removed and in b), an undercut parallel to the resist opening can be seen, which can result in wider trenches after KOH etching. The excessive undercut in c) is already wider than the targeted final trench width and originates from insufficient adhesion of the resist on the wafer. Circular or semi-circular shaped defects in the resist are so called mouse bites that form due to overexposure of the photoresist and can be seen in d).

The structure of the oxide can be seen more clearly after stripping the resist. A nicely shaped oxide opening can be seen in Figure 5.3 a). Mouse bites, undercut or a combination of both lead to frayed openings as in Figure 5.3 b) and c). To etch uniform trenches with KOH, defects such as this must be avoided.

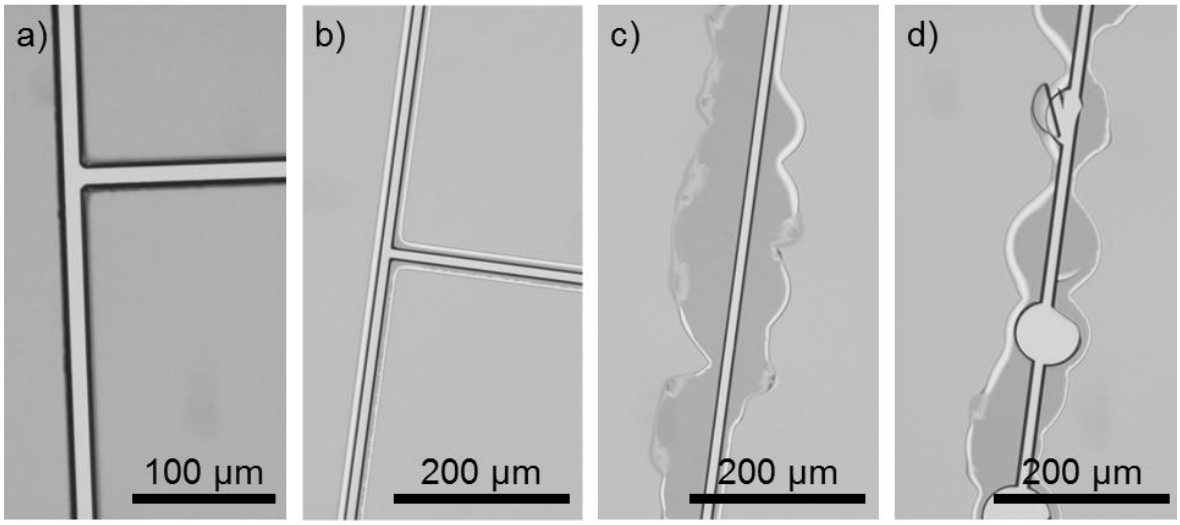

Figure 5.2: Microscopy pictures of samples with structured photoresist after etching the silicon oxide. The photoresist was structured as intended in a), b) and c). No undercut after oxide etching can be seen in a). In b) undercut parallel to the resist opening is visible, while in c) excessive undercut can be seen. Mouse bites and excessive undercut are shown in d).

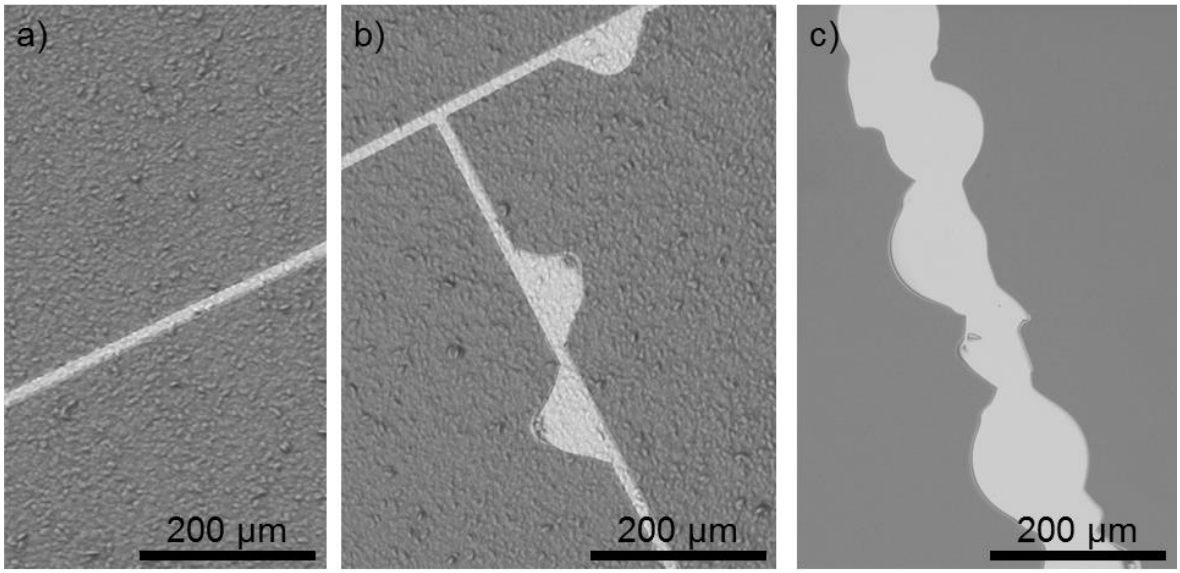

Figure 5.3: Micrsocopy pictures of samples with structured silicon oxide. In a) oxide is structured as intended. Mouse bites, undercut or both lead to bulged openings in b) and c)

According to [49] the etch rate of <100> oriented silicon surfaces in aqueous KOH is maximal at a KOH concentration of around 20 % aqueous KOH and can be increased by increasing the temperature. The etch rate of thermally grown SiO_2 is smaller by some orders of magnitude but rises steeply with increasing KOH concentration up to its maximum between 30 and 40 % KOH concentration and also increases with increasing temperature. A KOH concentration of 8 % was chosen to reduce the oxide etch rate and keep the silicon etch rate high. As already discussed in section 4.1.1, the anisotropic KOH etching depends on

crystal orientation. The <111> surface has the slowest etch rate in KOH, which is why the slopes of the trenches are confined by <111> planes. On SOI wafers the intermediate oxide layer acts as an etch stop. Therefore the formed trenches have a flat bottom and <111> oriented slopes. Over-etching leads to a thinning of the intermediate oxide and a widening of the trench. The thinning of the oxide as well as the influence of too wide trenches will be discussed later in chapter 6 on interconnection.

Highly boron doped (> 10^{19} cm^{-3}) silicon exhibits a slower etch rate [50] and a highly doped BSF can therefore lead to longer etching times. As the BSF doping concentration used in the frame of this thesis was not as high, this effect did not have to be taken into account.

The samples were etched for approximately 60 min and the etch depth of the trenches had to be monitored by microscopy, as they were not etched totally homogeneously. A partly etched trench can be seen in Figure 5.4. The bottom of the trench shows the typical KOH etched silicon structure with small pyramid stumps as long as the trench is not fully etched. When the silicon layers gets very thin interference effects can be observed and when only the intermediate oxide layer is left it does not show any structure at all. These features made it possible to see if the cell strips were fully separated.

This method of cell strip formation worked well for the laboratory process on SOI wafers, but would not be applicable to multicrystalline material because of the anisotropic etching of KOH. The process is also very sensitive to defects in the resist and masking oxide – a scratch in either of them leads to a hole in the cell. As the emitter is diffused later in the process these do not induce shunts, but reduce the active cell area.

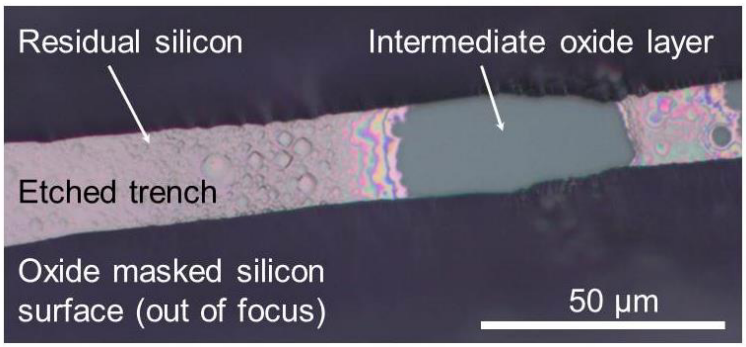

Figure 5.4: Microscopy picture of a partly etched trench. On the left silicon can be seen in the trench, exhibiting a typical KOH etched structure. Where the silicon was completely etched only the smooth grey intermediate oxide layer is visible.

5.1.2 Industrial realization

The laboratory approach with the photolithography process and oxide as masking layer is not feasible for industrial realization. Alternatively experiments with waterjet guided laser and dry laser were done. In the liquid jet guided laser principle, which was patented by Synova S.A. [51], a thin fluid jet is formed through a nozzle and the laser beam focused to be coupled into that fluid jet. Water was chosen as fluid in this case and a laser from Spectra Physics with a wavelength of 532 nm and a pulse duration of 15 ns. The used dry laser with a wavelength of 355 nm and a pulse duration of 10 - 12 ps from InnoLas Systems is usually used for laser edge isolation.

Recrystallized and epitaxially thickened silicon wafers on SiC encapsulated graphite substrates were used for all laser experiments. The RexWE layers had thicknesses ranging from 17 to 30 µm over a sample caused by varying growth rates on different grain orientations and inhomogeneity of the CVD process. To account for these inhomogeneities and because first experiments showed residual silicon in the trenches a subsequent etch step was implemented. The subsequent etch step also removes laser induced damage. According to Baumann et al. [52] a waterjet guided laser induces much shallower damage than a standard laser system, but to ensure high electric quality of the silicon this damage should still be etched. KOH and plasma etches were used for this purpose.

Waterjet guided laser

The trench depth of the waterjet guided laser was adjusted by varying the internal laser power, the frequency of the laser pulses and the scanning velocity. For the waterjet a nozzle of 50 µm was chosen and the pressure was set to 150 bar. In first experiments the internal laser power was set to 43 and 86 % of the possible internal laser power, which corresponds to 4.5 and 9.0 W. The pulse frequency was set to 50 kHz, the speed was varied between 20 and 100 mm/s and one and two passes were lasered to form a trench. It was found that a laser power of 86 % was too high and removed the SiC layer at least in most cases. In the subsequent experiment, the laser power was set to 43 % and one, two and three passes were lasered, otherwise with the same parameters as before. The trench depth in dependence of the scanning speed can be seen in Figure 5.5. The light grey area indicates laser parameters that damaged the SiC layer, but did not

create holes in it. Parameters in the dark grey area lasered through the SiC layer into the graphite substrate. It can be seen that for slow scanning speeds one pass already destroys the SiC encapsulation, while for scanning speeds as high as 100 mm/s three passes are required to laser through the silicon layer.

SEM pictures of polished cross sections of trenches lasered with different laser parameters are displayed in Figure 5.6. Laser trenches in a) and b) were lasered to the SiC encapsulation with only little residual silicon in a) and a lot of re-solidified silicon in b). In c) the laser destroyed the SiC encapsulation and lasered into the graphite substrate, while in d) the trench does not reach the intermediate layer.

The parameters of the waterjet guided laser could be well adapted to the layer thickness to form uniform trenches, nevertheless a subsequent etching steps seems to be necessary and will be discussed later.

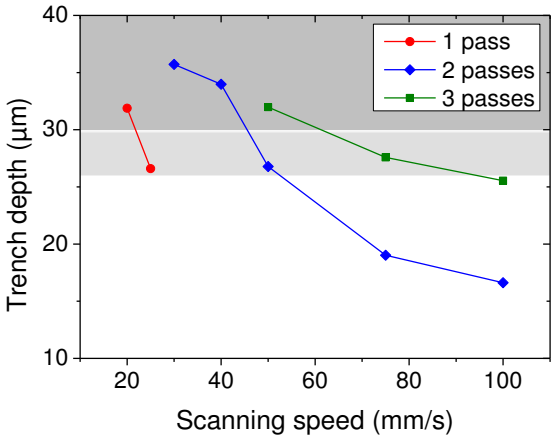

Figure 5.5: Trench depth in dependence on scanning speed for one, two and three passes of the laser. For parameters in the light grey area the SiC layer got damaged and lasered through with parameters in the dark grey area.

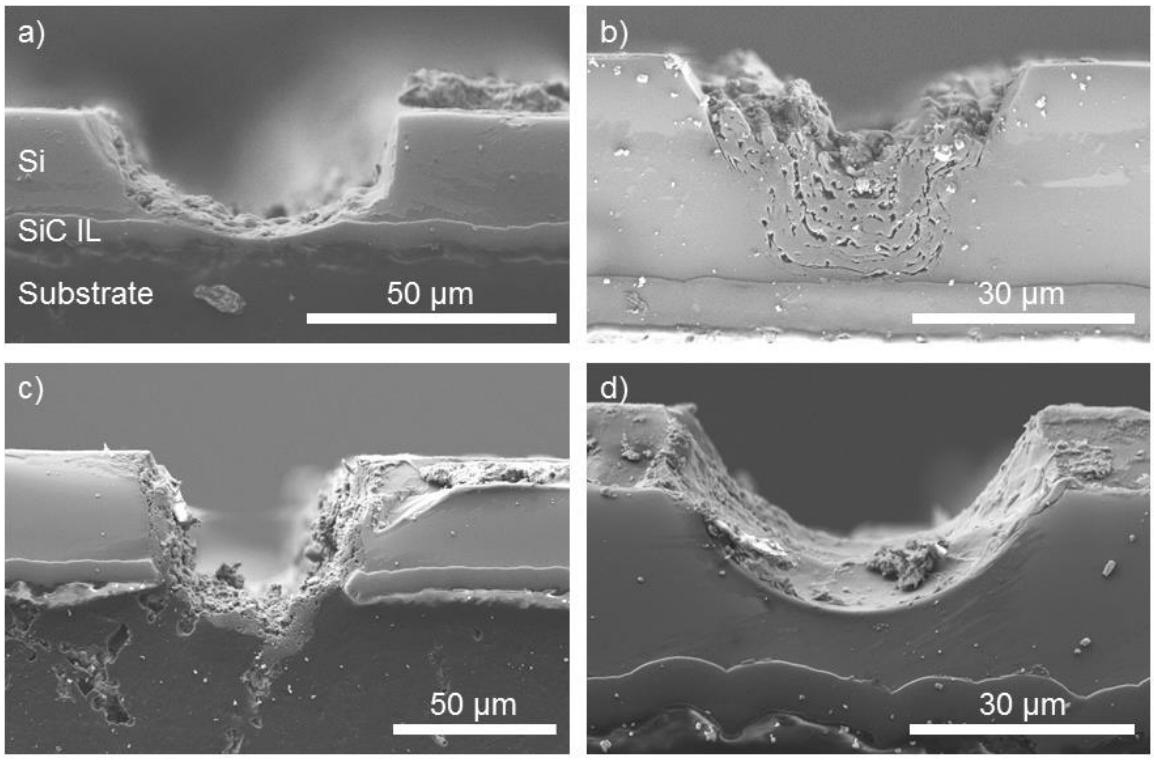

Figure 5.6: SEM pictures of polished cross sections of trenches formed by waterjet guided laser with different laser parameters. While in a) and b) it was lasered to the SiC intermediate layer, in c) the encapsulation was destroyed an in d) the trench is too shallow.

Dry Laser

Two iterations of laser parameter optimization were done for the dry laser. The spot of the used laser system has a diameter of approximately 20 µm. To ensure even trenches, a small pulse spacing was chosen and was varied between 1 and 4 µm in the first experiment. One, two and three passes were used to laser a trench at maximum power of 7.3 W. In the second iteration a laser power of 3.6 W was used and lines were lasered with pulse spacing from 1 to 6 µm and 1 to 6 passes. Trenches lasered with a laser power of 7.3 W and pulse spacing of 1 and 2 µm went through the SiC layer into the graphite as e.g. in Figure 5.7 a). Comparing Figure 5.6 and Figure 5.7 it can be seen that trenches lasered with the waterjet guided laser are wider than the ones lasered with the dry laser. The narrower trenches allow for a smaller gap between the cell strips in the interconnection which increases the active module area fraction, see section 3.3.

The parameters can be adjusted well to the thickness of the silicon layer, as can be seen in Figure 5.7. Unfortunately the SiC layer could not function as barrier layer for the laser and inhomogeneities in layer thickness make a subsequent etching step necessary.

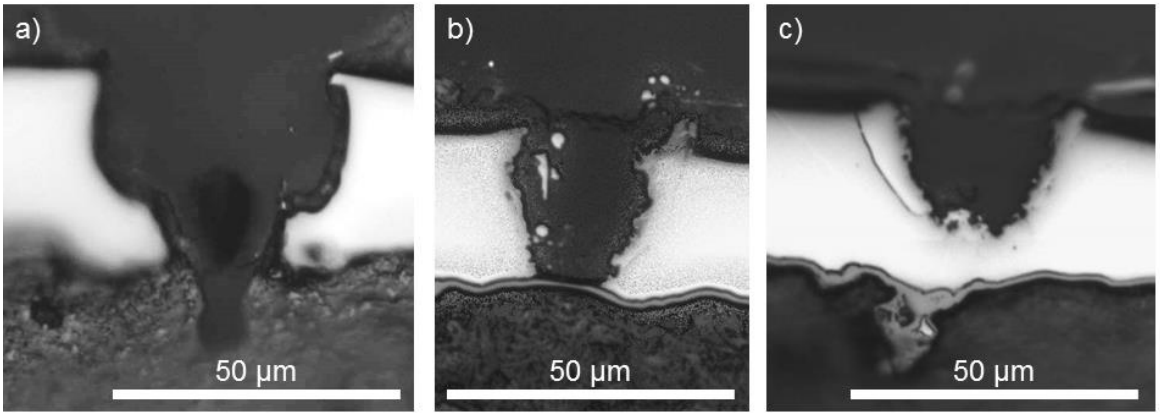

Figure 5.7: Microscopy pictures of cross sections of lasered trenches. The white layer is the silicon, the smooth grey layer beneath the SiC encapsulation and below the graphite substrate can be seen. In a) the laser destroyed the SiC layer and lasered into the substrate, in b) the silicon layer was lasered to the SiC layer and in c) the silicon was not completely ablated.

Subsequent etch step

With the generic thickness variations of the epitaxially grown silicon, the trench depth has to be adapted to the minimum layer thickness and the areas with a thicker silicon layer have to be etched after lasering using the SiC encapsulation as etch stop.

In Figure 5.8 microscopy images of cross sections of identical laser trenches before and after a subsequent etch can be seen. As subsequent etch a 3 min KOH etch (23 % aqueous KOH, 80 °C) in a), a 5 min plasma etch (CCP with SF_6, see 5.2.1) in b) and a plasma texturing process, see chapter 4, in c) were used. All three are feasible as a subsequent etch. Considering the differing etch rates of various crystal orientations in KOH and the single-sided etching of plasma etching processes, a plasma etching process would be preferably used as a subsequent etch. A combination of subsequent etch and plasma texturing process in one etch step is also possible and can simplify the processing sequence.

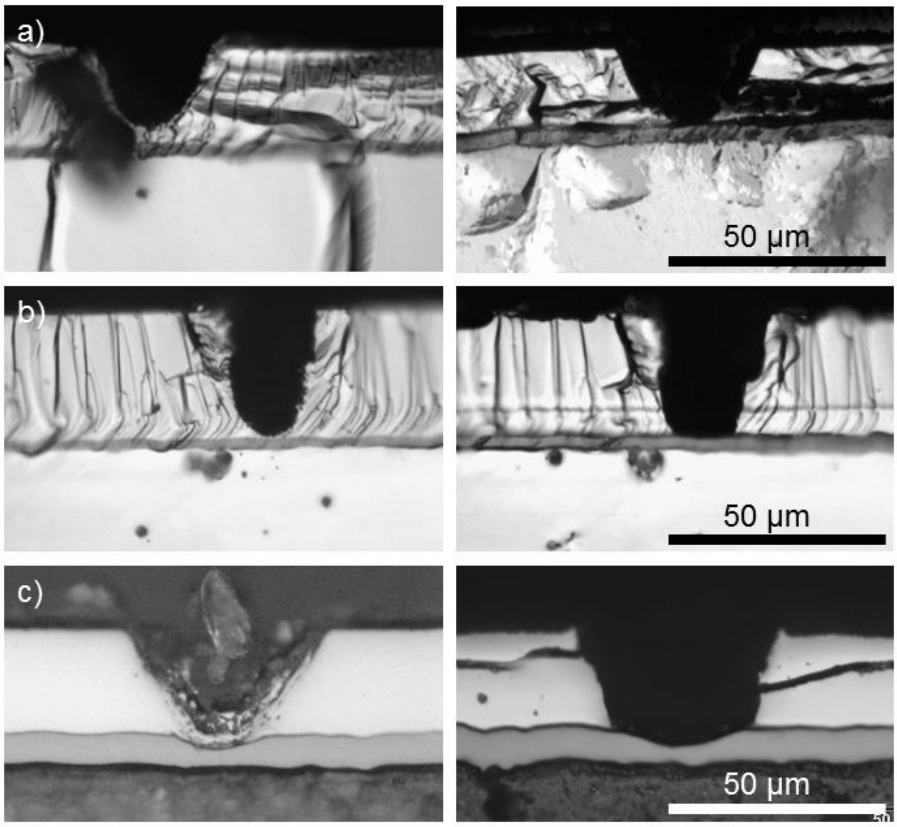

Figure 5.8: Microscopy pictures of cross sections of lasered trenches before (left) and after different subsequent etches (right). In a) a KOH etch, in b) a plasma etch and in c) a plasma texturing process was used.

5.1.3 Summary – separation of cell strips

The laboratory realization with photolithographic structuring of the silicon oxide masking layer and subsequent KOH etch to form the trenches worked well for the processed cells but is not industrially feasible. For both lasering methods the parameters could be adapted to the required trench depth. After investigation of laser processes and possible subsequent etching processes, the most promising process was found to include a subsequent plasma etch. Using a plasma texturing process as subsequent etch reduces the number of processing steps and is therefore considered the best alternative.

5.2 Emitter structuring

In order to contact the base of the cell in a single side contacted cell concept such as the iSiMo concept, the emitter needs to be structured in order to access the base. In the case of the iSiMo modules the base is contacted next to the trench that separates the cell strips, as shown in Figure 3.1. Other cell concepts

such as interdigitated back contact (IBC) cells or emitter wrap through (EWT) cells also have structured emitters and industrial application processes developed for these cell concepts can be used, e.g. [53]. A structured emitter can be obtained either by silicon structuring of a wafer with emitter or by selective emitter formation, e.g. by emitter diffusion with a structured diffusion barrier. Silicon oxide is frequently used as an emitter diffusion barrier but also other diffusion barriers that can, for example, be applied by ink jet are found in literature [54]. In this thesis, only the case of structuring an emitter after diffusion will be discussed. The emitter structuring process used for the fabrication of mini modules in this thesis consisted of application and photolithographic structuring of a resist, subsequent plasma etching of the emitter and stripping of the resist. The evaluation and development of the plasma etching process is described in the next section.

5.2.1 Plasma etching for emitter structuring

For the plasma etching step in the process of emitter structuring the same tools were used as for plasma texturing (see section 4.3). The results presented here were achieved with the SI 600, where an already established process was used. Later the silicon etching process was also transferred to the Plasmalab System 133, with similar results.

80 sccm SF_6 was used as an etching gas in CCP configuration with a power of 300 W and an electrode height of 90 mm at a process pressure of 20 Pa. The plate cooling was set to -15 °C to prevent the resist from overheating and polymerizing. The processing time was 2.5 min, because longer processes also lead to polymerization. For longer etching times a break of 10 min was introduced after every 2.5 min to allow the samples to cool down again.

To characterize the emitter structuring process, a layout of 9 cells with an area of 1 cm² on a 5 x 5 cm² wafer was chosen, which is frequently used at ISE to process front side contacted c-Si thin film solar cells (e.g. plasma textured cells in section 4.5.5). In that case the emitter also has to be structured in order to contact the base on the front side. A thickness map of a processed wafer can be seen in Figure 5.9. The green lower area is the area where 5-6 µm silicon was etched. The nine 1 x 1 cm² areas that were masked by photoresist are clearly visible.

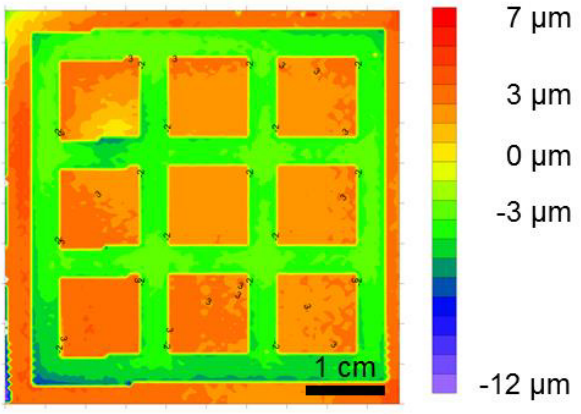

Figure 5.9: Thickness measurement map of a sample etched in the mesa etch process for 5 min with 4 samples on the plate. The etching process removed 5-6 µm very homogeneously.

As most plasma etching processes are dependent on the Si area that is available for etching, experiments were done with different number of samples on the plate. The resulting etch depths and rates for different processing times depending on the number of samples can be seen in Figure 5.10. While there is a wide spreading of measured etch rates for processes with one sample a trend of a decrease in etch rate with increasing silicon area can be observed. For the purpose of emitter structuring the definitive etch rate is secondary as the emitter just needs to be removed. With an etch rate around 1.5 µm/min a process of 2.5 min is sufficient for standard diffused emitters of less than 1 µm thickness. More important is the homogeneity across the processed samples. The sample in Figure 5.9 was etched for 5 min with four samples on the plate and, as can be seen, silicon was homogeneously etched over the whole wafer.

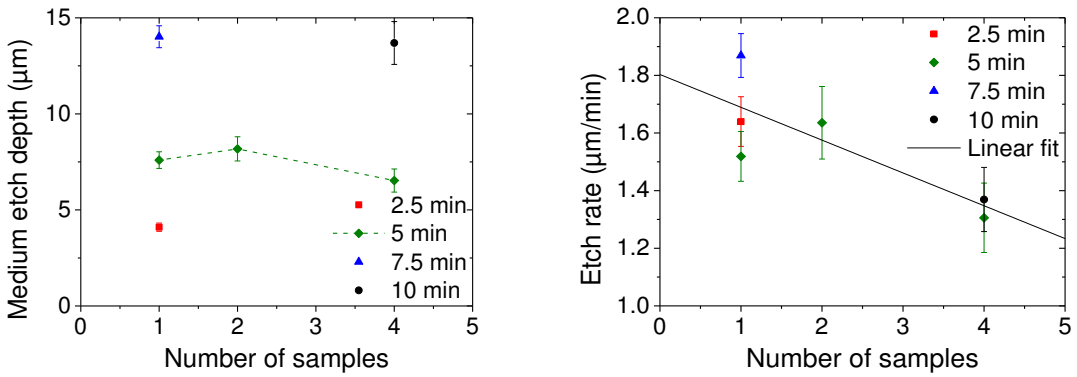

Figure 5.10: Average etch depth (left) and etch rate (right) for processes with differing etching times and number of samples. Error bars indicate the standard deviation. Left: The dashed line is a guide to the eye. Right: The linear fit is a fit of all displayed measurements indicating the decreasing etch rate with increasing silicon area.

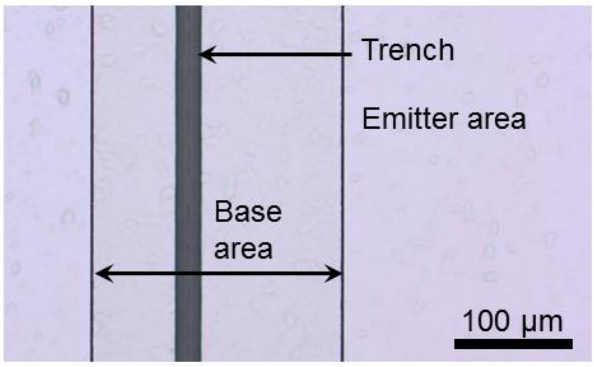

Figure 5.11: Microscopy picture of FZ wafer that was structured as the SOI wafers for mini-module fabrication. The structuring of the emitter can clearly be seen.

In the laboratory process for the integrated interconnected mini-modules the emitter was also structured by the plasma etching process described above. A microscopy picture of an FZ wafer that was processed in parallel to the SOI wafers is displayed in Figure 5.11.

5.2.2 Summary – Emitter structuring

Emitter structuring using photolithographically structured resist and plasma etching is a reliable and stable process on a laboratory scale. For industrial realization photolithography is not feasible, but could possibly be replaced by printing an etching barrier. For the industrialization of plasma etching, inline tools are already available.

6 INTERCONNECTION

The actual interconnection of the cell strips is the topic of this chapter. Two approaches are discussed: The first approach uses evaporated contacts in a photolithographic process, whose optimization is illustrated here. The second approach is realized by screen-printed contacts, which would be industrially feasible. Different isolating screen-printing pastes are also evaluated for this approach.

After separation of the cell stripes and emitter structuring the cells need to be interconnected. The open pn-junction at the trench edge is the most critical issue in the interconnection, as the metallization must cross it as well as the trench to the next cell strip. To prevent shunts at the open pn-junction, an isolation layer has to be applied beneath the metallization. As different metallization techniques are possible, the isolating layer needs to be adapted to the used metallization. A SiN_x layer can isolate an evaporated metallization but will not prevent shunting if standard screen-printing pastes are used. Additionally, the metallization must be chosen in respect to the doping of the silicon it should contact. A process on a laboratory scale has been developed in this thesis and will be presented in the next section, for industrial realization experiments on isolating screen-printing pastes have been conducted and will also be discussed in this chapter.

6.1 Laboratory realization

For the laboratory process evaporated metal contacts and a PECVD deposited SiN_x isolating layer were chosen, with structuring steps done by photolithography. The processing steps are shown in Figure 6.1. After application and structuring of the SiN_x layer the Al/Ti/Pd/Ag metallization is evaporated using structured photoresist as mask. Depending on the thickness of the evaporated metallization an electro plating step is necessary. SiN_x layers from different PECVD tools were evaluated as well as different photoresists for both photolithography processes. Thick- and thin-film photoresists were used as well as positive photoresists where the exposed areas are removed during development and negative photoresists

where the exposed areas remain after development. Depending on the photoresist a thick or thin metallization was evaporated.

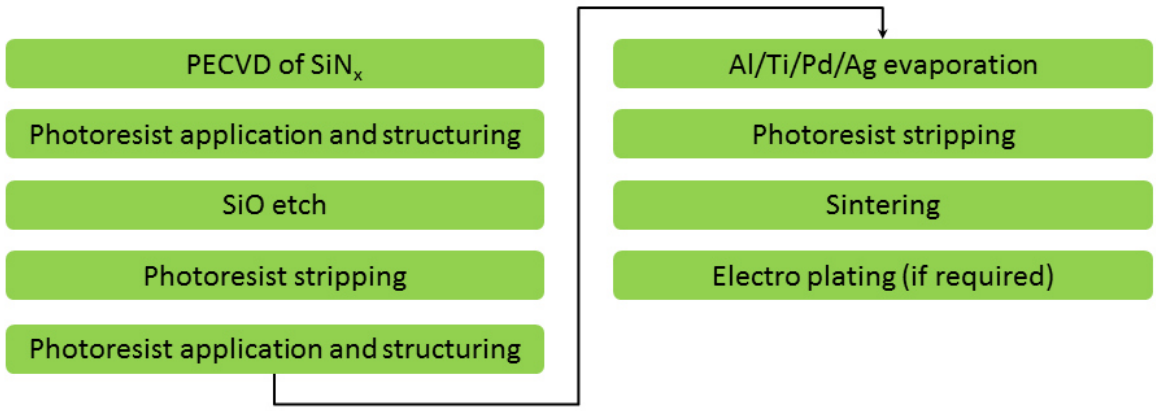

Figure 6.1: Processing steps of interconnection in the laboratory process.

6.1.1 Properties of SiN_x layer

The silicon nitride layer can not only act as passivation and anti-reflective layer but also provide the necessary isolation of the pn-junction. An additional requirement for this application is the easy structurability. Different silicon nitride layers from two deposition tools were tested and two of these layers were applied to the fabrication of iSiMo mini-modules. Properties of the used layers (SiN_x A, SiN_x B, SiN_x C) are presented in this section. SiN_x A and B are from the same laboratory scale tool, SiN_x A was developed as anti-reflection layer while SiN_x B was designed as passivating layer. SiN_x C was deposited in an industrial type tool and is a firing stable anti-reflective layer that also passivates. It is used as front surface silicon nitride in standard screen-printed cells.

Passivation properties

To determine the passivation quality of the silicon nitride layers from the laboratory scale tool (SiN_x A and SiN_x B) lifetime samples were fabricated with 1 Ωcm FZ material coated with SiN_x on both sides. The results are summarized in Table 6.1. It was confirmed, that SiN_x B has good passivating properties in contrast to SiN_x A.

Table 6.1: Effective lifetime of FZ samples with different SiN_x layer. Measurements performed with QSSPC.

SiN_x layer	Effective lifetime (µs)	Standard deviation
SiN_x A	0.79	0.01
SiN_x B	464.5	116.1

Optical properties

The reflection of the lifetime samples with SiN_x A and SiN_x B was measured to determine the quality of the layer as anti-reflective coating. As expected, SiN_x A, which was developed as ARC, showed very low reflection at 600 nm and the typical curve progression for silicon nitride on a planar silicon surface, see Figure 6.2. SiN_x B shows a much higher reflectance and could not be used as ARC. SiN_x B was developed as passivating layer and has a higher Si content than SiN_x A, which leads to increased light absorption in the layer compared to ARC SiN_x layers. SiN_x B is therefore unsuitable for the application on the front surface of solar cells.

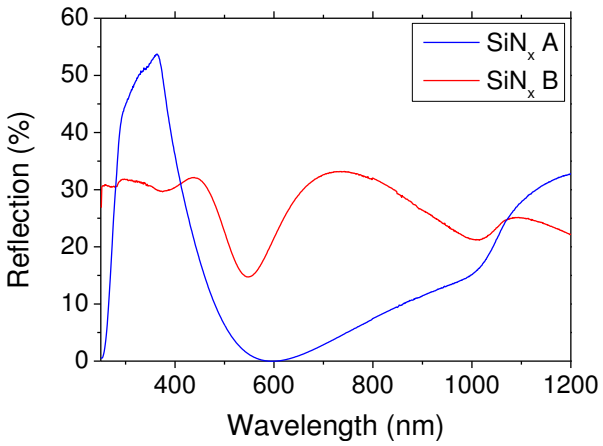

Figure 6.2: Measured reflection of FZ silicon with SiN_x layer comparing SiN_x A and B.

SiN_x structuring

The structuring of the silicon nitride layer was done in SiO etch with a structured photoresist as mask. Depending on the composition, different SiN_x layers exhibit different etch rates and are sometimes hard to etch. In the first experiments SiN_x A was used in combination with Microposit S1828 G2 photoresist, which has a thickness of approximately 2.8 µm.

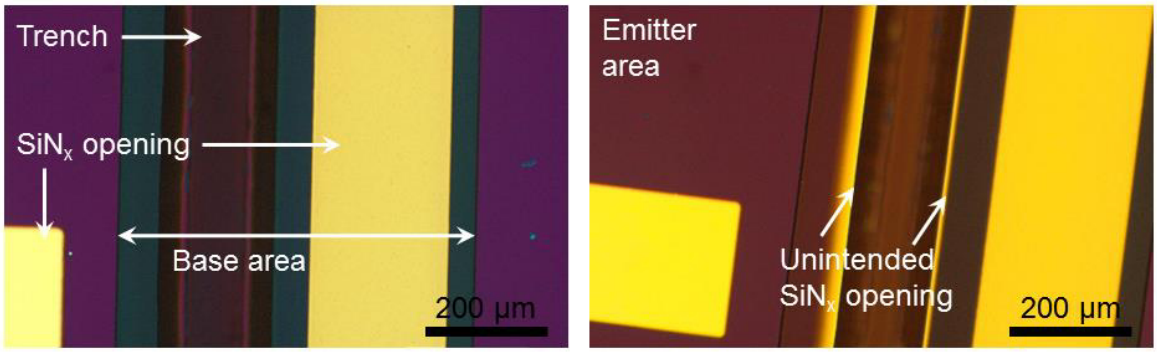

Figure 6.3: Microscopy images of the structure after silicon nitride structuring without defects (left) and with unintended SiN_x opening at the trench edges (right).

The resulting structure after approximately 3 min of etching and subsequent resist stripping is displayed on the left of Figure 6.3 and shows clear openings of the SiN_x layer. Using SiN_x C the etching time had to be extended to up to 25 min. The otherwise same process lead to additional silicon nitride openings at the trench edge. Especially at the left side of the trench in Figure 6.3 (right) it is crucial that the layer isolates. It was found that the photoresist is thinner at the trench edges than on the flat surface and the SiN_x etching at the trench edge was considered to be caused thereby. To solve the problem a thicker photoresist, ma-P 1275 was used and lead to results as before, even with extended etching times. Nevertheless, with respect to structurability, SiN_x A is preferable as isolating layer as it exhibits a shorter etching time than SiN_x C.

Isolation

The successful isolation can be seen in the mini-module results, as shunts affect the parallel resistance, which can then lead to a reduced fill factor and V_{OC}. As the cells are connected serially the V_{OC} of individual cells adds up to the V_{OC} of the module. In Table 6.2 the V_{OC} of single cells in a four cell module fabricated with SiN_x A is compared to the total V_{OC} of the module. With an error of ± 1 % the added up V_{OC} fits well to the direct V_{OC} measurement of the module. Achieving an open circuit voltage of above 600 mV is only possible with an intact isolation layer to prevent shunting. SiN_x B and SiN_x C were not used in iSiMo modules. Therefore no statement can be made on these silicon nitride layers.

Table 6.2: V_{OC} measurement of single cells and the sum of a mini-module consisting of four cells in comparison with the measured module V_{OC}.

Cell number / module	**V_{OC} (mV)**
1	619 ± 6
2	624 ± 6
3	624 ± 6
4	623 ± 6
Sum of single cells	2491 ± 25
Module measurement	2495 ± 25

Summary – Properties of different SiN_x layers

The silicon nitride layer SiN_x A was characterized concerning isolating, reflection and passivation properties as well as structurability and compared to SiN_x B and SiN_x C. SiN_x A had a high etch rate compared to SiN_x C and could be structured well. As SiN_x A was designed as an ARC, it reduces reflection but does not passivate a silicon surface. Besides isolation, the structurability of the silicon nitride layer is crucial for the laboratory scale iSiMo process. SiN_x A is therefore a good choice for fabrication of the mini-modules, but an improved SiN_x that also passivates could enhance their performance.

6.1.2 Metallization

The metallization is applied in a photolithographic lift-off process. To simplify the process the same metal is used for both polarities of the solar cell. This section illustrates the challenges of and improvements done in the metallization process. It is also discussed why Al/Ti/Pd/Ag metallization was chosen.

Microposit S1828 G2 photoresist was used in first experiments and resulted in incomplete interconnection between the cells. As can be seen in Figure 6.4 a, the interconnection in the trench was missing. As a makeshift solution, conductive silver was applied to be able to thicken contacts by electroplating and characterize the fabricated modules (Figure 6.4 b).

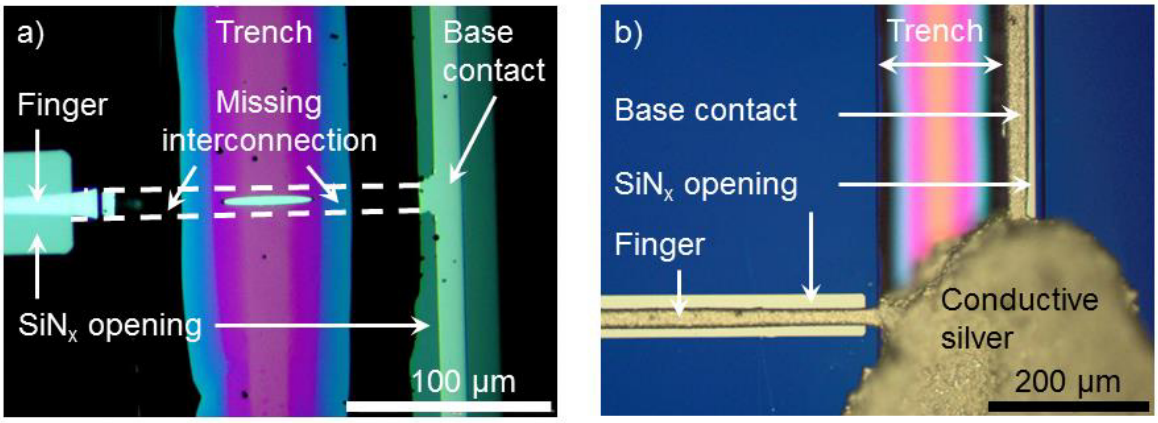

Figure 6.4: Microscopy pictures of the interconnection between two cell strips. The emitter contact is running from the left over the trench to connect the base contact of the next cell on the right. a) Interconnection in the trench is missing. b) Interconnection established by conductive silver, afterwards electro-plating is possible.

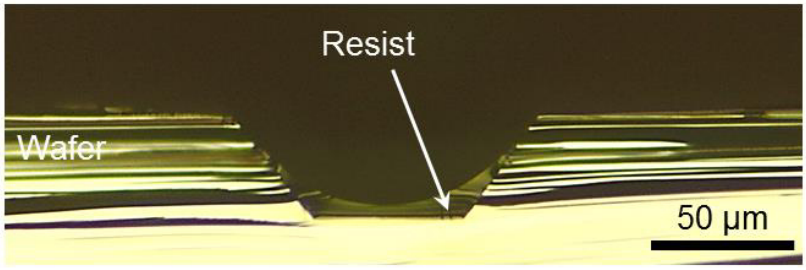

Figure 6.5: Microscopy image of a cross section of a wafer with trench after photoresist spin-coating.

The origin of the interrupted metallization could be found when taking a closer look at the photoresist after the spin-on process. Figure 6.5 shows a microscopy image of a cross section of a sample with photoresist in the trench. The thickness of the resist in the trench, especially in the corners, far exceeds the thickness of the resist on the flat surface. Positive photoresists, such as the one used, must be fully exposed in order to be removed during development. The much thicker resist in the trench corners was not fully exposed during the standard exposure time and therefore not removed during development. After evaporation and lift-off, the metal was also lifted in the trenches, causing interruptions in the interconnection. Two approaches were followed to improve the metallization process: A second exposure step for areas where the resist is thicker to ensure full exposure of the resist in the trench and the use of a negative resist.

Double exposure

As solely extending the exposure time would cause defects in the resist and lead to a broadening of opened lines, a second exposure step was applied to a positive resist only at the trenches, where the resist is thicker. The broadening of the resist opening due to double exposure can be seen in Figure 6.6 on the left. The resist is fully removed even in the trench and the metal interconnection does not show interruption. The 2.8 µm thick Microposit S1828 G2 was used for this process, which showed thinning at the edge of the trench that in turn caused parasitic metal evaporation on the trench edge (Figure 6.6). As the trench edge was isolated, the parasitic metal only shadows the underlying cell but does not otherwise harm the performance of the module. The interconnection through the trench is complete although it cannot clearly be seen in the microscope pictures in Figure 6.6.

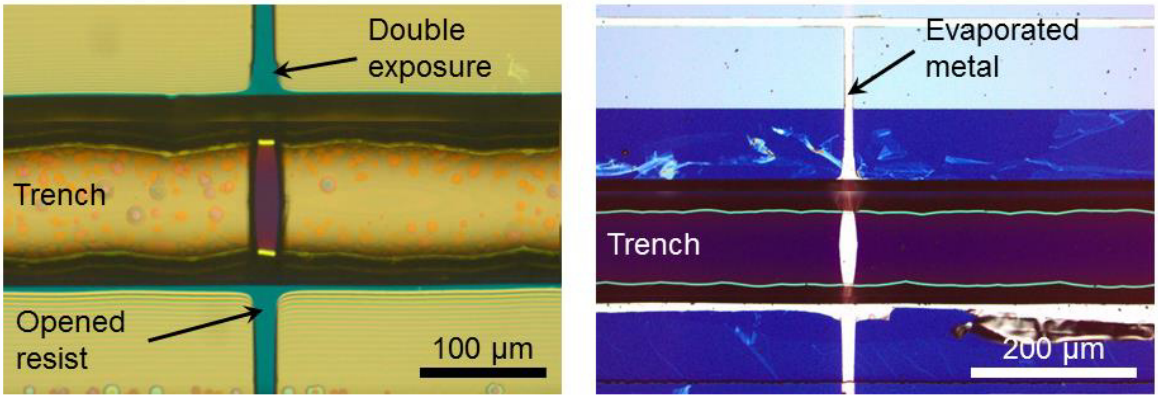

Figure 6.6: Microscopy images of sample with trench after after development of the resist with double exposure of resist in the trench (left) and after subsequent metal evaporation and lift-off (right)

Negative resist

As with the negative resist the unexposed part is removed during development, the thicker resist can be removed by extending the developing time. The 7 µm thick AZ nLoF 2070 resist was used, where only the first couple of micrometers are exposed during exposure. While the resist is developed, the unexposed resist under the exposed part is also removed causing an undercut, as illustrated in Figure 6.7. As the subsequent step is metal evaporation, the undercut does not pose an issue, the metal contact is merely widened scarcely.

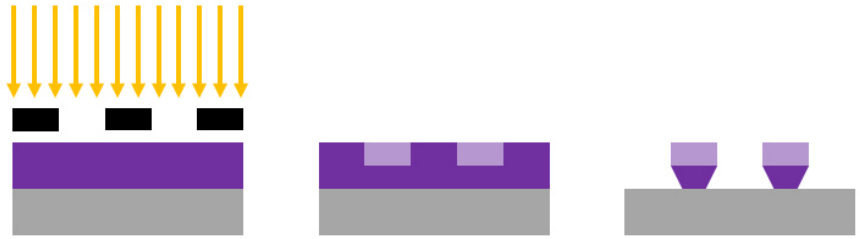

Figure 6.7: Schematical illustration of the process of a thick negative photoresist with the resulting undercut after development.

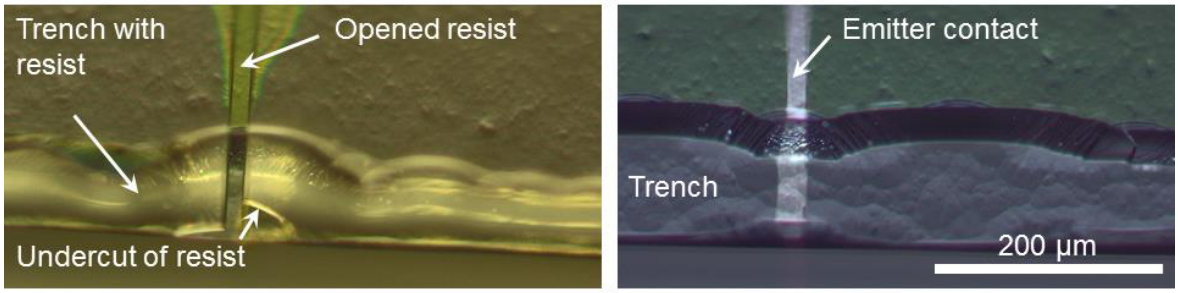

Figure 6.8: Microscopy pictures of sample with trench after development of the negative resist (left) and subsequent metal evaporation and lift-off (right). The samples were tilted in order to be able to see the trench edge.

In Figure 6.8 samples with trench are displayed after development of the resist and after metal evaporation and resist lift-off. The undercut of the thick resist in the trench can clearly be seen, as well as the slight broadening of evaporated metal after the lift-off.

Metal evaporation and lift-off

Metal was evaporated on the structured photoresist, which was subsequently lifted. A stack of 100 nm aluminum, 50 nm titanium, 50 nm palladium and 100 nm silver in combination with the Microposit S1828 G2 was deposited or, when using the AZ nLoF 2070, the thickness of the silver layer was increased to 5000 nm. The thin evaporated contacts were thickened to 5 to 10 µm thickness by silver electro-plating to increase the conductivity, which was not necessary for the thick contacts. Light-induced plating [28] was not used, as it is very difficult to regulate with the electrical potential difference due to the serial interconnection. The light intensity would have to be adjusted in combination with the electrical potential to get a homogeneous deposition rate over the whole module.

With defective structuring of the photoresist, as explained above, an intact interconnection is impossible. In most cases metal evaporation and lift-off lead to intact interconnection when the photolithographic structuring of the resist was

successful, see Figure 6.8 and Figure 6.6. Nevertheless, disruptions could often be observed, as shown in Figure 6.9. The interconnection through the trench is intact, but at the trench edge the finger seems to be ripped off which most likely occurred during lift-off. Another issue that can occur is an incomplete lift-off (Figure 6.9). In contrast to ripped-off contacts, incomplete lift-off hardly affects the performance of the mini-modules at this stage. It increases shadowing which of course decreases the J_{SC} of the module.

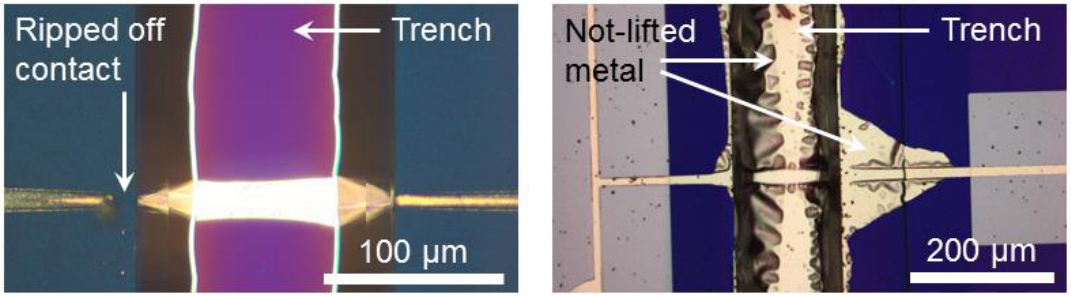

Figure 6.9: Microscopy pictures of integrated interconnected mini-modules after metal evaporation and lift-off. Left: Thick evaporated metal was ripped off, possibly during lift-off. Right: Incomplete lift-off after thin metal evaporation.

6.1.3 Intermediate oxide layer

All the structuring steps also affect the intermediate layer between the thin crystalline silicon layer and the substrate. It is vital that the intermediate layer remains intact if a conductive substrate is used. Otherwise, the cells would be short-circuited through the substrate. In the case of the SOI wafers the IL consists of a 1 µm thick SiO_2 layer. The SiO_2 layer is etched by the KOH etch of the silicon structuring step as well as in the plasma etching process for emitter structuring and by all HF containing wet chemical etches and cleaning steps. In Figure 6.10 a SEM picture shows the bottom of the trench at the edge, after silicon nitride structuring was done. The SiO_2 IL between silicon substrate and silicon thin-film shows an undercut created by the etching steps. The SiN_x layer can also be seen on the slope of the trench as well as on the bottom. The remaining layer thickness of the SiO_2 in the middle of the trench is approx. 170 nm. While this is sufficient as isolation, there is a step of about 800 nm in the trench corners which the metallization needs to bridge. It could be observed that the state of the intermediate layer can vary in a module batch. A sample of the same batch was also investigated in the SEM and no undercut was visible which is attributed to a locally fluctuating concentration of etching species.

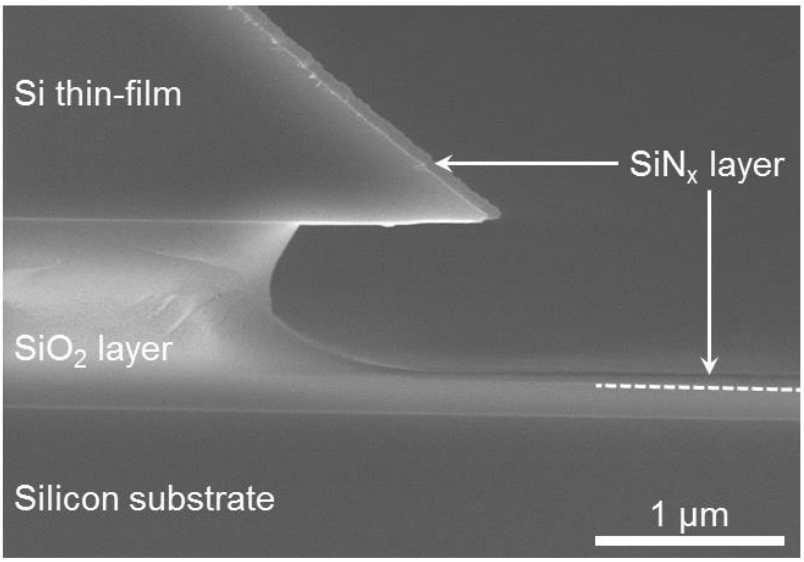

Figure 6.10: SEM picture of the bottom of the trench at the edge.

6.1.4 Contacting metal

The contacting material of a solar cell depends on the contacting area as well as the doping of the silicon. This material has to provide a good adhesion and low contact resistance. This section refers to evaporated contacting fingers, as these are used in the laboratory scale interconnection concept.

Using evaporated contacts, p-type silicon is usually contacted by aluminum and n-type by titanium. To enable thickening by silver electro-plating a stack of Al/Ti/Pd/Ag or Ti/Pd/Ag is applied. As the use of two different materials for emitter and base contact complicates the processing and alignment, both were contacted by the same metal.

When metal is brought in contact with a semiconductor a so called Schottky contact with Schottky barrier is formed. The barrier height Φ_B is dependent on the metal work function Φ_M and the semiconductor electron affinity X [55].

$$\Phi_B = \Phi_M - \mathrm{X} \tag{6.1}$$

The contact resistivity between metal and semiconductor is not only dependent on the barrier height but also on the doping concentration, as that determines the dominating conduction mechanism. Thermionic emission dominates on lowly doped material of $N_D < 10^{17}$ cm^{-3}, while for highly doped material with $N_D > 10^{19}$ cm^{-3} field emission is the dominating conduction mechanism and on moderately doped material with doping concentrations of 10^{17} cm^{-3} < N_D < 10^{19} cm^{-3} thermionic field emission dominates. A review on semiconductor metal contacts

and contact resistance can be found in [28, 55]. Figure 6.11 shows the relation between doping concentration N_D and contact resistivity ρ_c for different Schottky barrier heights Φ_B.

For aluminum and titanium on p- and n-type silicon typical contact resistivities are shown in Figure 6.12. Highly doped silicon (10^{19} cm^{-3} – 10^{20} cm^{-3}) of both polarities can be contacted with aluminum and titanium. Moderately to lowly doped p-type silicon (10^{14} cm^{-3} – 10^{17} cm^{-3}) can better be contacted with aluminum, while moderately doped (< 10^{19} cm^{-3}) n-type silicon shows increased contact resistivity in combination with aluminum. Regarding the interconnection concept where a p-type base and n-type emitter need to be contacted, aluminum was considered the best choice as contacting material. That choice poses some demands for the emitter: High surface doping concentration (10^{19} cm^{-3} – 10^{20} cm^{-3}) to ensure low contact resistivity and a deep pn-junction (approx. 0.5 µm). The deep pn-junction is necessary to prevent shunting. Aluminum tends to spike into silicon, especially if it is sintered, and spiking through the emitter would cause shorting of the cell. The chosen emitter that meets these requirements has a sheet resistance of 40 Ω/□.

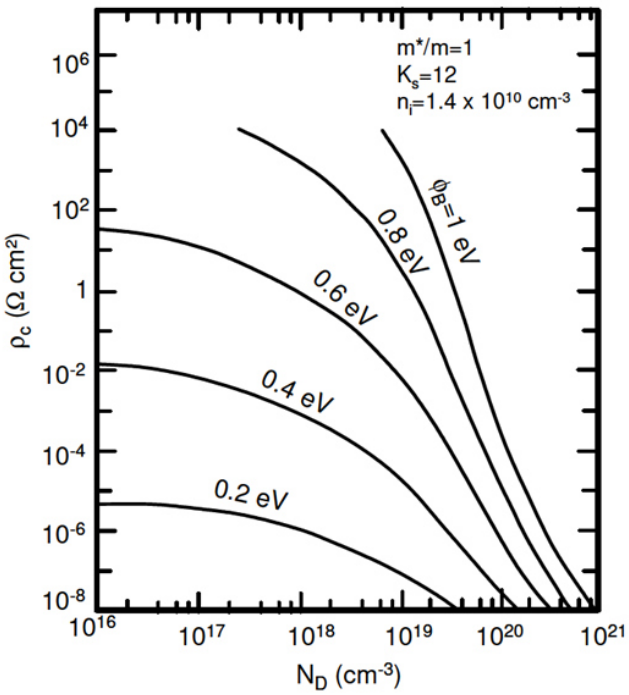

Figure 6.11: Contact resistivity depending on doping concentration for different barrier heights, [28] (redrawn from [55]).

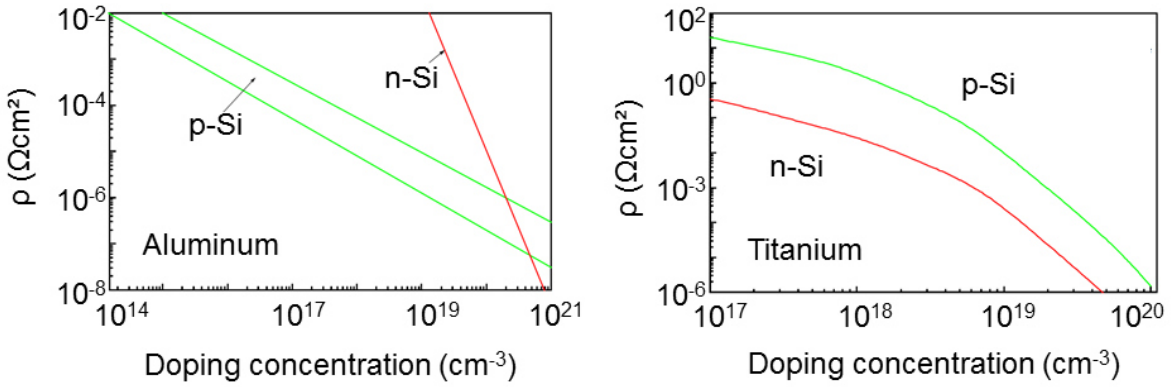

Figure 6.12: Contact resistivity of aluminum-silicon contact (left) and titanium-silicon contact (right) on n- and p-type silicon dependent on doping concentration, from [56].

Measurements of the contact resistance of the Al/Ti/Pd/Ag fingers on the 40 Ω/□ emitter were conducted using the transmission line modelling method (TLM) described in [57]. Values between 1.0 mΩcm² and 7.5 mΩcm² were measured, which lies in the expected range.

6.1.5 Summary – Laboratory realization

An interconnection process was developed using photolithography for the structuring steps. Different silicon nitride layers were tested as isolating layers with regard to structurability, optical and passivating properties. SiN_x A (optimized as ARC) is an appropriate choice for fabrication of the mini-modules, but an improved SiN_x, which also passivates, could enhance their performance. Different photoresists were used to ensure accurate structuring of the SiN_x layer, but a thick-film resist is recommended. For the metallization the resist accumulated in the trench which complicated the structuring. Two solutions were presented: Using a negative resist combined with longer development of the resist and, even more successful, a double exposure of the positive resist in the trenches.

Microscopy pictures showed the interconnection through the trench.

6.2 Screen-printed interconnection

In the fabrication of solar cells, screen-printing is most commonly used for metallization [58]. Consequently, research was done on screen-printing as metallization and interconnection technique for this module concept. As SiN_x layers are no sufficient isolation against standard screen-printing pastes, isolating pastes were evaluated in test structures.

Three different isolating screen-printing pastes were tested in combination with three silver metallization pastes with different glass frit content. In the first experiment, test structures were fabricated to determine the isolating properties of the pastes. Attempts were made to improve adhesion in a second iteration by using different firing profiles with the most promising pastes.

Detailed information about the firing profiles or used pastes cannot be provided. The composition of the pastes was not disclosed by the manufacturers and can therefore also not be discussed.

6.2.1 Preparation of samples

125 x 125 mm² pseudosquare Cz wafers were used for the test structures and processed in the sequence displayed in Figure 6.13. A 75 Ω/□ phosphorous emitter was formed by $POCl_3$ diffusion and a SiN_x layer deposited by PECVD. Four 5 x 5 cm² areas per wafer were defined and the isolation paste applied. Two of the areas were fully covered with isolation paste, one was partly covered and one left uncovered as reference area. In the first experiment the isolation pastes were all fired according to manufacturer's data in a single wafer firing furnace; firing approximately 30 min with peak temperatures of 580 to 850 °C, depending on the paste. A metallization grid was applied in all four areas and fired. A silver metallization paste was used: one for standard solar cells and two pastes for metallization wrap through (MWT) solar cells with reduced glass frit content.

In the second iteration of the experiment different firing profiles for the isolating pastes were used, to improve the adhesion and shorten the relatively long firing times. These profiles included not only different peak temperatures but also co-firing with the metallization and short firing profiles, similar to metallization firing profiles.

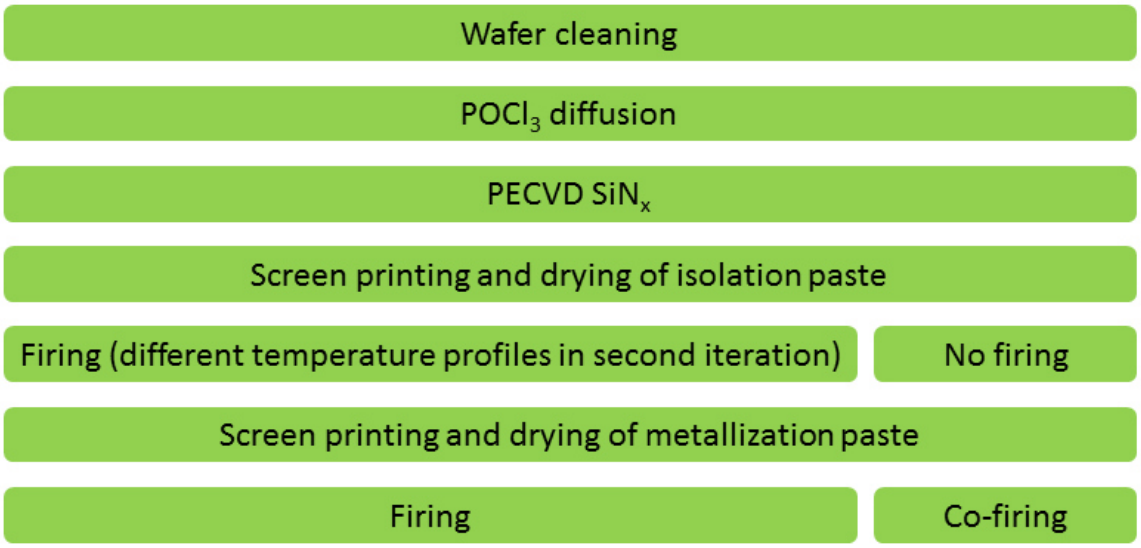

Figure 6.13: Processing sequence of test samples to determine the isolation properties of isolating screen-printing pastes and optimize their firing parameters.

The samples were characterized by TLM measurements [57] to check if the metallization could establish a contact through the isolating layer and, in the reference areas without isolation, through the SiN_x layer.

6.2.2 Adhesion and isolating properties

Two of the three investigated isolation pastes from the first experiment isolated against all three silver metallization pastes. Paste 1 partly peeled off the wafer, as shown in Figure 6.14. The adhesion of the silver paste on paste 2 was insufficient, which was caused by bubble formation in the isolating layer underneath the contact fingers, as can be seen in Figure 6.15. The formation of bubbles in the isolating paste suggests that the adhesion problems might be solved by optimization of the firing parameters. The third paste, fired at the lowest temperature, did not form a reliable isolation layer against two of the silver pastes. The TLM measurements showed that a contact could in some cases be established in spite of the isolating layer. The paste appeared to soften during metallization causing the metallization fingers to meander on the paste and partly subside into it (Figure 6.16), which might be the cause for the unreliable isolation of this paste. The third paste was therefore not further analyzed. In areas without isolation the silver paste with the highest glass frit content formed the best contact and was used in further experiments.

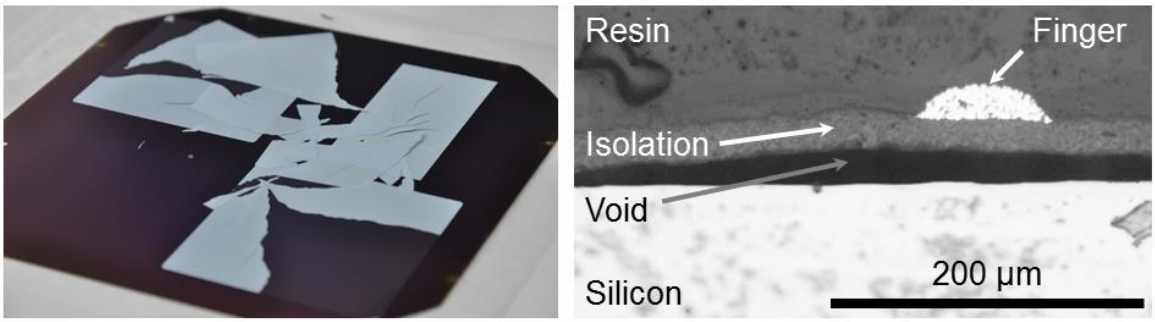

Figure 6.14: Flaking of paste 1. Picture of severe flaking of paste on wafer (left). Microscopy image of cross section polishing of wafer with isolation paste and metallization, where void between isolation layer and wafer is clearly visible (right).

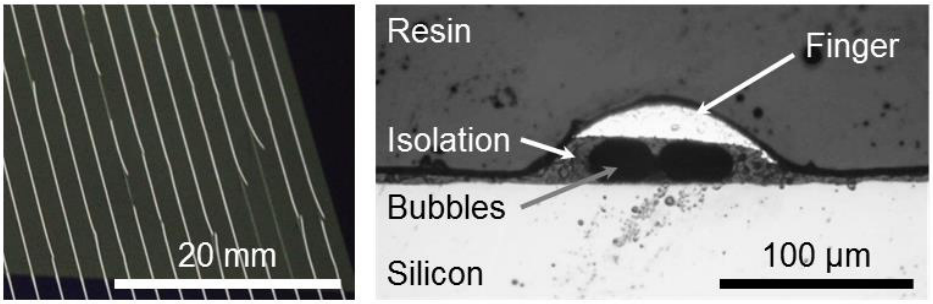

Figure 6.15: Picture of metallization fingers peeling off paste 2 (left), microscopy image of cross section polishing of wafer with isolation and metallization with bubbles forming underneath the finger causing the finger detachment.

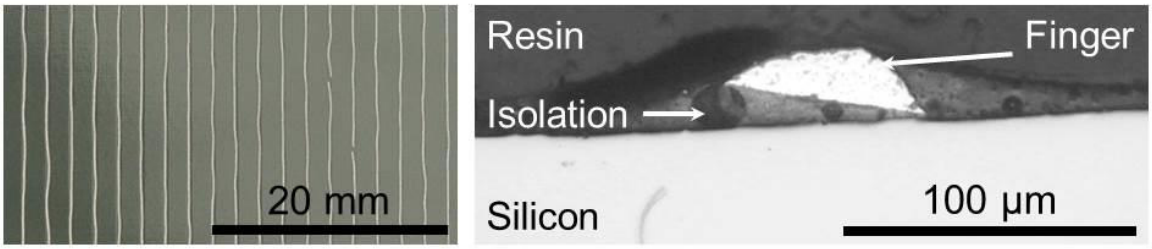

Figure 6.16: Picture of meandering metallization fingers on isolating paste 3 (left). Microcopy image of cross section polishing of wafer with isolating layer and finger with the finger sunk into the paste (right).

6.2.3 Firing parameter optimization

The samples for firing profile optimization were processed as for the first experiment using paste 1 and 2 and the metallization paste with the highest glass frit content. Firing profiles for the isolating layers had different peak temperatures (above 600 °C). Long (about 30 min) and short firing profiles, similar to metallization firing, were used as well as co-firing of isolating paste and metallization. Typical profiles are displayed in Figure 6.17.

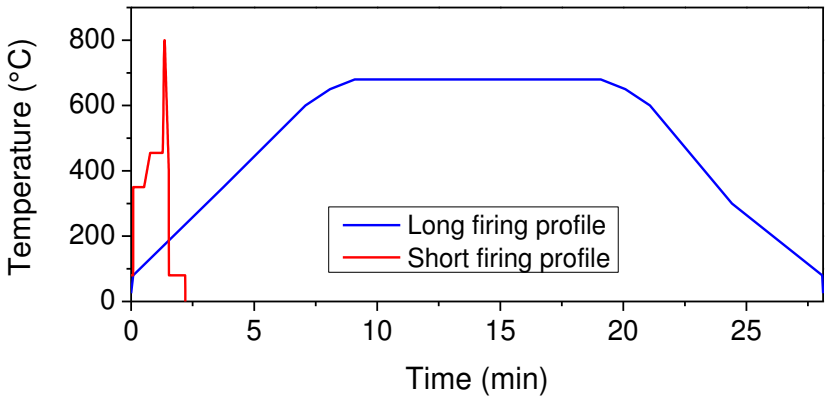

Figure 6.17: Typical profiles of long and short firing processes for isolation pastes.

The isolating properties of the pastes were not affected by changes in firing profiles, as even the pastes on the co-fired samples could isolate against the silver metallization.

Firing isolation paste 1 with a long (approx. 30 min) firing profile at temperatures beyond a limiting temperature (T_{limit}) induced the paste to crystallize causing severe tension that broke the wafer, see Figure 6.18. However, after any other firing profile, no change in the paste was visible by eye or in microscopy images. Short firing profiles above the limiting temperature of paste 1 seemed to have a negative effect on the adhesion of the paste. Although the adhesion problems with paste 1 could not be fully avoided, long firing profiles at lower temperatures led to better adhesion of the isolation layer on the silicon nitride. Similar results could be obtained by co-firing the isolation with the metallization. Overall paste 1 did not perform as well in the second experiment as the first, as blistering occurred especially underneath the metallization finger which was not the case in the first experiment. An unintended difference of the metallization firing profile could be the reason for blistering.

Figure 6.18: Paste 1 after firing above the limiting temperature (left) and after firing at lower temperatures with metallization on top (right).

Paste 2 shows a clear difference in color before and after firing. It also has a limiting temperature above which blistering occurs using long firing profiles. T_{limit} of paste 2 is above the firing temperature suggested by the manufacturer but still below the limiting temperature of paste 1. Microscopy images of the paste after firing are displayed in Figure 6.19 and show the structural change of the paste at different temperatures. Firing below the T_{limit} did not lead to blistering, which started in individual areas after firing at T_{limit}. After firing above the limiting temperature blistering occurred over the whole area. However, the blistering had a positive effect: the isolating properties of the paste were not affected and the adhesion of the metallization was very good, since no bubble formation beneath the contacts occurred. A short firing profile and co-firing with the metallization led to better adhesion than a long firing profile at temperatures below the limiting temperature. However, these layers could not perform as well as the blistering layer. An overview of the influence of firing parameters on the adhesion of paste 1 on the wafer and the metallization on isolating paste 2 is presented in Figure 6.20.

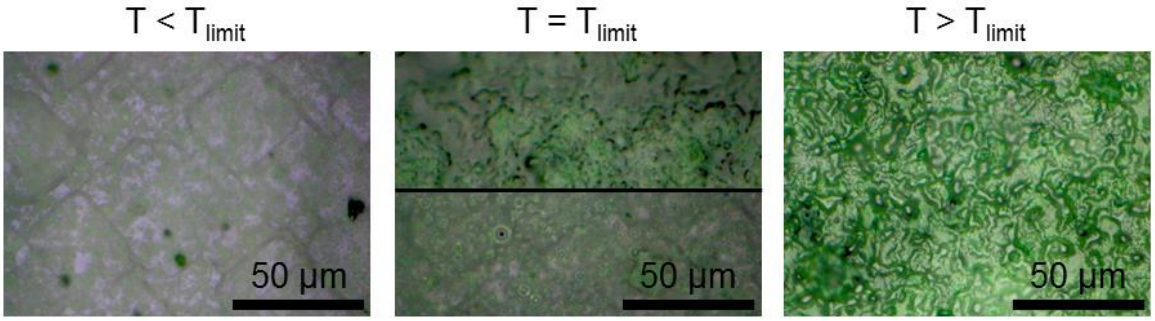

Figure 6.19: Paste 2 after firing with a long firing profile at different peak temperatures. Below the limiting temperature (left) no blistering can be seen, at the limiting temperature (middle) there are areas with and without blistering and above the limiting temperature (right) blistering occurs over the whole area.

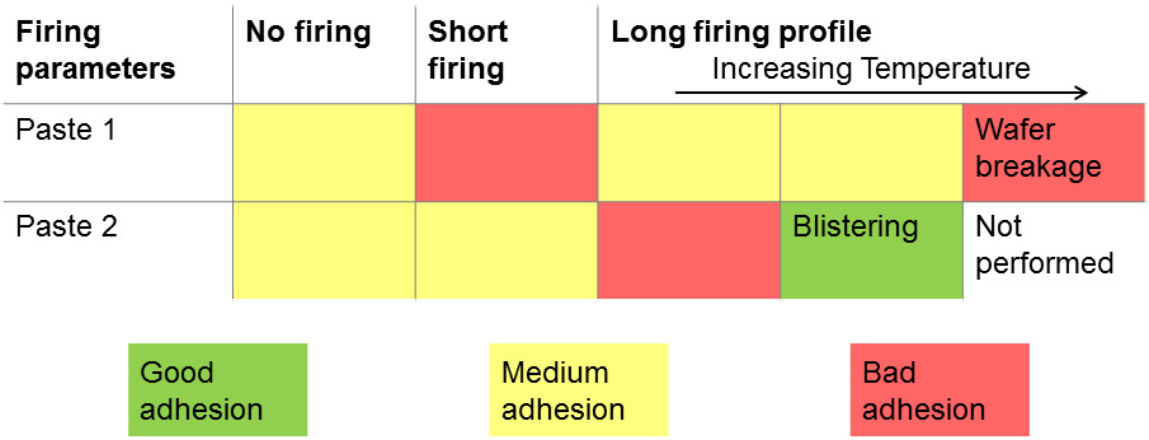

Figure 6.20: Summary of the firing parameter optimization concerning the adhesion between isolating layer and wafer for paste 1 and between isolating layer and metallization for paste 2.

6.2.4 Print image of fingers

The print image of the metallization fingers varied depending on the surface. An especially interesting parameter is the width of the finger as it determines the shading loss. As the MWT pastes were not optimized to fire through SiN_x and form narrow fingers, they were not expected to perform as well as the standard paste. However it is interesting to investigate the influence of the isolating pastes on the finger width, especially at the edge of the isolating layer. In Figure 6.21 the finger widths of the different metallization pastes on SiN_x and the isolating pastes, fired according to manufacturer's data, are shown. The standard metallization paste performs similarly well on all materials with a finger width of 70-80 µm. MWT paste 1 showed narrower fingers on all isolating pastes than on SiN_x and MWT paste 2 only shows a significantly reduced finger width on isolating paste 1. The standard metallization paste also showed no broadening of fingers in combination with optimized firing parameters and isolating paste 2.

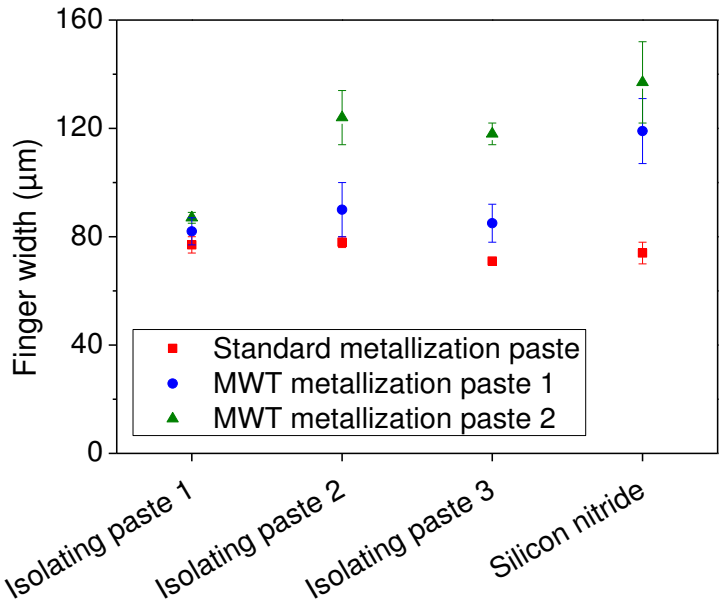

Figure 6.21: Finger width of the metallization pastes on different surface materials, measured by cross-section polished samples.

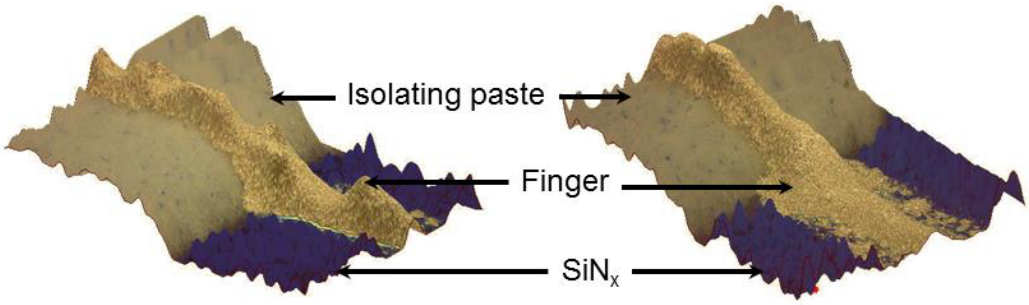

Figure 6.22: 3-dimensional images calculated from z-stack of microscopy pictures. The finger of the metallization paste runs across SiN_x and a layer of isolating paste 1. Left: Standard metallization paste; Right: MWT metallization paste 1.

The reduction in finger width of MWT metallization paste 1 can be seen in Figure 7.1. The finger narrows as it is printed on isolating paste 1 compared to on SiN_x. For the standard metallization paste the finger geometry does not change and no significant broadening at the edge of the isolating layer can be seen.

6.2.5 Summary – Screen-printing interconnection

In summary, two different screen printing pastes were found that isolated against all tested silver metallization pastes. For paste 1 adhesion problems could be reduced by firing parameter optimization, for paste 2 they could be completely solved. The finger width of the standard metallization paste on isolating pastes 1

and 2 is in the same range as on silicon nitride. The structure of the test samples is much more challenging concerning adhesion than the final application, since in the interconnection concept the isolation is only applied at the trench edge and the silver fingers run across it perpendicularly. Therefore both pastes should be suitable for this module concept.

Recent developments in non-contacting via pastes for metallization wrap through (MWT) [59] concepts could prove beneficial for interconnection concepts. Via pastes are being developed which only form a contact to the desired polarity. A via paste forms the external contacts on the rear and connects them to the fingers on the front side. For concepts without a rear side emitter the via paste has to show a non-contacting behavior towards the base of the cell [60]. Lohmüller et al. show experiments and cell results with different non-contacting via pastes in [60]. In an integrated interconnected module scheme non-contacting pastes could be used for the interconnection and, depending on the paste, simultaneously as emitter fingers. Another paste would then be used for contact formation to the base. The screen-printing approach of integrated interconnected thin-film module can directly benefit from advances made in MWT wafer cell technology.

A yet untested challenge is how well screen-printing at trench edges or steps works. In [61] RexWE solar cells were fabricated using screen-printing metallization. The finger in Figure 6.23 widens at the grain boundary due to height differences. The broadening would not cause severe shading losses as there is no active layer in the trench. On the other hand the finger thickness at the trench edge has to be investigated as a thinning would lead to resistive losses.

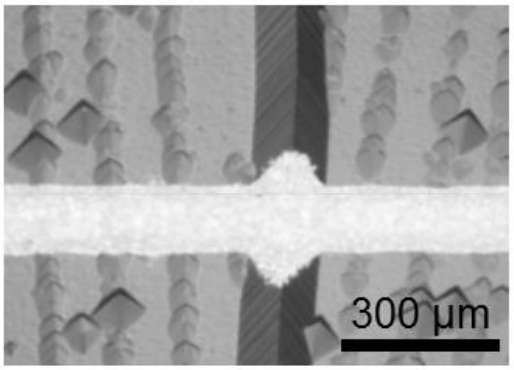

Figure 6.23: Picture of emitter finger printed across a grain boundary of a RexWE solar cell [61].

7 SOLAR CELL RESULTS

The processing sequence, module layout and actual results of the fabricated mini-modules are illustrated in this chapter. The effect of sintering time and temperature as well as cell strip width are discussed by means of cell results and are compared to simulations, in the case of the cell strip width. The compatibility of the mini-modules with a standard encapsulation process is also shown.

Integrated interconnected modules were fabricated with processing steps detailed in the chapters above. A texture was not applied, but could easily be included before $POCl_3$ diffusion. The processing sequence is displayed in Figure 7.1. The trenches were formed by oxide masking and KOH etching (see section 5.1.1) and the emitter was structured in a plasma etching process (see section 5.2.1). For the interconnection photolithographic structuring steps and SiN_x isolation in combination with evaporated contacts (see section 6.1) were used.

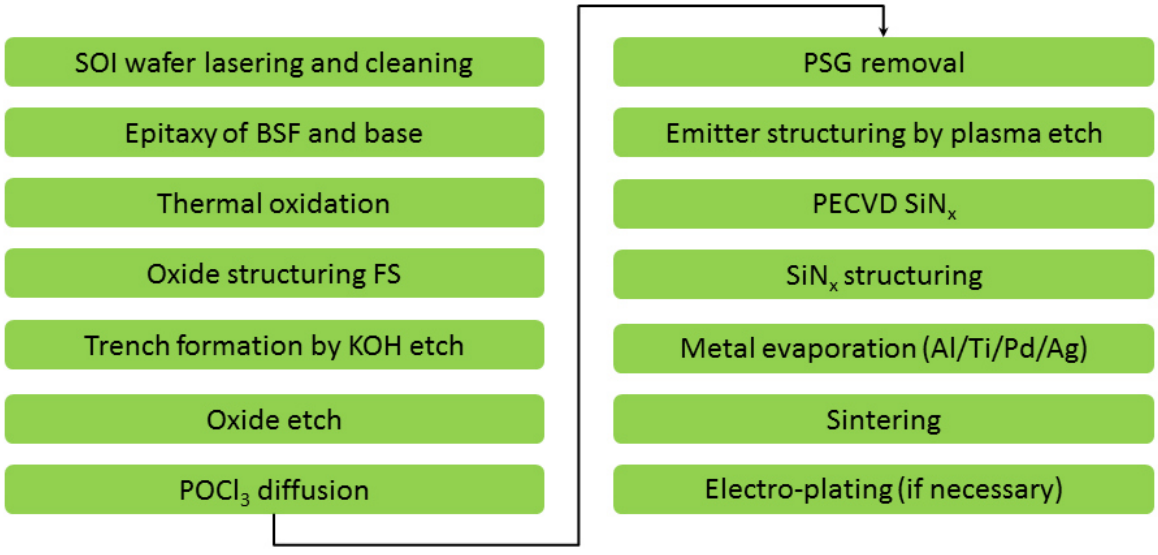

Figure 7.1: Processing sequence for fabricated mini-modules on SOI material.

7.1 Module layout

A sample size of 5 x 5 cm² was chosen for the fabrication of the mini-modules. Photolithography masks were designed for the laboratory process and their layout will be introduced here. To fabricate modules with cell strip widths of 3, 5 and 10 mm, as discussed in 3.3, two sets of masks were designed. One set has 3 and

5 mm wide cell strips with 2 and 5 cell modules each and the other has 10 mm cell strips with a 2 and a 4 cell module. A plot of the two mask sets can be seen in Figure 7.2. Every module has large contacting pads on each side for the IV measurement and characterization of the modules. Two sets of alignment keys are required, as one is etched away during KOH etching of the trenches. After generation of the alignment keys, four different masks have to be aligned to the sample. Therefore the accuracy of alignment must be taken into account, when designing a set of masks. A safety margin of 50 µm was used and for the 3 and 5 mm wide cell strips a safety margin of 10 µm was also tested. Square-cut control structures were included to confirm sufficient alignment. Also a process control window was added where SiN_x is etched on a larger area during the SiN_x structuring process. In contrast to a silicon surface with SiN_x coating, a clean silicon surface is hydrophobic, which can be surveyed by eye on the process control window.

A detail of the masks at the interconnection of two cells and the edge of the module can be seen in Figure 7.3. The emitter area is yellow, the contacts grey, the SiN_x openings are depicted blue and the trench green. For the trench etching the oxide is etched in 10 µm wide lines (dark green), but the trench widens to approx. 120 µm (lighter green) during KOH etching.

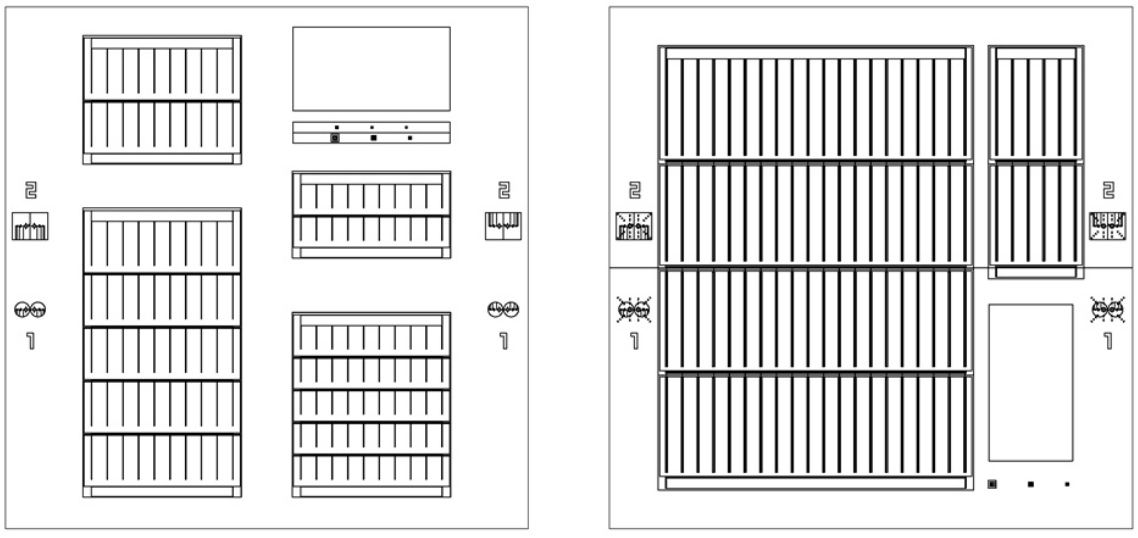

Figure 7.2: Plot of the photolithography masks for processing of mini-modules on 5 x 5 cm.

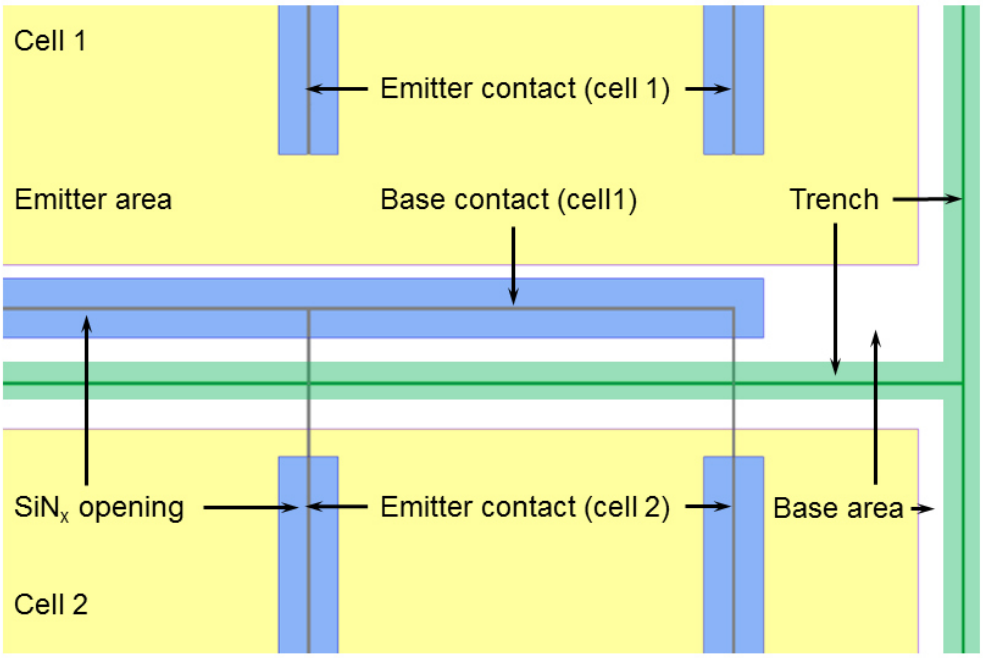

Figure 7.3: Detail of photolithography masks at the interconnection of two cells at the edge of the module.

Table 7.1: Cell and module areas of fabricated mini-modules.

Cell strip width (mm)	Number of cells in module	Cell area (cm^2)	Module area (cm2)
3	2	0.45	0.912
	5	0.45	2.316
5	2	0.75	1.512
	5	0.75	3.816
10	2	0.90	1.7919
	4	3.00	12.045

The cell and module areas of the fabricated mini-modules are listed in Table 7.1. The denoted areas are the ones later used in calculation of short circuit current and efficiency. The trenches between the cells are included in the calculation of the module area, the contacting pads on the side of the modules are not included.

7.2 The first module batch

In the first mini-module batch the epitaxially grown layer consisted of 5 µm BSF with a boron doping concentration $5 \cdot 10^{18}$ cm^{-3} of and 30 µm base with a doping concentration of $4 \cdot 10^{16}$ cm^{-3}. SiN_x A from the laboratory scale tool (see 6.1.1) was used as isolating layer. The interconnection was interrupted and had to be fixed with conductive silver before electro-plating, as described in 6.1.2. As the processes of electro-plating and sintering had to be optimized, the samples were processed individually. The parameters for electro-plating were adjusted accordingly. Fingers peeled partially off the wafer during electro-plating. To increase the contact between aluminum and silicon, the next mini-modules were then sintered at 350 °C for 10 min before electro-plating, which lead to better contact adhesion. Nevertheless most of the fully processed mini-modules were electro-plated before and after sintering. Therefore they exhibit partly peeled off fingers, which lead to an increased series resistance.

The resulting solar cell parameters of the mini-modules are listed in Table 7.2. As pointed out above, the module area for the efficiency calculation includes the trenches between the cell strips. The contacting pads for the measurements are not included.

The successful interconnection can be seen in the V_{OC} values. An average open circuit voltage of up to 620 mV per cell was measured, which lies in the expected range considering the use of a 40 Ω/□ emitter. In a previous experiment FZ wafer solar cells with the same emitter also showed a V_{OC} of 620 mV. As already shown in Table 6.2 the individual V_{OC} of each cell of the module adds up to the V_{OC} of the mini-module. A mini-module consisting of five cells was fabricated achieving a V_{OC} over 3 V.

Table 7.2: IV parameters of the best integrated interconnected mini-modules. The pseudo fill factor was measured by SunsV_{OC}. * After consecutive sintering, see 7.2.1.

Cell width (mm)	Number of cells	V_{OC} (mV)	J_{SC} (mA/cm²)	FF (%)	η (%)	pFF (%)
3	2	1229	26.3	31	4.9	76
5	2	1240	27.5	52	8.8	60*
10	2	1132	22.4	37	4.7	-
5	5	3055	27.3	53	8.7	74
10	4	2494	24.2	38	5.6	78

As the mini-modules are not textured and have a 30 µm thick absorber the J_{SC} of up to 27.5 mA is in the expected range.

The fill factor of the modules ranges from 31 to 53 %. The origin of these low values was assumed to lie in an increased series resistance. This was confirmed by SunsV_{OC} measurements, which provide IV curves without the effect of series resistance. The cells of each module had to be measured individually in the SunsV_{OC} measurement. The listed pseudo fill factor (pFF) is therefore the average value. The pFF measured by SunsV_{OC} reaches up to 78 %, which shows that high fill factors are in principle achievable (see Table 7.2). The resulting increased series resistance can be partly attributed to the metallization problems. This is why an effect of cell strip width on series resistance cannot be distinguished from the effect of the contacting issues on the series resistance.

7.2.1 Effect of sintering

An increased series resistance due to a high contact resistance can often be reduced by sintering. On the other hand it is known that aluminum tends to spike through the emitter and create shunts after longer sintering times. Two modules were therefore sintered consecutively for different times and at different temperatures to investigate both effects. Both modules are 2-cell modules with 5 mm cell strip width. They were first measured after sintering for 10 min at 350 °C. The second sintering step was also at 350 °C but for 25 min and the third at 400 °C for 15 min. The IV parameters are listed in Table 7.3 and the corresponding IV curves of module 1 in Figure 7.4.

It can be seen that for module 1 the V_{OC} remains at the same level after the second sintering step, while there is little decrease in J_{SC} of 2.2 mA/cm² and the FF is reduced by 19 % abs. resulting in a 3.6 % abs. efficiency decrease. As the modules already have an increased series resistance, it is hard to fit the IV measurements with the two diode model. Nevertheless, the change of the IV curve suggests an increase in series resistance after the second sintering step. For further sintering the trend continues with an additional decrease in V_{OC}. The relatively stable V_{OC} compared to J_{SC} and FF indicates an effect of series resistance and not parallel resistance.

Module 2 shows a similar behavior as module 1 with a severer decrease in performance.

To ascertain the origin of the degradation of mini-modules after further sintering steps, a closer look at SunsV_{OC} measurements of module 1 was taken. The parameters from the SunsV_{OC} measurement are included in Table 7.3. As the cells in the module had to be measured separately the V_{OC} is the sum of the measured values, while pFF and pseudo efficiency are averages of the individual cells. The pseudo efficiency was calculated with a J_{SC} of 27.5 mA/cm². The pFF from SunsV_{OC} is considerably higher than the FF from IV measurements and the V_{OC} from SunsV_{OC} is in the same range as the one from IV measurements after the first sintering. The stable V_{OC} and FF prove that the aluminum did not spike through the emitter and create shunts. The losses can be attributed to the series resistance, which was further increased by consecutive sintering. The interconnection of these modules had to be done using conductive silver, whose conductivity apparently is affected by the sintering process.

Table 7.3: IV parameters of two 2-cell modules after consecutive sintering at 350 and 400 °C and SunsV_{OC} measurements of module 1 after all sintering steps.

		Module	**V_{OC} (mV)**	**J_{SC} (mA/cm²)**	**FF (%)**	**η (%)**
350 °C	10 min	Module 1	1240	27.5	52	8.8
		Module 2	1238	27.0	46	7.6
350 °C	25 min	Module 1	1237	25.3	33	5.2
		Module 2	1164	11.5	20	1.3
400 °C	15 min	Module 1	1194	13.9	23	1.9
		Module 2	929	0.1	11	0.0
					pFF (%)	**pη (%)**
SunsV_{OC}		Module 1	1232	-	60	10.25

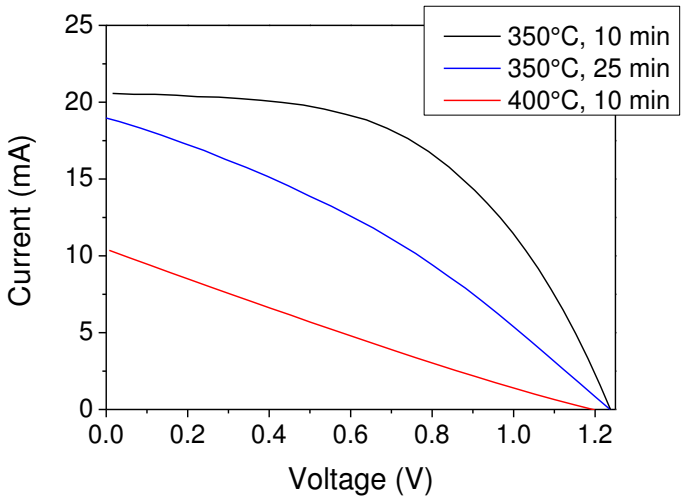

Figure 7.4: IV measurements of 2-cell module (module 1) with 5 mm cell strip width after different sintering times and temperatures.

7.3 Consecutive module batch

In the following module batch the doping profile which was simulated (see 3.3.3) was used. A stack of 15 µm thick BSF with a doping concentration of $1 \cdot 10^{18}$ cm^{-3} and 25 µm base with $4 \cdot 10^{16}$ cm^{-3} doping concentration was epitaxially grown. The trenches were again etched as in the first batch and SiN_x A from the laboratory tool was used as isolating layer. For the interconnection of the 10 mm wide cells the negative photoresist was used in combination with thick evaporation of metal as described in 6.1.2. Afterwards the mini-modules were sintered either for 25 min at 350 °C or 15 min at 400 °C. In spite of using the negative resist, the interconnection was not always successful and cells had to be interconnected with conductive silver in some cases. The 3 and 5 mm wide cells were metallized with the double exposure also described in 6.1.2. The samples were sintered at 350 °C for 20 min and the evaporated metallization was thickened by electro-plating.

The cell results are distributed over a wide range. The IV parameters of the best mini-module of each group can be found in Table 7.4. 2-cell modules with 3 mm cell strip width exhibited the highest efficiencies of up to 8.9 %. The J_{SC} lies in the expected range as in the modules of the first batch. For the two-cell modules M2-3 and M2-10 the V_{OC} reflects the interconnection of two cells with an average of 540 to 600 mV while in M2-5 either both cells have a reduced V_{OC} or one cell was short circuited and does not contribute to the module.

Table 7.4: IV parameters of the best mini-module of each group.

Module	Cell width (mm)	Number of cells	V_{OC} (mV)	J_{SC} (mA/cm²)	FF (%)	η (%)
M2-3	3	2	1204	24.3	62	8.9
M2-5	5	2	601	26.9	36	2.9
M2-10	10	2	1084	24.2	30	3.9
M5-3	3	5	2393	24.3	41	4.6
M5-5	5	5	2403	25.6	41	5.0
M4-10	10	4	2360	18.6	23	2.5

Single cell measurements are shown in Table 7.5 and confirm that cell 1 was short circuited. Cell 1 has a J_{SC} of 11.6 mA/cm², which should also be the limit of the module, but the module has a J_{SC} of 26.9 mA/cm² and the other cell parameters show that cell 1 is not a solar cell. The V_{OC}, J_{SC} and FF of cell 2 fit well to the module measurement and calculating the efficiency with these parameters but the whole module area adds up to 2.6 %. Cell 1 does thus not contribute to the module efficiency.

Table 7.5: Single Cell IV parameter measurements of module M2-5 in comparison with the calculated and measured module parameters.

Cell / Module	V_{OC} (mV)	J_{SC} (mA/cm²)	FF (%)	η (%)
Cell 1	17	11.6	25	0.0
Cell 2	580	26.2	34	5.2
η calculated from parameters of cell 2 with the area of the whole module				2.6
Module (measured)	601	26.9	36	2.9

Spectral response measurements were conducted on cell 1 of module M2-5 and are displayed in Figure 7.5. The run of the IQE curve is similar to other crystalline silicon thin-film solar cells. In the short wavelength range the IQE is decreased due to a not well passivated front side of the cell. It could therefore be improved by optimizing the emitter and surface passivation. In the long wavelength range the IQE is decreased due to the thickness of the absorber layer and no implemented light-trapping. It is for example comparable to the cells fabricated on SOI that are shown in Figure 4.34 (section 4.5.5) with a planar front surface.

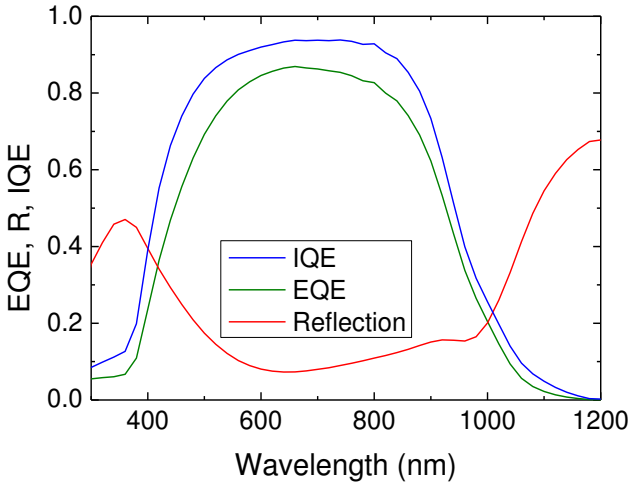

Figure 7.5: IQE, EQE and reflection of one cell of a mini-module (M2-5) with 5 mm cell strip width.

As discussed in 4.5.5, light-trapping increases the IQE in the long wavelength range and leads to an increased J_{SC}.

Compared to the first cell batch, the fill factor could be increased to up to 62 %. Nevertheless a FF above 60 % was only achieved in modules with 3 mm cell strip width. The impact of cell strip width on the cell parameters will be discussed in the next section.

7.3.1 Effect of cell strip width

Fill factor and efficiency of all modules of this batch with a measurable efficiency are displayed in Figure 7.6 in dependence on cell strip width. There is a wide distribution of results due to interrupted interconnection as described in section 6.1.

It should be noted that originally the same amount of modules for each cell strip width was fabricated, but with different success rates. While all modules with 3 mm cell strip width were successfully processed into solar modules, 80 % of the modules with a 5 mm cell strip width and only 30 % of modules with a 10 mm cell strip width generated power under illumination. For the samples with 10 mm wide cell strips a different metallization process was used and the heavy drop in yield for these modules could be attributed to that, as it is not expected that the cell strip width is connected to the processing yield. Nevertheless, a small number of working modules affects the significance of a statistical analysis.

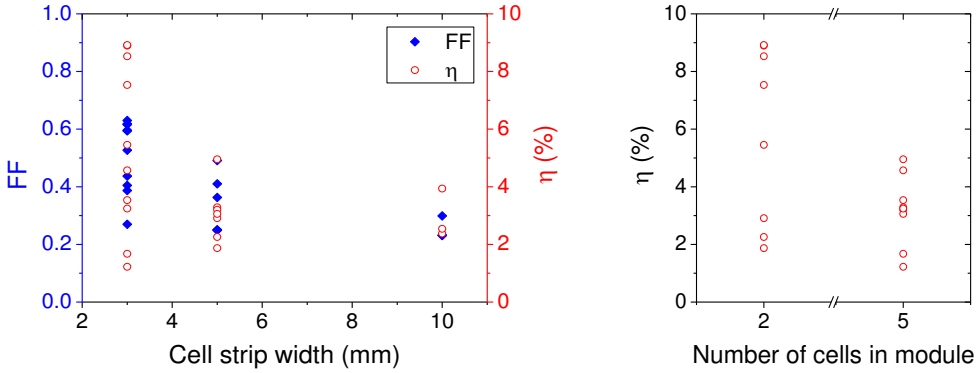

Figure 7.6: Fill factor and efficiency of fabricated mini-modules in dependence on cell strip width (left) and efficiency dependent on the number of cells (right).

In the right graph of Figure 7.6 a correlation between the number of cells in a module and the module efficiency can be seen. The 10 mm wide cells were excluded from this graph, as no 5-cell modules were fabricated with a 10 mm cell strip width. The efficiency loss due to an increased number of cells in the module is related to a not yet optimized process. A defect in one cell limits the module efficiency and the more cells a module has, the higher the probability that one of them has a defect. In an optimized process the probability of a defect is minimized and the correlation of efficiency on number of cells would decrease drastically.

Nevertheless, a trend of decreasing FF and efficiency with increasing cell strip width is visible in the left graph in Figure 7.6, especially considering the maximum values. This trend follows the prediction and simulation of section 3.3, but due to the variance in IV parameters it has to be verified by further experiments.

For the further investigation of the cell strip width on the module performance only 4- and 5-cell modules are used. In Figure 7.7 an overview of J_{SC}, V_{OC}, fill factor and efficiency in dependence on cell strip width is given. The module with the highest J_{SC} has a cell strip width of 5 mm, but due to the variance of the modules in one group no trend can be observed. The simulation (see 3.3.3) predicted an increase in J_{SC} for increasing cell strip width up to 8 mm. For 10 mm wide cell strips there is a decrease in J_{SC} in the fabricated mini-modules. This decrease can be attributed to a very high series resistance which can be qualitatively observed in the progression of the IV curves shown in Figure 7.8. The modules with 3 and 5 mm cell strip width already exhibit an elevated series resistance, which can be seen in the slow increase in current near the V_{OC}. For the module with 10 mm cell strip width the current increases even more slowly and

does not reach a plateau near the J_{SC}. The high series resistance in combination with a higher current limits the current density.

The variance in V_{OC} of the mini-modules shows that in some cases the interconnection was not successful and one or more of the cells were short circuited as module M2-5. The V_{OC} is not influenced by the cell strip width, as the simulations and experiments on edge effects (see section 3.3.4) predict. The used SiN_x was not optimized for passivation and therefore the surface recombination velocity is high, which fits to the drop in the short wavelength IQE shown in Figure 7.5. Thus the iSiMo mini-modules can be compared to the lifetime samples with trench structure before application of the passivating layer, discussed in section 3.3.4. For these samples, the reduced surface recombination velocity at the step of the pn-junction did not visibly influence the effective lifetime as the effective lifetime was at a low level of 13 – 16 µs in areas with emitter. When the pn-junction does not affect the effective lifetime, the V_{OC} cannot be influenced by the cell strip width, which is the case for the modules of this batch.

As already stated, the maximum fill factor values decrease with increasing cell strip width, but as processing issues described in section 6.1 also affect the fill factor, a definite statement on the influence of the cell strip width is not possible.

The efficiency depends on all three parameters and is similarly distributed for modules with 3 and 5 mm cell strip width. For 10 mm strips the efficiency is reduced mainly due to the limited fill factor.

The limited number of samples as well as variation in IV parameters due to processing issues prohibit a final conclusion on the best suited cell strip width, but suggest that the optimum lies in the considered range of 3 to 10 mm.

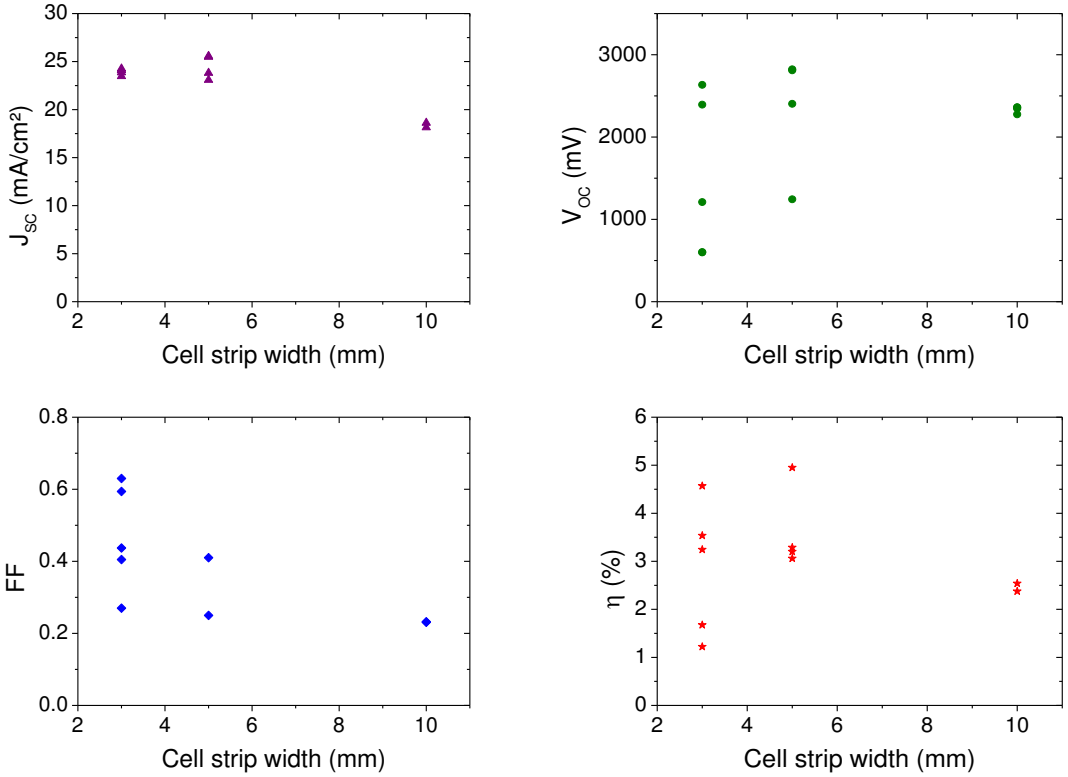

Figure 7.7: IV parameters of 4-cell modules in the case of 10 mm cell strip width and 5-cell modules in the case of 3 and 5 mm cell strip width dependent on cell strip width.

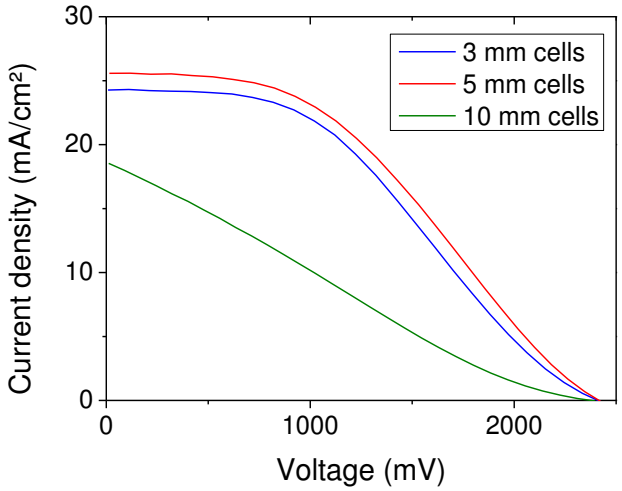

Figure 7.8: IV measurement of 4 cell module with 10 mm cell strip width (M4-10) and 5 cell modules with 3 and 5 mm cell strip width (M5-3, M5-5).

7.4 Module encapsulation

Two mini-modules of the first module batch with 10 mm cell strip width were encapsulated between glass and a white back sheet with ethylene vinyl acetate (EVA) in a standard module encapsulation process, see Figure 7.9.

The comparison of IV measurements before and after encapsulation is shown in Table 7.6. As before, the module area includes the trenches between the cells. The area around the mini-modules was shadowed by a black mask to reduce the influence of the reflecting back sheet. The area between the mini-modules was not covered, which lead to a slight increase in J_{SC} of about 0.5 mA/cm² after encapsulation due to the reflection of the back sheet in the area between the mini-modules. Calculating the efficiency of the mini-modules after encapsulation with the J_{SC} they had before encapsulation leads to the same efficiency before and after encapsulation in case of mini-module 1. In case of mini-module 2 the efficiency decreases slightly by 0.1 % abs. It can therefore be concluded that the mini-modules are in principle suitable for standard encapsulation.

The two modules were also interconnected serially. In this case the voltage of both mini-modules adds up to 4.8 V, as expected. The resulting fill factor and efficiency lie between the values of the single modules.

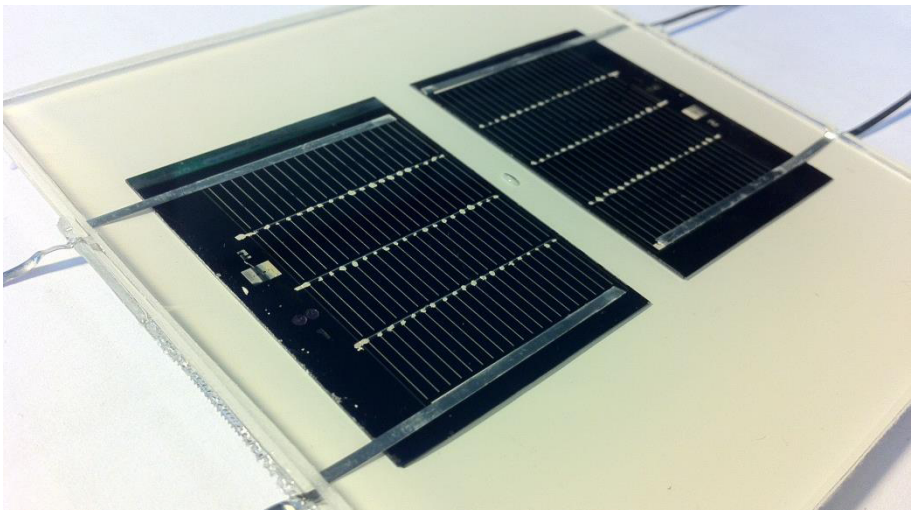

Figure 7.9: Picture of encapsulated mini-modules.

Table 7.6: IV parameters of mini-modules before and after encapsulation. The area around the mini-modules was shadowed by a mask to reduce reflection of the back sheet.

Mini-module	**V_{OC} (mV)**	**J_{SC} (mA/cm²)**	**FF (%)**	**η (%)**
1 – not encapsulated	2494	24.2	38	5.6
2 – not encapsulated	2359	23.3	35	4.8
1 – encapsulated	2478	24.6	38	5.7
2 – encapsulated	2341	23.9	35	4.9
1 and 2 connected serially	4806	24.9	36	5.4

7.5 Summary – module results

A processing sequence as well as the design of the used photolithography masks was introduced. In the frame of this thesis two successful batches of mini-modules were fabricated. Each batch included modules with 3, 5 and 10 mm wide cell strips consisting of 2 and 5 cells (for 3 and 5 mm) or 2 and 4 cells (for 10 mm). The modules exhibited efficiencies up to 8.9 % and a V_{OC} larger than 3 V for a 5-cell module was reached. The main limitation was the fill factor, which could be increased up to 63 % due to optimizations in the metallization process. Nevertheless further optimizations in the metallization process could enhance the fill factor and thereby the module performance.

A definitive conclusion about the optimum cell strip width for iSiMo modules fabricated in this processing sequence cannot be drawn from the module results, as processing issues also affect the module parameters and cannot considered separately. The parameters are distributed quite broadly, but show a trend of increasing fill factor with wider cell strips due to increased series resistance. This effect is in good agreement with the simulations.

Encapsulation of two mini-modules in a standard EVA process turned out to be suitable for this concept. The encapsulation did not decrease the module performance.

8 SUMMARY

The iSiMo (integrated interconnected crystalline silicon thin-film module) concept, which was the main topic of this thesis, combines the classical thin-film approach of interconnected cell strips with crystalline silicon wafer technology. In order to transfer the idea to an actual mini-module, the module layout was evaluated, especially with respect to the optimum cell strip width, which was found to lie in the range of 3 to 10 mm. A processing sequence was developed for a laboratory scale process, selected processing steps were investigated in more detail and preliminary tests were done for the transfer to industrially feasible processes.

One of these processes was plasma texturing, which could not yet be applied to the fabricated mini-modules but to other thin-film and wafer solar cells. It is a crucial process for the iSiMo concept as crystalline silicon thin-film solar cells need excellent light-trapping to compensate the thinner absorber and be competitive to wafer solar cells. Plasma texturing processes were developed in two different tools and wafer as well as thin-film solar cells were fabricated. In combination with a reflective rear side, the light-trapping effect of the texture could be shown. Using a single layer ARC, the texture lead to a low reflection over a wide wavelength range, compared to a planar surface, and to an increase of 1.8 % abs. in efficiency for wafer solar cells, demonstrating the applicability of the developed plasma texture also to wafer solar cells.

The first step for processing of an iSiMo module is the separation of the silicon film into cell strips. In the fabrication of the mini-modules, this was done by KOH etching using a photolithographically structured SiO_2 as mask, which is a comparatively complicated process and therefore not suitable for industrial production. As an alternative, laser processing was investigated with two different laser systems and showed promising results. In combination with a subsequent etch step to remove residual silicon in the laser-trench, the cell strips could be isolated completely. The best option for a subsequent etch step is considered to be plasma texturing, as this can simplify the overall processing sequence. The second silicon structuring process that was investigated is emitter structuring, which was done by plasma etching. For the mini-modules a photoresist was used as mask, which could be replaced by a printed mask in an industrial process.

Other solutions like the application of a structured diffusion barrier prior to emitter diffusion are possible but were not investigated.

To realize the actual interconnection of the cell strips into a module, two approaches were followed: the laboratory scale solution with evaporated contacts , which was used in the fabricated mini-modules, and screen-printed contacts for industrial implementation. In order to interconnect two cells, the emitter fingers need to cross the lateral pn-junction parallel to the trench, which needs to be isolated against the contacts. The isolation material must be chosen depending on the used contacting material and method. For the evaporated contacts different PECVD (plasma enhanced chemical vapour deposition) silicon nitride layers were evaluated in regard to passivating and optical properties as well as structurabilty. Aluminum was chosen as contacting material because it shows a low contact resistance to moderately doped p-type silicon and highly doped n-type silicon. All structuring steps were realized by photolithography, where different resists were used for silicon nitride structuring as well as for the metallization process to ensure accurate results despite the steps and trenches of the mini-modules. Using screen-printing metallization a silicon nitride layer is not sufficient as isolation, which is why isolating screen-printing pastes were tested in combination with different silver metallization pastes. Two of the isolating pastes could prevent a contact formation and occurring adhesion problems could be improved for one paste and completely solved for a second paste by firing parameter optimization.

In the development of a new cell or module concept, every single processing step can be optimized for the desired application, which was unfortunately not completely possible in the frame of this thesis. Nevertheless, mini-modules with efficiencies up to 8.9 % were fabricated with the laboratory scale process on SOI (silicon on insulator) wafers with epitaxially grown BSF and base. For a 5-cell module a V_{OC} larger than 3 V was reached. The main limitation was the fill factor, which could be increased up to 63 % due to optimizations in the metallization process. Implementation of light-trapping, e.g. through plasma texturing, would significantly improve the J_{SC} and hence the module efficiency.

As the interconnection is already done with the metallization and the standard EVA encapsulation is compatible with the mini-module process, the module efficiency did not decrease due to encapsulation.

This thesis proves the realization of the iSiMo concept not only on a laboratory scale, but also presents approaches for industrially applicable processes, showing the feasibility of the concept as an alternative module concept for crystalline silicon thin-film photovoltaic beyond wafer technology.

DEUTSCHE ZUSAMMENFASSUNG

Das iSiMo (integriert verschaltetes kristallines Silizium-Dünnschicht Modul) Konzept, das den Kern dieser Arbeit darstellt, vereint den klassischen Dünnschichtansatz von verschalteten Zellstreifen mit der Technologie kristalliner Siliziumwafer. Um die Konzeptidee auf Mini-Module zu übertragen, wurde der Einfluss des Modul-Layouts untersucht, vor allem der der Zellstreifenbreite, deren Optimum, wie sich herausstellte, im Bereich von 3 bis 10 mm liegt. Für die Herstellung von Mini-Modulen im Labormaßstab wurde eine Prozesssequenz entwickelt, in der einzelne Prozessschritte genauer untersucht und Vorversuche für den Transfer hin zu Industrieprozessen durchgeführt wurden.

Einer dieser Prozesse war die Plasmatextur, welche zwar nicht für die Mini-Module verwendet werden konnte, die aber in anderen Dünnschicht- und Wafer-Solarzellen eingesetzt wurde. Dennoch ist sie ein wichtiger Prozess für das iSiMo Konzept, da kristalline Silizium-Dünnschichtsolarzellen ein hervorragendes Light-Trapping benötigen um den dünneren Absorber auszugleichen und konkurrenzfähig mit Wafer-Solarzellen zu sein. In zwei verschiedenen Anlagen wurden Plasmatexturprozesse entwickelt und diese sowohl in Dünnschicht- als auch Wafer-Solarzellen angewandt. Der Light-Trapping Effekt der Textur konnte in Verbindung mit einer reflektierenden Rückseite in Dünnschichtsolarzellen gezeigt werden. Bei Verwendung einer einlagigen Antireflexschicht verringerte die Textur, im Vergleich zu planen Oberflächen, die Reflexion über einen weiten Wellenlängenbereich, führte damit zu einer Effizienzsteigerung von Wafer-Solarzellen um 1,8 % abs. und zeigte so den Nutzen der Plasmatextur auch für Wafer-Solarzellen.

Der erste Schritt zur Herstellung von iSiMo Modulen ist das Trennen des Siliziumfilms in Zellstreifen. Im Prozess der Mini-Module wurde dies mittels KOH Ätzens in Verbindung mit einem photolithographisch strukturierten SiO_2 als Maske realisiert. Dieser im Vergleich komplexe Prozess ist nicht industriell umsetzbar, weshalb alternativ Laser-Prozesse mit zwei verschiedenen Laser-Systemen durchgeführt wurden, welche vielversprechende Ergebnisse lieferten. In Kombination mit einem Nachätzschritt zur Entfernung des Rest-Siliziums aus dem Lasergraben konnten die Zellstreifen vollständig elektrisch voneinander getrennt werden. Als beste Alternative für einen Nachätzschritt konnte die Plasmatextur

identifiziert werden, da durch deren Verwendung der Gesamtprozess vereinfacht werden kann. Der zweite Prozess zur Siliziumstrukturierung, der untersucht wurde, ist die Emitter-Strukturierung, welche mittels Plasmaätzens realisiert wurde. Ein Photolack wurde als Maske für die Mini-Module verwendet, der in einem Industrieprozess durch eine gedruckte Maske ersetzt werden könnte. Andere Lösungen, wie die Verwendung einer strukturierten Diffusionsbarriere, sind möglich, wurden aber nicht untersucht.

Um die eigentliche Verschaltung der Zellstreifen zu einem Modul zu realisieren wurden zwei Ansätze verfolgt: Ein Prozess im Labormaßstab mit aufgedampften Kontakten, der auch für die Herstellung der Mini-Module verwendet wurde, und Siebdruckkontakte für die industrielle Umsetzung. Die Emitterfinger müssen, um zwei Zellen zu verbinden, den lateralen pn-Übergang parallel zum Graben queren, der deshalb von den Kontakten isoliert werden muss. Das Isolationsmaterial muss in Verbindung mit Metallisierungsmethode und –material ausgesucht werden. Für die aufgedampften Kontakte wurden verschiedene mittels PECVD (Plasma-unterstützte chemische Gasphasenabscheidung) abgeschiedene Siliziumnitridschichten im Hinblick auf sowohl Passivierungs- und optische Eigenschaften als auch Strukturierbarkeit untersucht. Aluminium wurde als Kontaktmaterial verwendet, da es geringen Kontaktwiderstand zu sowohl niedrig dotiertem p-typ Silizium als auch hochdotiertem n-typ Silizium aufweist. Alle Strukturierungsschritte wurden mittels Photolithographie umgesetzt, wofür, sowohl für die Siliziumnitrid-Strukturierung als auch für die Metallisierung, verschiedene Photolacke genutzt wurden um trotz der Stufen und Gräben der Mini-Module fehlerfreie Ergebnisse zu erlangen. Für die Siebdruckkontaktierung ist eine Siliziumnitridschicht als Isolation nicht ausreichend, weshalb Isolations-Siebdruckpasten in Verbindung mit verschiedenen Silber-Metallisierungspasten getestet wurden. Zwei der Isolationspasten konnten eine Kontaktbildung verhindern und auftretende Haftungsprobleme konnten durch eine Feuerparameter-Optimierung für eine Paste verringert und für eine zweite Paste vollständig gelöst werden.

In der Entwicklung eines neuen Zell- oder Modulkonzepts kann jeder einzelne Prozessschritt für dieses Konzept optimiert werden, was bedauerlicherweise nicht im Rahmen dieser Arbeit möglich war. Dennoch konnten mit dem Laborprozess Mini-Module auf SOI (Silizium auf einem Isolator) Wafern mit epitaktisch

gewachsenem BSF und Basis mit Wirkungsgraden bis zu 8,9 % hergestellt werden. Ein V_{OC} von über 3 V konnte für ein 5-Zellen Modul erreicht werden. Die hauptsächliche Beschränkung war der Füllfaktor, der mittels Anpassungen im Metallisierungsprozess auf 63 % erhöht werden konnte. Die Implementierung von Light-Trapping, z.B. durch Plasmatextur, würde den J_{SC} deutlich erhöhen und dadurch auch die Effizienz steigern.

Da die Verschaltung schon in einem Schritt mit der Metallisierung erledigt wird und die Standard EVA Verkapselung mit dem Mini-Modul-Prozess kompatibel ist, konnte keine Effizienzreduktion durch den Verkapselungsprozess beobachtet werden.

Diese Arbeit zeigt die Umsetzung des iSiMo Konzepts nicht nur im Labormaßstab sondern beleuchtet auch Ansätze für industrielle Prozesse und demonstriert damit die Umsetzung des Konzepts als alternatives Modulkonzept für kristalline Silizium-Dünnschicht Photovoltaik jenseits der Wafertechnologie.

ABBREVIATIONS

c-Si TF	Crystalline silicon thin-film
EpiWE	Epitaxial wafer equivalent
RexWE	Recrystallized wafer equivalent
iSiMo	Integrated interconnected crystalline silicon thin-film module
PorSi	Porous silicon
SOI	Silicon on insulator
FZ	Float zone
mc	Multi crystalline
mono	Mono crystalline
FS	Front side
RS	Rear side
IL	Intermediate Layer
BSF	Back surface field
PSG	Phosphorous silicate glass
ARC	Anti-reflective coating
DARC	Double layer anti-reflective coating
EVA	Ethylene vinyl acetate
CVD	Chemical vapor deposition
APCVD	Atmospheric pressure chemical vapor deposition
PECVD	Plasma enhanced chemical vapor deposition
RIE	Reactive ion etching
ICP	Inductively coupled plasma
CCP	Capacitively coupled plasma
RF	Radio frequency
MW	Micro wave
ECR-RIE	Electron cyclotron resonance reactive ion etching
ICPRIE	Inductively coupled plasma reactive ion etching
MR	Magnetic ring
SEM	Scanning electron microscope
EDX	Energy dispersive x-ray spectroscopy
TLM	Transmission line model
µPCD/MWPCD	Microwave photoconductance decay

QSSPC	Quasi steady state photo conductance
FF	Fill factor
Voc	Open circuit voltage
Jsc	Short circuit current density
η	Efficiency
SR	Spectral response
IQE	Internal quantum efficiency
EQE	External quantum efficiency

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First author

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Co-author

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