Investigation of Poly-Si/SiO_x Passivating Contacts at Low Thermal Budgets

Doctoral Thesis for Obtaining the Academic Degree Doctor of Science (Dr. rer. nat.)

submitted by

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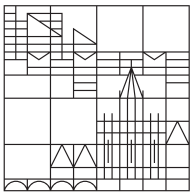

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List of Abbreviations

List of Acronyms

Acronym	Description
Ag	Silver
Al	Aluminum
APCVD	Atmospheric pressure chemical vapor deposition
ARC	Anti-reflective coating
a-Si	Amorphous silicon
B	Boron
B_2H_6	Diborane
BSF	Back surface field
Cu	Copper
CVD	Chemical vapor deposition
c-Si	Crystalline silicon
Cz	Czochralski
DT	Drive-through
ECV	Electrochemical capacitance-voltage
EDX	Energy-dispersive x-ray
FF	Fast firing
FPC	Fired passivating contact
FS	Fused silica
FZ	Float zone
GDOES	Glow discharge optical emission spectroscopy
H_2O	Water
HF	Hydrofluoric acid
HNO_3	Nitric acid
HTPC	High temperature passivating contact
IBC	Interdigitated back contacts
KOH	Potassium hydroxide
LPCVD	Low pressure chemical vapor deposition
MIS	Metal-insulator-semiconductor
MPP	Maximum power point
N	Nitrogen
O	Oxygen
P	Phosphorous

Acronym	Description
PCD	Photoconductance decay
PECVD	Plasma enhanced chemical vapor deposition
PERC	Passivated emitter and rear cell
PH_3	Phosphine
PL	Photoluminescence
PLD	Peroxy linkage defects
Poly-Si	Polycrystalline silicon
PV	Photovoltaic
PVD	Physical vapor deposition
RTP	Rapid thermal processing
SEM	Scanning electron microscope
SHJ	Silicon heterojunction
Si	Silicon
SiH_4	Silane
SiN_x	Silicon nitride
SiO_2	Silicon dioxide
SiO_x	Interfacial oxide
$SiO_{x,inter}$	Interlayer oxide
SPFT	Set peak firing temperature
SRH	Shockley-Read-Hall
TB	Thermal budget
TCO	Transparent conductive oxide
TEM	Transmission electron microscope
TLM	Transfer length method
TMAH	Tetramethylammonium hydroxide
TOPCon	Tunnel oxide passivating contact
TRPL	Time-resolved photoluminescence
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
XRR	X-ray reflectometry
ZnO	Zinc oxide

List of Symbols

Symbol	Unit	Description
A	$\mathrm{A/cm^2K^2}$	Effective Richardson constant
χ	%	Raman crystallinity
Δn	$\mathrm{cm^{-3}}$	Excess charge carrier density
Δn_{av}	$\mathrm{cm^{-3}}$	Average charge carrier density
d_{ox}	nm	Oxide thickness
d_{x}	mm	Finger pitch
E_{A}	eV	Activation energy
D	$\mathrm{m^2/s}$	Diffusion coefficient
ΔE_{s}	meV	Offset between $E_{\mathrm{C/V}}$ and E_{F}
η	%	Conversion efficiency
E_{C}	eV	Conduction band edge
E_{F}	eV	Fermi level
E_{G}	eV	Band gap
ϵ	-	Strain
E_{V}	eV	Valence band edge
FF	%	Fill factor
f_{P}	-	Pinhole fraction
G	$\mathrm{cm^{-3}s^{-1}}$	Generation
iV_{OC}	mV	Implied open circuit voltage
J_0	$\mathrm{fA/cm^2}$	Saturation current density
$J_{0,\mathrm{Met}}$	$\mathrm{fA/cm^2}$	J_0 for metallized areas
$J_{0,\mathrm{Pass}}$	$\mathrm{fA/cm^2}$	J_0 for non-metallized areas
J_{SC}	$\mathrm{fA/cm^2}$	Short-circuit current density
J_{T}	$\mathrm{fA/cm^2}$	Tunneling current
k_{B}	$\mathrm{eV/K}$	Boltzmann constant
L	$\mu\mathrm{m}$	Crystallite size
L_{F}	$\mu\mathrm{m}$	Finger width

Symbol	Unit	Description
m_0	kg	electron mass
m_{eff}	kg	Effective mass
m_{T}	kg	Tunneling mass
μ	$\mathrm{cm^2/Vs}$	Carrier mobility
N_{base}	$1/\mathrm{cm^3}$	Base doping
N_{D}	$1/\mathrm{cm^3}$	Poly-Si doping concentration
N_{P}	$1/\mathrm{cm^2}$	Pinhole density
ω	°	Incidence angle
P_{T}	%	Tunneling probability
Q_{t}	$1/\mathrm{cm^2}$	Charge carrier surface density
r	nm	Pinhole radius
ρ	mΩcm	Resistivity
$\rho_{\mathrm{C/P/T}}$	$\mathrm{m\Omega cm^2}$	Contact resistivity contribution combined/pinhole/tunneling
R_{Aug}	$\mathrm{cm^{-3}s^{-1}}$	Auger recombination rate
R_{C}	Ω	Contact resistance
R_{Rad}	$\mathrm{cm^{-3}s^{-1}}$	Radiative recombination rate
R_{Sheet}	Ω/sq	Contact resistance
R_{Spread}	Ω	Spreading resistance
R_{SRH}	$\mathrm{cm^{-3}s^{-1}}$	SRH recombination rate
R_{Surf}	$\mathrm{cm^{-2}s^{-1}}$	Surface recombination rate
τ	ms	Minority charge carrier lifetime
θ	°	Reflection angle
V_{B}	meV	Grain boundary Barrier height
w	nm	Width of in-diffused region
Z	mm	Finger length

1. Introduction

The global primary energy consumption has steadily increased over the past century, showing no indication of slowing down in the foreseeable future [1]. This rising energy demand must be met. Importantly, fossil fuels such as gas and oil, which contribute significantly to climate change, are unsustainable for long-term use [2]. Additionally, geopolitical factors can destabilize their supply, as evidenced by recent events like Russia's invasion of Ukraine. Few viable alternatives remain beyond renewable energy sources, for example nuclear power. However, political factors and increasing costs have led many countries to plan for nuclear phase-out in the coming years. Moreover, electricity demand is expected to surge in the near future, driven by the shift towards electric vehicles and further economic growth in emerging markets [2]. To meet this demand, renewable electrical energy will play a critical role in the global energy transition [3]. Photovoltaics (PV) is a particularly promising option, as it enables decentralized energy production, reducing reliance on political and economic factors. Furthermore, in recent decades, the cost per kWh of PV-generated electricity has declined steadily, with silicon-based solar cells currently dominating the market, holding over 90% market share [4].

The PV industry is currently transitioning from passivated emitter and rear cell (PERC) technology to tunnel oxide passivating contact (TOPCon) solar cells, with passivating contacts anticipated to become the leading cell concept in the coming years [4]. In the TOPCon approach, the rear contact is typically realized through a stack of polycrystalline silicon (poly-Si) and silicon oxide (SiO_x), instead of diffusing dopants directly into the silicon base. The SiO_x seperates the metal/semiconductor interface from the solar cell bulk, leading to a strong reduction of recombination at the metallized cell areas.

Cost has long been a driver of innovation in the PV industry, where financial competitiveness with other energy sources is essential. Two main strategies for reducing the cost per kWh are available. The first strategy focuses on further enhancing cell efficiency. TOPCon concepts have achieved efficiencies above 26% in laboratory conditions and in industry, nearing the theoretical limit for silicon solar cells [5–7]. Increasing the efficiency further requires more complex fabrication processes, which are typically more expensive. The second strategy to reduce the cost per kWh aims to lower fabrication expenses instead, ideally while maintaining high cell efficiency. Various cost-reduction measures are currently

under investigation. These include minimizing silicon and silver usage or simplifying the process flow to support lean manufacturing.

Typically, the fabrication of poly-Si passivating contacts involves the extended crystallization of amorphous silicon (a-Si) to poly-Si. This work investigates the performance of passivating contacts by reducing the thermal budget of the annealing step or omitting it altogether, potentially lowering the cost per kWh. In order to simplify the fabrication, all annealing is ideally concentrated into a single fast firing step, which is already commonly employed to enhance passivation and enable screen-printing metal contact formation. This method is referred to as *fired passivating contact* (FPC) in contrast to the approach featuring an extended crystallization, which is in this work referred to as *high temperature passivating contact* (HTPC) [8].

Given the central role of passivating contacts in this work, Chapter 2 introduces the theoretical framework and processing steps to fabricate poly-Si/SiO_x based passivating contacts. To effectively examine the properties of passivating contacts, various characterization methods are presented in Chapter 3. In Chapter 4, the impact of different thermal budgets on key contact properties, including dopant in-diffusion, surface passivation, poly-Si resistivity, and crystallite size, is explored for samples without metallization. By varying the annealing time and fast firing temperature for different interfacial oxides, the feasibility of the FPC approach is assessed for different poly-Si layers. Chapter 5 examines charge carrier transport through both the interfacial oxide and poly-Si, as each is critical for achieving optimal solar cell performance. Understanding the factors contributing to macroscopic poly-Si resistance is particularly important for contacts produced with significantly reduced thermal annealing. Finally, Chapter 6 addresses the critical step of metallization using a fire-through silver (Ag) paste, which presents a significant challenge for the FPC approach. A distinctive feature of this work is the use of atmospheric pressure chemical vapor deposition (APCVD) to deposit a-Si layers, with the goal of enabling metallization that achieves good contact quality without significant loss of passivation. The high deposition temperature for APCVD a-Si around 700°C makes APCVD a promising candidate for the FPC approach, as partial crystallization during the deposition may occur [9].

2. Basics of Passivating Contacts

In this chapter, the fundamental concepts of passivating contacts are presented. First, key semiconductor properties for silicon solar cells are outlined. Subsequent sections will discuss the essential characteristics of poly-Si based passivating contacts and their fabrication for this work. This includes the interfacial oxide in Section 2.2, the poly-Si layer in Section 2.3, the annealing processes in Section 2.4, and the metallization of these structures in Section 2.5. Lastly, the state of the art for the fired passivating contact (FPC) approach is introduced in Section 2.6.

2.1. Solar Cell

In order to understand the role and importance of passivating contacts in the PV industry landscape, this section presents general properties of solar cells. In Section 2.1.1, the working principle of a solar cell is explained. Section 2.1.2 discusses efficiency-limiting factors, while surface passivation mechanisms are outlined in Section 2.1.3. Lastly, Section 2.1.4 provides a historical overview of various silicon-based solar cell architectures leading up to the development of passivating contacts.

2.1.1. Working Principle of a Silicon Solar Cell

A crucial physical model for understanding semiconductors, such as silicon, is the *energy band model*. In this model, the discrete energy levels of atoms in a material's lattice structure broaden into energy bands, which are separated by an energy band gap E_G, where no states are available for occupation. The band gap is used to categorize materials into *semiconductors* ($E_\mathrm{G} < 3$ eV), *insulators* ($E_\mathrm{G} > 3$ eV), and *metals*, where the bands overlap [10]. Another important quantity is the *Fermi energy* E_F, corresponding to the energy at which the occupation probability for an electronic state is 50% [11]. In a solar cell, photons with energies E_Ph exceeding the bandgap energy E_G are absorbed, exciting electrons from the valence band (E_V) to the conduction band (E_C), thereby generating electron-hole pairs. The

separation and collection of these charge carriers at the metal contacts require a built-in potential within the cell. This is achieved by doping the silicon crystal with impurities, which introduce additional charge carriers. For instance, doping with elements such as phosphorus (having one more valence electron than silicon) creates excess electrons, forming *n-type* silicon, where the Fermi level shifts closer to E_C. Conversely, doping with elements like boron creates *p-type* silicon, where the Fermi level shifts closer to E_V.
When p-type and n-type silicon are brought into contact, a *pn-junction* forms, which creates a charge carrier concentration gradient. This results in the diffusion of electrons and holes due to their concentration gradients across the junction. The resulting *space charge region* (SCR) creates an electric field that opposes the diffusion flow [10]. This field leads to the built-in potential V_{bi}, which counteracts further diffusion of electrons and holes and reaches an equilibrium when the force due to the electric field balances the diffusion force. In the energy band model, this directly produces a band-bending due to alignment of the Fermi levels on both sides of the junction, as shown in Figure 2.1(a). Under illumination, the cell is in a non-equilibrium state, characterized by the *quasi-Fermi levels* $E_{F,n}$ and $E_{F,p}$, as shown in Figure 2.1(a) and (b) [12]. Figure 2.1(b) also illustrates the *open-circuit voltage* $V_{OC} = E_{F,n} - E_{F,p}$, which quantifies the voltage when no current flows through the circuit [13]. Ideally, without losses, V_{OC} would be equal to V_{bi}.

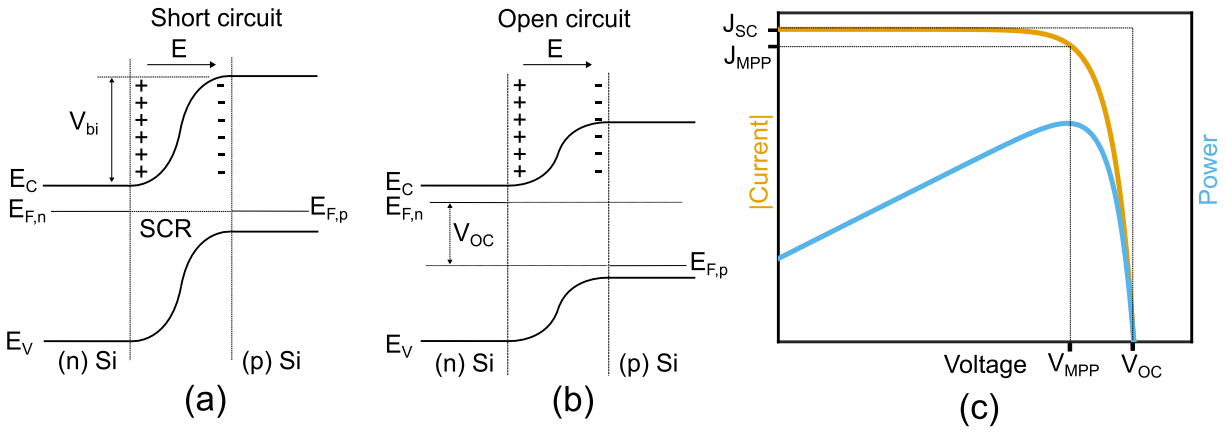

Figure 2.1.: *Band diagrams for a pn-junction are shown under (a) short circuit ($V = 0$) and (b) open circuit conditions ($J = 0$). (c) $J - V$ curve under illumination, highlighting key parameters of the solar cell such as the open-circuit voltage (V_{OC}), short-circuit current (J_{SC}), maximum power point voltage (V_{MPP}), and current at maximum power point (J_{MPP}). The figures are adapted from [10].*

The cell characteristics of a solar cell can be assessed through current-voltage (J-V) measurements, as depicted in Figure 2.1(c). Under illumination, the relationship can be approximated using the one-diode model

$$J(V) = J_0 \left(\exp\left(\frac{qV}{k_B T} \right) - 1 \right) - J_{SC}, \tag{2.1}$$

where k_B is the Boltzmann constant, q is the elementary charge, T represents the temperature, and J_{SC} is the short-circuit current density at $V = 0$ [14]. The parameter J_0, known as the saturation current density, represents all recombination mechanisms and is often used to characterize the quality of passivation in a solar cell. When $J(V) = 0$, Equation (2.1) simplifies to express the open-circuit voltage as

$$V_{OC} = \frac{k_B T}{q} \ln\left(\frac{J_{SC}}{J_0} + 1\right). \tag{2.2}$$

Another critical parameter for evaluating cell performance is the *fill factor* (FF), defined as

$$FF = \frac{J_{MPP} V_{MPP}}{J_{SC} V_{OC}}, \tag{2.3}$$

where J_{MPP} and V_{MPP} correspond to the current and voltage at the maximum power point, as illustrated in Figure 2.1(c) [12]. Finally, the *efficiency* η of the cell, which is the ratio of usable energy at the maximum power point to the incident power P_{in}, can be expressed as

$$\eta = \frac{V_{MPP} J_{MPP}}{P_{in}} = \frac{V_{OC} J_{SC} FF}{P_{in}}. \tag{2.4}$$

2.1.2. Limits of Conversion Efficiency

Ideally, the energy of incoming photons is completely converted into electrical energy. However, several limiting factors prevent this from happening. The theoretical efficiency limit for solar cells, known as the *Shockley-Queisser limit*, is approximately 33% for a solar cell consisting of a single pn-junction [15]. In this model, the sun's radiation is treated as a black body at 6000K. Moreover, it assumes that all incident photons are absorbed and generate electron-hole pairs, and only radiative recombination (explained below) is considered. The primary loss mechanisms for the Shockley-Queisser limit are incomplete absorption of the solar spectrum and thermalization losses. These two processes compete with each other, leading to an optimum band gap E_G, where a significant portion of the incident photons are absorbed ($E_{Ph} > E_G$), while thermal relaxation losses are minimized [15]. In a real cell there are additional loss pathways, namely recombination, optical, and resistive losses, which will be discussed in the following, as it is crucial to understand these in order to reduce them effectively.

Recombination Losses

The inverse process to charge carrier generation is known as recombination. Multiple recombination mechanisms can occur, namely radiative, Auger, Shockley-Read-Hall (SRH), and surface recombination. For each mechanism, a recombination rate R_i and a corresponding minority carrier lifetime τ_i can be defined as

$$\tau_\mathrm{i} = \frac{\Delta n}{R_\mathrm{i}}, \tag{2.5}$$

where Δn is the excess carrier density [16]. The total carrier lifetime τ is given by [12]

$$\frac{1}{\tau} = \frac{1}{\tau_\mathrm{Rad}} + \frac{1}{\tau_\mathrm{Auger}} + \frac{1}{\tau_\mathrm{SRH}} + \frac{1}{\tau_\mathrm{Surf}} = \frac{1}{\tau_\mathrm{Int}} + \frac{1}{\tau_\mathrm{SRH}} + \frac{1}{\tau_\mathrm{Surf}}, \tag{2.6}$$

where τ_Int is the intrinsic carrier lifetime. These recombination mechanisms exhibit different dependencies on charge carrier density, as illustrated in Figure 2.2. Depending on the injection level Δn, different mechanisms dominate.

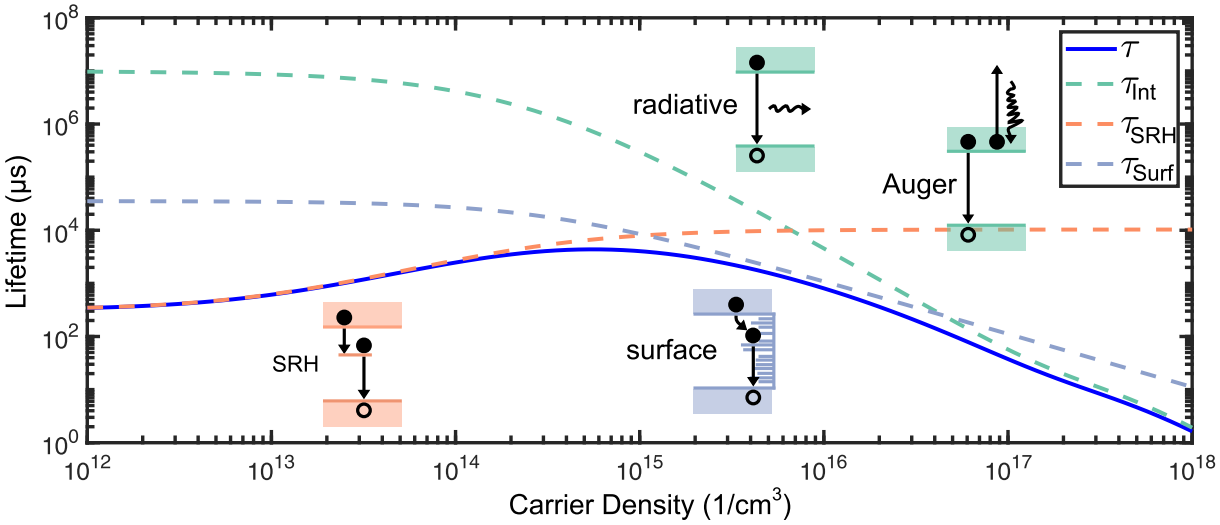

Figure 2.2.: *Computed intrinsic, SRH, and surface minority lifetimes as a function of excess charge carrier density. SRH limits lifetime in low injection, while surface recombination dominates in high injection. Adapted with permission from [17].*

Radiative recombination: Radiative recombination is the reverse process of charge carrier generation under illumination, where an electron in the conduction band recombines with a hole in the valence band, emitting a photon. Since silicon has an indirect band gap (the conduction band minimum and valence band maximum occur at different momenta), a phonon is required to satisfy momentum conservation. The recombination rate is given by

$$R_\mathrm{Rad} = B_\mathrm{Rad} np, \tag{2.7}$$

where B_{Rad} is the radiative recombination coefficient, n is the electron density in the conduction band, and p is the hole density in the valence band [18].

Auger recombination: Auger recombination is a three-particle process in which the energy released by electron-hole recombination is transferred to a third charge carrier, which subsequently thermalizes. The Auger recombination rate is expressed as

$$R_{\text{Aug}} = (C_{\text{n,Aug}} n + C_{\text{p,Aug}} p) np, \tag{2.8}$$

where $C_{\text{n,Aug}}$ and $C_{\text{p,Aug}}$ are the Auger recombination coefficients for electrons and holes, respectively [19]. Due to the quadratic dependence on the injection level, Auger recombination is more prevalent for high doping concentrations, as is visible in Figure 2.2. Radiative and Auger recombination are often referred to as intrinsic recombination, as the properties are inherit to the material itself.

SRH recombination: Shockley-Read-Hall (SRH) recombination occurs via defect states, such as impurities or crystal imperfections, within the band gap [20, 21]. The recombination rate is given by

$$R_{\text{SRH}} = \frac{C_{\text{n,SRH}} C_{\text{p,SRH}} N_{\text{t}} (np - n_{\text{i}}^2)}{C_{\text{n,SRH}} (n + n_1) + C_{\text{p,SRH}} (p + p_1)}, \tag{2.9}$$

where $C_{\text{n,SRH}}$ and $C_{\text{p,SRH}}$ are the defect capture cross-sections, n_{i} is the intrinsic carrier concentration, and n_1 and p_1 are defined as $n_1/p_1 = n_{\text{i}} \exp\left(\frac{\pm E_{\text{t}} - E_{\text{i}}}{k_{\text{B}} T}\right)$, with E_{t} representing the trap energy level [20]. Figure 2.2 shows that at high injection levels SRH recombination diminishes in significance as the traps become saturated.

Surface recombination: As a semiconductor device is not extended infinitely, the lattice is suddenly interrupted at the surface, leading to a lot of so called *dangling bonds*. Surface recombination is similar to SRH recombination but occurs at surface defect states, which are distributed continuously across the band gap [22]. In contrast to recombination rates in the bulk, the surface recombination rate is given in units of density per area. Typically, the recombination current J_{Rec} defines the surface recombination velocity

$$S = \frac{R_{\text{Surf}}}{\Delta n_{\text{Surf}}} = \frac{J_{\text{Rec}}}{q \Delta n}, \tag{2.10}$$

where Δn_{Surf} is the excess carrier density at the surface [22]. Similar to the one-diode model in Equation (2.1), one can define the surface saturation current density [23]

$$J_{\text{Rec,eff}} = q S_{\text{eff}} \Delta n_{\text{Surf,eff}} = J_0 \left(\frac{np}{n_{\text{i}}^2} - 1 \right). \tag{2.11}$$

Unlike SRH recombination, surface recombination usually limits the lifetime in high injection

conditions. Thus, several approaches have been developed to reduce the impact of surface recombination in solar cells, which are described in Section 2.1.3.

Optical Losses

Optical losses originate from suboptimal incoupling of light into the cell. These can stem from simple shading losses due to metal contacts on the front side. Thus, it is beneficial to reduce the metallized area or by optimizing the shape of the metal fingers and busbars [24]. However, there is a trade-off between the fraction of the metallized area and resistive losses, as for a smaller metallized area the resistivity contribution inreases.
Furthermore, the reflectivity of the Si surface itself should be minimized, where two methods are often employed. Firstly, an anti-reflective coating (ARC) layer ensures optimal light incoupling, as according to Fresnel's equation the wavelength-dependent reflection depends on the refractive index of the material above (n_1) and beneath (n_2) the reflective coating. The ideal refractive index $n_{\text{ARC}} = \sqrt{n_1 n_2} \approx 2$ is close to that of SiN_x for a wavelength around 600 nm, depending on the stoichiometry of the layer [25].
Secondly, texturing the surface with pyramidal structures on the μm scale via a chemical process increases light incoupling further. This leads to an enhanced optical path length in the cell, increased likelihood of light trapping, and a larger surface area [26]. Lastly, parasitic absorption in layers other than the primary absorber also contributes to optical losses in a solar cell. These losses can be minimized by selecting an optimal cell design [27].

Resistive Losses

This mechanism is related to resistive losses during transport of charge carriers. Various contributions can be identified, including the conductivity of the base and the lateral transport between the metal fingers [17]. For passivating contacts, also the resistivity contribution from transport through the oxide (Sections 2.2.2 and 5.1) is of importance. Another parameter examined in this work is the contact resistance ρ_{C} between the metal fingers and the emitter, or in the case of poly-Si-based passivating contacts, the poly-Si layer. Furthermore, potential resistive losses can arise from the metal fingers and busbars themselves, which are affected by their cross-sectional area and the material's conductivity.

Given all these loss pathways, a more precise theoretical efficiency limit for crystalline silicon (c-Si) solar cells with one absorber material is 29.4% [28]. Currently, the highest achieved efficiency for c-Si solar cells remains around 27% [5]. To reach these high efficiency values, an enhanced surface passivation is essential, which will be discussed in the next section.

2.1.3. Surface Passivation

Generally, one can distinguish between two main surface passivation mechanisms, which are *chemical passivation* and *field-effect passivation* [29]. Chemical passivation refers to the saturation of dangling bonds at the crystal surface. One way to achieve this is by using materials with a similar crystal structure. For passivating contacts, an interfacial silicon oxide is often used, consisting of just a few atomic layers with a thickness of 1-2 nm. These very thin oxides usually have an unknown stoichiometry and are thus referred to as SiO_x.
On the other hand, field-effect passivation uses the principle that both types of charge carriers need to be present for recombination to occur. By creating an electric field, the position and distribution of charge carriers can be controlled [30]. Ideally, minority carriers are repelled, while majority carriers accumulate at the contact. By changing the polarity of the electric field and increasing its strength, it is also possible to repel majority carriers and attract minority carriers, a phenomenon known as inversion [31, 32]. The electric field for field-effect passivation is usually generated by fixed charges in dielectrics, such as Al_2O_3 for negative charges, or SiN_x and SiO_x for positive charges [29]. A highly doped Si region can also provide field-effect passivation, which can be explained by band bending due to Fermi level alignment, as described in Section 2.1.1. This mechanism enhances the selectivity of charge carriers by facilitating the transport of majority carriers while hindering the flow of minority carriers through favorable band edge alignment. Band bending in (n) poly-Si/SiO_x/(n) c-Si contacts is explored further in Section 2.6.1. The implementation of these surface passivation mechanisms has contributed to significant increases in solar cell efficiency over the last 70 years. To understand the benefit of using passivating contacts, various Si-based solar cell concepts are discussed in the next section, along with their respective advantages and drawbacks.

2.1.4. Historical Development of Cell Concepts

The first practical solar cells, developed in the 1950s, were limited by the progress of semiconductor processing steps and material quality [33, 34]. Moreover, the relatively high cost of silicon was a hindrance for the rapid expansion of the technology. Over time, improvements in these factors led to a reduction in cell costs and an increased production [35]. The culmination of these advancements occurred in the late 1970s with the widespread success of the *aluminum back surface field* (Al-BSF) cell architecture.
As shown in Figure 2.3(a), the Al-BSF cell features a (p) c-Si base with an n-type emitter that is textured on the front side. On top, a SiN_x layer is deposited, followed by screen-printed silver (Ag) fingers. The back side is covered with a full-area Al paste that is fired

to form a contact. During the firing process, Al forms an alloy with Si at the rear surface, resulting in a p-type doped back surface field (BSF) [36].
While this cell design was relatively simple and inexpensive, the formation of an Al-Si alloy layer at the interface increased recombination. In the 1980s, Martin Green introduced the *passivated emitter rear cell* (PERC) concept, improving on the Al-BSF architecture [37]. As shown in Figure 2.3(b), PERC cells evolved to feature an AlO_x/SiN_x stack on the rear side with local laser openings for contact formation. Until recently, the PERC cell was the most widely used industrial concept, but remains limited to $\eta < 24\%$ due to the metal-semiconductor interface on the rear side [4].

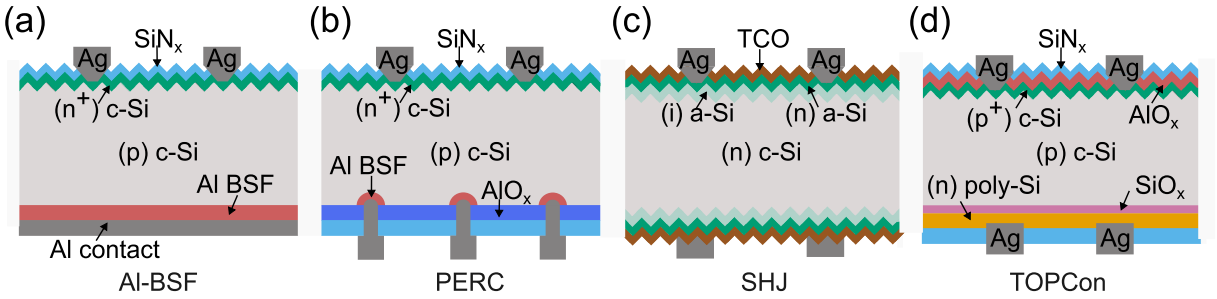

Figure 2.3.: *Illustration of different cell concepts with (a) Al-BSF cell, (b) PERC cell, (c) SHJ cell, and (d) TOPCon cell concepts. Adapted after [38].*

To further increase efficiency, more complex designs like *interdigitated back contact* (IBC) cells have been developed, where the contacts are placed entirely on the rear side, allowing for more light to be absorbed by the active layer on the front side [6, 39]. Another approach involves the use of full-area passivating contacts, which separate metal contacts from the c-Si base [40]. A key feature of these designs is the high charge carrier *selectivity*, defined as the ratio of majority and minority carrier flow to the contacts [7].
Two successful types of selective contacts are widely recognized. The first is the *silicon heterojunction* (SHJ), shown in Figure 2.3(c). In this design, a stack of intrinsic and doped amorphous silicon is deposited on both sides of the cell. This approach has achieved efficiencies close to 27% [5, 41]. However, the SHJ technology faces challenges in industrial processes due to their reliance on expensive transparent conductive oxides (TCO) for metallization and its incompatibility with high-temperature processing.
The second type of selective contact is the *tunnel oxide passivating contact* (TOPCon), illustrated in Figure 2.3(d). Research on TOPCon structures began gaining traction around 2014 [42], but significant groundwork from previous decades laid the foundation for their development [43, 44]. TOPCon cells often feature an (n) c-Si base combined with a p-type emitter, a SiN_x ARC, and Ag metallization. The key feature of the concept is that the rear side of the cell is passivated by a thin tunnel oxide and a doped poly-Si layer, replacing the local Al-BSF used in PERC cells. Ag metal fingers are then typically used to cover

the rear side. This approach allows for excellent surface passivation quality, which can be quantified by the *saturation current density* $J_{0,\text{Pass}}$ (discussed in Section 3.1). For n-type TOPCon cells, $J_{0,\text{Pass}}$ values as low as 1 fA/cm^2 have been reported [45], representing a substantial improvement over PERC cells, where the lowest values typically range around tens of fA/cm^2 [46].

As this work is based on the TOPCon structure, the following sections will provide detailed explanations of the key concepts, along with fabrication techniques for passivating contacts. All samples follow the process flow shown in Figure 2.4, with additional information in the respective sections. The substrate is first prepared by potassium hydroxide (KOH) etching to remove saw damage, followed by wet-chemical cleaning, as described for instance in [47]. Next, the SiO_x is grown, a-Si is deposited, and thermal annealing may be applied. Two main experimental routes are followed: some samples are coated with SiN_x and fired for lifetime and layer characterization, while others undergo metallization via screen-printing or evaporation.

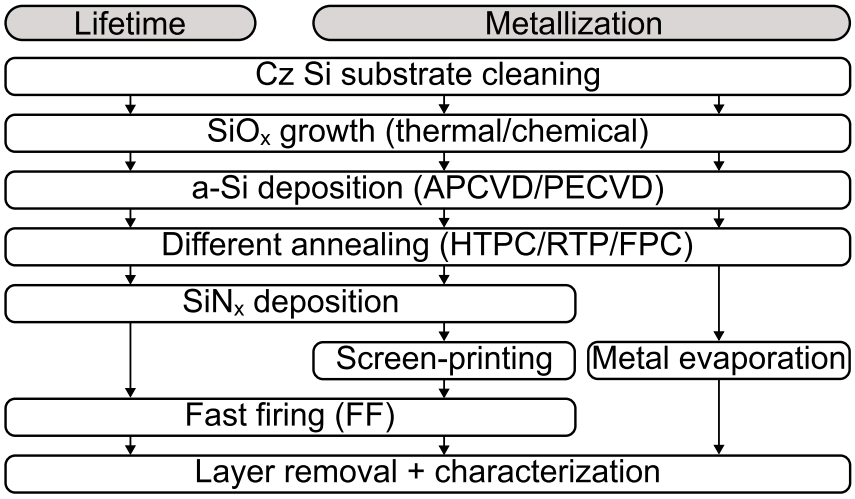

Figure 2.4.: *Process flow for passivating contacts used in this work, where one can differentiate between lifetime samples for layer characterization and metallization samples prepared via screen-printing or metal evaporation.*

2.2. Interfacial Oxide

An essential characteristic of passivating contacts is their ability to provide excellent surface passivation, which is largely due to the interfacial oxide layer. The growth of these oxides is the first fabrication step after substrate preparation (Figure 2.4) and is discussed in detail in Section 2.2.1. Beyond passivation, transport of charge carriers through the oxide is another critical factor to address, which is elaborated upon in Section 2.2.2.

2.2.1. Oxide Growth

Oxide growth can roughly be divided into two main categories. These are *thermal* and *chemical* oxidation, both of which are described below.

Thermal Oxidation

Thermal oxidation for oxide thicknesses $d_{\mathrm{ox}} > 25$ nm is commonly described by the *Deal-Grove model*, which characterizes oxide growth based on three particle fluxes [48]. These are the flux of oxidants from the gas phase to the gas/SiO_x interface, the flux through the already grown oxide, and the reaction at the silicon surface, causing the oxide layer to grow partially into the silicon wafer [49]. In this work, the thermal oxidation process is conducted in a quartz tube furnace. The samples are driven into the furnace at a temperature 50K below the target oxidation temperature and then heated in a mixed N_2/O_2 atmosphere. At the peak temperature, the O_2 flow is increased while N_2 flow is reduced to zero for the duration of the oxidation process. Afterward, the samples are cooled down before being removed from the furnace.
According to the Deal-Grove model, the oxide thickness d_{ox} is dependent on time and temperature and can be described by an *Arrhenius-type relation*

$$d_{\mathrm{ox}} = d_0 \exp\left(-\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T}\right), \tag{2.12}$$

where d_0 is a pre-factor and E_{A} the activation energy for the process [48]. This relationship is demonstrated in Figure 2.5(a), which shows the impact of various oxidation temperatures on oxide thickness in an Arrhenius plot. The oxide thickness was measured on a Float-Zone wafer using spectral ellipsometry, where details can be found in [27]. For high temperatures, the data fits well to the logarithmic behavior described by Equation (2.12), yielding an activation energy of (0.64$\pm$0.12) eV. However, for low temperatures, the Deal-Grove model and simple Arrhenius relation fails to accurately describe oxide growth. Consequently, in Figure 2.5(a), data points at low temperatures were excluded for the determination of E_{A}, due to inaccuracies in the model during the initial phase of oxidation [49, 50]. Literature reports values of E_{A} ranging from 1.5 eV to 4 eV [51–53]. These discrepancies may be attributed to the different growth mechanisms that dominate at various temperature regimes, depending on whether oxidation is primarily diffusion-driven or reaction-driven [52].
Various modifications to the Deal-Grove model have been proposed to correct for deviations, particularly for thin oxides [49, 50, 54]. Most studies focus on dry oxide growth in the temperature range of 800-1000°C, producing oxide thicknesses much greater than 2 nm, which are not suitable for passivating contact applications. No model has been formulated

to accurately describe oxide growth for thicknesses $<$ 2 nm, as the Deal-Grove model typically applies for $d_{ox} >$ 25 nm. However, trends observed for thicker oxides are often assumed to apply to thinner ones as well.

This is further explored in Figure 2.5(b), which shows the effect of oxidation parameters over a temperature range of 525-625°C. It can be seen that a higher temperature still leads to a thicker oxide. To tune the oxide thickness in a range of 1.5-2 nm, the oxidation time is varied as well. While extended oxidation time increases thickness, temperature plays a more significant role than the duration of the process, consistent with Arrhenius-type behavior.

In an attempt to control the oxide thickness even more, for some samples the oxygen flow during heat up was set to zero. This lowered the oxide thickness, but still led to thicknesses above 1.4 nm. Even when no oxygen flow at all was present, a measurable oxide thickness ($>$ 1.3 nm) remained due to the formation of a native oxide when the wafers were driven out of the furnace at temperatures above 475°C in ambient conditions. A similar behavior is also observed during a-Si deposition, as discussed in Section 2.3.1. By fine-tuning the oxygen flow during heat-up and adjusting the temperature, different oxide thicknesses can be achieved. However, several factors influence oxide formation, such as doping type and concentration [55–57], as well as surface morphology [58, 59]. This is particularly relevant when growing oxides on a-Si or poly-Si layers, which tend to have higher oxidation rates and is done in Section 6.2 [60, 61].

In addition to oxide thickness, thermal stability is a crucial factor for application in passivating contacts. Investigations on thin oxides using methods such as transmission electron microscopy (TEM), X-ray photoelectron spectroscopy, and X-ray reflectometry have revealed that stoichiometry can significantly affect the thermal stability of oxides [62–65].

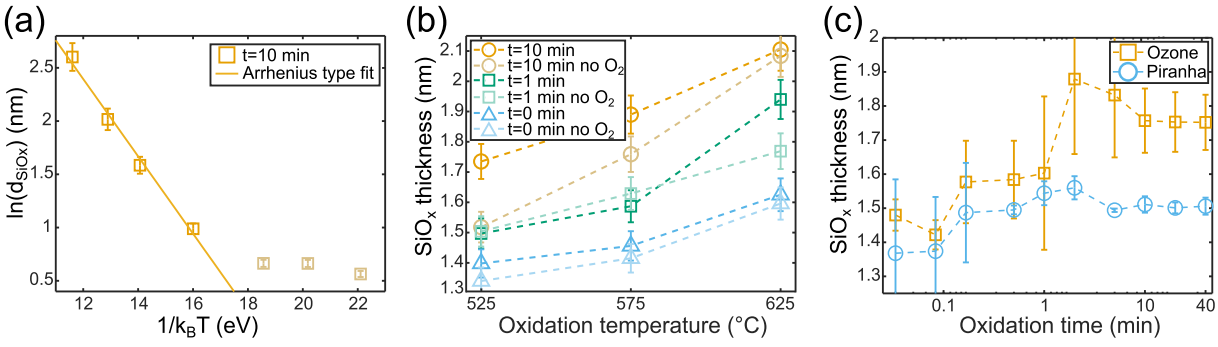

Figure 2.5.: *(a) Logarithmic oxide thickness d_{ox} as a function of inverse temperature, plotted in an Arrhenius plot to determine the activation energy. (b) Oxide thicknesses at different oxidation times with and without oxygen flow during heat-up for low-temperature oxidation. (c) Oxide thickness in ozone and piranha solutions after various oxidation times.*

Wet-Chemical Oxidation

While thermal oxides are particularly beneficial for creating thick layers ($d_{\text{ox}} > 2$ nm), wet-chemical oxides offer greater control over layer properties at low temperatures, simply by adjusting the oxidation time or chemical concentrations, making them ideal for mass production. These processes typically occur between 20-130°C and can result in higher defect densities at the oxide interface [8, 62]. Different methods can be employed for oxide growth, including immersion in hot nitric acid [66–69], UV-assisted ozone oxidation [64, 65], ozonized water oxidation [70, 71], and piranha acid oxidation [71, 72].
The mechanism of oxide growth in H_2O-based solutions depends on the chemical in use. However, this process is often modeled by linear growth kinetics, with reaction species being transported through the oxide. The growth is typically reaction-limited rather than transport-limited due to the small oxide thickness (< 2 nm). The diffusion activity of atomic oxygen is thought to be the primary driving force behind the oxidation process [73, 74]. A key difference between thermal and wet-chemical oxidation is that in wet processes a competing dissolution process occurs, which limits the maximum oxide thickness by reaching a steady-state regime. A review on the dissolution of oxides in aqueous solutions can be found in [75]. The effect of this self-limiting growth is demonstrated in Figure 2.5(c), which shows oxide growth in ozone and piranha solutions for varying oxidation times. Initially, the oxide thickness increases with oxidation time, especially for the ozone-based oxidation. However, dissolution begins to reduce the thickness, leading to a steady-state balance between growth and dissolution, where the oxide thickness stabilizes. This characteristic makes wet-chemical oxides excellent candidates for usage in passivating contacts. It is important to note that very short chemical exposures may reduce homogeneity, as suggested by the error bars in Figure 2.5(c), which show variations in thickness measurements across different points on the Float-Zone wafer. Furthermore, chemical oxides are usually less thermally stable than thermally grown ones, although there are significant differences between various chemical oxidation agents [62]. For instance, it has been reported that ozone-based oxides exhibit better thermal stability than HNO_3 or piranha oxides, which has been attributed to a more favorable stoichiometry [65, 73]. Thermal stability investigations of ozone, piranha, and thermal oxides are conducted in Section 5.1.

2.2.2. Charge Carrier Transport Through the Oxide

The transport of charge carriers through the interfacial oxide plays a significant role in the overall performance of solar cells, particularly for achieving high charge carrier selectivity at the contacts [76, 77]. Two dominant transport mechanisms are observed through the

oxide: direct *tunneling* and transport via *pinholes*, both illustrated in Figure 2.6(a). These mechanisms can be distinguished using temperature-dependent transfer-length method (T-TLM) measurements, as described in Section 3.3.3, where the contact resistivity (ρ_C) is determined [76, 78, 79]. This refers to the area-normalized resistance associated with the whole metal/poly-Si/SiO_x/c-Si contact, whereas the resistance due to the transport through the metal/poly-Si interface usually is negligible [78].

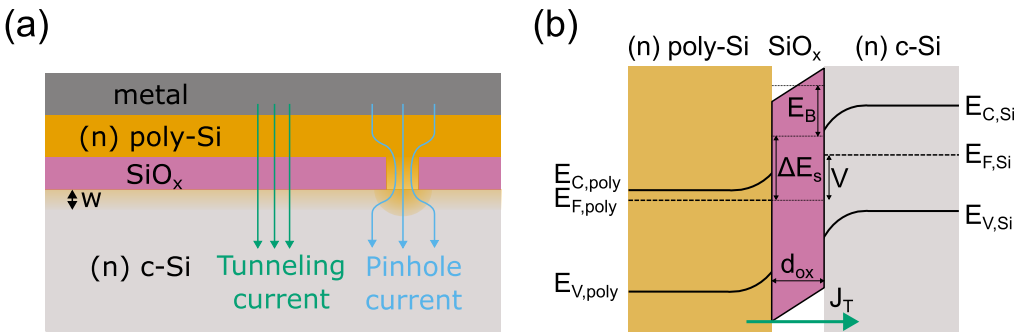

Figure 2.6.: *(a) Charge carrier transport mechanisms, namely tunneling and pinhole formation, through a (n) poly-Si/SiO_x/(n) c-Si stack. (b) Band diagram for tunneling transport through the interfacial oxide. Adapted from [78, 79].*

Tunneling Transport

To derive the tunneling contribution to ρ_C, one can consider the current-voltage characteristics of a semiconductor-insulator-metal (MIS) structure, which were extensively studied in the 1970s [43, 80, 81]. In the following, we will treat a (n) poly-Si/(n) c-Si high-low junction. For a (p) poly-Si/(p) c-Si junction the considerations are analogue. It has been shown by Feldmann et al. that the poly-Si can be treated similar to a metal due to the high doping, which leads to the Fermi level approaching the conduction band edge [82]. Thus, the already established MIS theory can be used to describe a tunneling junction [81]. One can differentiate between direct band to band tunneling and trap assisted transport for minority and majority carriers, respectively. For high-low junctions, minority carrier transport can be disregarded due to the small minority charge carrier densities for measurements in the dark and under small bias voltages [83]. In this description, transport via traps will also be ignored, following Folchert et al. [79]. The direct tunneling current into the wafer is [11, 81, 84]

$$J_T(V) = AT^2 P_T \exp\left(-\frac{\Delta E_s}{k_B T}\right)\left(\exp\left(\frac{qV}{nk_B T}\right) - 1\right), \tag{2.13}$$

where $A = 4\pi q m_{eff} k_B^2/h^3$ is the effective Richardson constant and

$$P_T = \exp\left(-d_{ox}\sqrt{\frac{8m_T E_B}{\hbar^2}}\right) \tag{2.14}$$

is the tunneling probability with the tunneling mass m_T and ideality factor n, which refers to the change in surface potential at the poly-Si/SiO_x/c-Si interface. In Figure 2.6(b), parameters like the tunneling barrier height E_B, the oxide thickness d_ox, and the offset between conduction band and Fermi level at the SiO_x/c-Si interface ΔE_s are shown. One can calculate the tunneling contribution to contact resistance for $V = 0$ via [79]

$$\rho_{\mathsf{C,T}} = \left(\frac{\mathrm{d}J_\mathsf{T}}{\mathrm{d}V}\right)^{-1}_{V=0} = \frac{nk_\mathsf{B}}{qATP_\mathsf{T}} \exp\left(\frac{\Delta E_\mathsf{s}}{k_\mathsf{B}T}\right). \tag{2.15}$$

Pinhole Formation and Transport

In this section, the contribution to the contact resistivity for pinhole transport through the oxide is discussed. Pinholes are small disruptions in the oxide, typically formed during thermal annealing [77, 85, 86]. A widely accepted model for the evolution kinetics of pinholes, proposed by Ajuria and Reif [87], will be briefly outlined here. Similar to the crystallization of a-Si (see Section 2.3.3), void *nucleation centers* are hypothesized during oxide growth, which grow further under favorable conditions. The authors propose that pinhole formation is driven by agglomeration of the oxide, as a reduction in surface area leads to a more energetically favorable state, causing the thin film to "ball up". By comparing the surface energy of pinholes with radius r to a thin oxide layer, they found that when $r > 1.5d_\mathsf{ox}$, it is energetically favorable for the film to ball up. A prerequisite for oxide growth is the presence of perturbations. In the case of poly-Si (Section 2.3), grain boundaries are a good candidate for perturbations, especially at vertices, where multiple grain boundaries intersect [88].
The growth of nucleated voids can be kinetically described by considering diffusion of dopants, oxygen, silicon atoms, or vacancies through the SiO_x/c-Si junction. To calculate a rate equation for pinhole formation, several factors must be considered: Fick's law for diffusion in one dimension, the chemical potential of the curved void surface, the material transfer rate at the SiO_x/c-Si interface (correlating to surface diffusion), and volume conservation. This yields the expression for the pinhole growth rate

$$\frac{\mathrm{d}r}{\mathrm{d}t} = \frac{16D_\mathrm{Surf}\Omega^2 n_\mathrm{Surf}\gamma}{\pi k_\mathrm{B}Td_\mathrm{ox}^3} = \frac{\beta}{d_\mathrm{ox}^3}\exp\left(\frac{E_\mathrm{a}}{k_\mathrm{B}T(t)}\right), \tag{2.16}$$

where $D_\mathrm{Surf} = D_0 \exp\left(\frac{E_\mathrm{A}}{k_\mathrm{B}T(t)}\right)$ is the surface diffusivity, and β includes constants such as atomic volume Ω, surface concentration n_Surf, and interfacial energy γ. In the case of a time-independent temperature, Equation (2.16) shows a linear dependence on time, an Arrhenius-type dependence on temperature, and an inverse dependence on oxide thickness. For real processes, involving a time-dependent temperature profile $T(t)$ during annealing, numerical methods can be used to solve for the growth kinetics (see Section 5.1.2).

To describe the contact resistivity for pinhole-dominated transport, one can employ the semi-classical drift-diffusion model initially applied by Cox and Strack [89, 90]. They derived the expression

$$R_{\mathrm{Spread}}(T) = \frac{\rho_{\mathrm{B}}(N_{\mathrm{Diff}}, T)}{2\pi r_{\mathrm{p}}} \arctan\left(\frac{2w}{r_{\mathrm{p}}}\right) \tag{2.17}$$

for the spreading resistance between a circular contact and a silicon base. In the context of a TOPCon structure, r_{p} refers to the pinhole radius, w represents the width of the in-diffused region under the pinhole (see Figure 2.6(a)), and $\rho_{\mathrm{B}}(N_{\mathrm{Diff}}, T)$ is the temperature- and doping-dependent resistivity of the region underneath the pinhole with a doping concentration N_{Diff}. The arcus tangens arises from an empirical fit to experimental data. Over the years, this model has been modified for various geometries [91, 92], but its validity has been confirmed by multiple experimental studies [76, 78, 79]. For multiple pinholes with a pinhole density N_{P}, the contact resistivity

$$\rho_{\mathrm{C,P}} = \frac{R_{\mathrm{Spread}}(T)}{N_{\mathrm{P}}} \tag{2.18}$$

can be determined. Given the distinct temperature dependence of tunneling and pinhole transport, temperature-dependent TLM measurements can be used to identify the dominant transport mechanism through the oxide, as discussed in Section 3.3.3.

In recent years, several studies have focused on the dominant transport mechanisms in well-crystallized poly-Si/SiO_x contacts. The consensus is that for thin oxides ($d_{\mathrm{ox}} < 2$ nm), tunneling is the primary transport mechanism [76, 77, 93]. However, for thicker oxides, the tunneling probability decreases exponentially, and pinhole transport typically dominates. It is crucial to optimize annealing conditions for the specific oxide type and thickness to ensure the appropriate pinhole density without compromising passivation quality. Additionally, the oxide resistivity directly impacts the overall junction resistivity in TOPCon cells and should be minimized for optimal performance [17, 94].

2.3. Polycrystalline Silicon

Another important factor contributing to the excellent surface passivation of passivating contacts is the doped poly-Si layer, which provides field effect passivation and high charge carrier selectivity. Since poly-Si is a critical component of passivating contacts, different deposition techniques are discussed in Section 2.3.1. In addition, the properties of a-Si and poly-Si are introduced in Sections 2.3.2 and 2.3.3, respectively. Charge carrier transport through the poly-Si is then detailed in Section 2.3.4.

2.3.1. Deposition Techniques

Poly-Si is typically not deposited directly onto the SiO_x layer, as this can result in inferior properties such as smaller grain size and lower conductivity [95–97]. Therefore, a-Si is deposited with a typical thickness $<$ 300 nm and a doping concentration in the order of 10^{20} cm^{-3}, followed by a high-temperature annealing step to crystallize the a-Si. *Chemical vapor deposition* (CVD) and *physical vapor deposition* (PVD) are the most common way to deposit a-Si, which both are single-sided deposition processes.
For PVD, magnetron sputtering deposition is sometimes employed, though it is not widely used in industry due to its low throughput and sputter damage during deposition [98, 99]. CVD techniques such as low pressure CVD (LPCVD), hot wire CVD (HWCVD), plasma enhanced CVD (PECVD), and atmospheric pressure CVD (APCVD) are also viable options. Currently, PECVD is the preferred deposition method in industry due to its compatibility with existing processes, particularly for SiN_x deposition [100]. APCVD is less common for a-Si deposition, though it offers a lower cost of ownership compared to other CVD technologies [101].

PECVD

PECVD operates in a vacuum at temperatures between 200-400°C, employing a radio frequency (RF) plasma to dissociate precursor gases, leading to layer deposition. In this work, a lab tool for multiple wafer sizes from centrotherm international AG was used for deposition. The plasma is in direct contact with the samples, which act as electrodes. To deposit a-Si, the precursor gas SiH_4 is used, while B_2H_6 or PH_3 is added for (p) or (n) doping, respectively. The use of hydrogen-containing gases results in significant hydrogen incorporation into the a-Si layer, which can boost passivation, but also increase its susceptibility to blister formation [8, 102].

APCVD

In contrast to PECVD, APCVD does not require a vacuum, allowing it to be used as an in-line tool. In this work, an APCVD tool from Schmid Thermal Systems was used. A schematic representation of an APCVD system is shown in Figure 2.7. Samples are placed on a conveyor belt and transported through the machine, with deposition occurring at temperatures around 700°C. The injector head supplies SiH_4 and N_2 through separate channels, which flow laterally across the sample surface and are then extracted through the exhaust [9]. Doping is achieved by introducing PH_3 (n-type) or B_2PH_6 (p-type) into the gas

flow. The thermal dissociation of SiH_4 takes place immediately on the wafer surface, utilizing the very directed gas flows. Nitrogen gas curtains enable a low oxygen concentration and prevent the escape of reactive species from the deposition zone.

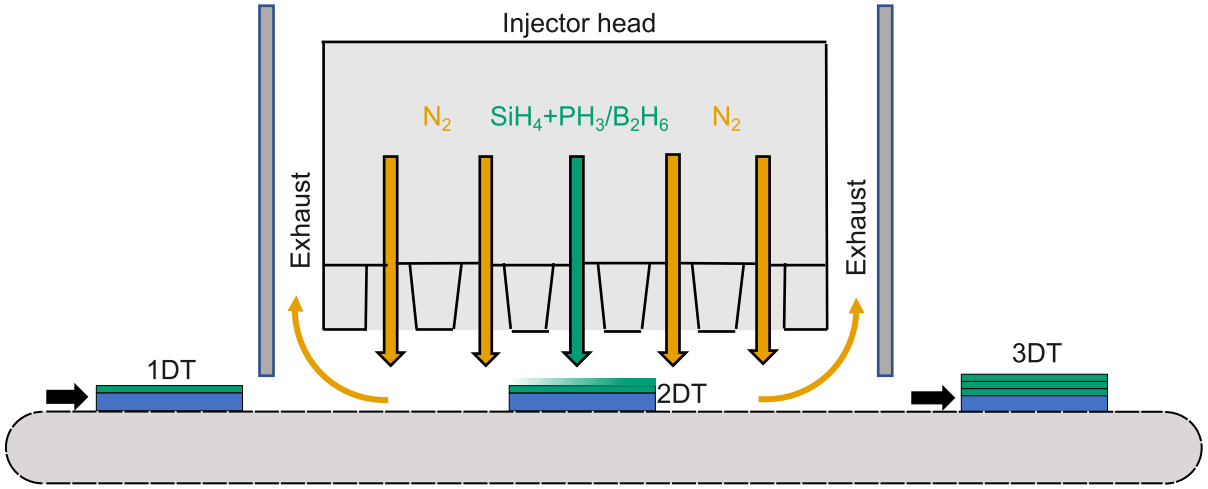

Figure 2.7.: *Schematic of an APCVD machine. The sample is placed on a conveyor belt, while deposition occurs under the injector head. Multiple drive-throughs (DT) can be used to achieve varying layer thicknesses. Adapted from [9].*

In this thesis, different a-Si thicknesses are used, which can be realized by two different methods. Firstly, changing the *belt speed* leads to a varying exposure time beneath the injector. In this way a maximum layer thickness of 330 nm was achieved. Secondly, the *multi-layer approach* can be used, where the deposition process is repeated multiple times by several drive-throughs (DT) until the desired layer thickness is achieved [17, 103, 104]. Importantly, during subsequent cool-down after the individual deposition processes in an oxygen containing atmosphere, a silicon oxide layer is grown on top of the a-Si layer [17]. Thus, each individual layer is separated by a thin interlayer oxide $SiO_{x,Inter}$, which is an important characteristic of APCVD layers.

APCVD a-Si has unique properties due to the high deposition temperature of around 700°C. In contrast to PECVD, very little hydrogen is incorporated into the a-Si. Additionally, the layer may already be partially crystallized during deposition, which is particularly intriguing for the FPC concept with its limited thermal budget.

However, APCVD machines may exhibit limitations, such as layer inhomogeneities and wrap-around during deposition onto the wafer backside if the system is not optimized for the specific layers. These issues can lead to significant variations in layer thickness and doping concentration, particularly near the wafer edges, where temperature gradients can occur [105]. Additionally, a-Si dust can in some cases accumulate on the edge of the wafer's backside, potentially complicating subsequent processing steps.

2.3.2. a-Si Properties

This section provides an overview of a-Si properties, with detailed descriptions available in [61] and [106]. A significant difference between c-Si and a-Si is the lack of long-range order in a-Si, which removes the distinction between direct and indirect band gap. To characterize the short-range order in a-Si, the coordination number Z can be defined as the number of bonds of each atom to an immediate neighbor. A defect then is an atom that has more or less bonds than its coordination number. Through the higher number of defects in the a-Si, additional states in the band gap are introduced. Thus, for a-Si a mobility band gap can be defined ($\approx$ 1.85 eV), referring to the energy difference between the delocalized states that contribute to conduction and the localized states near the band edges, which act as traps. These localized states result from disorder in the structure and can extend into the band gap (band tail states). Charge carriers can become trapped in these localized states, requiring additional energy (often thermal) to hop between these localized states, and is thus called *hopping conduction*. In contrast to c-Si, where carriers move freely, hopping conduction requires thermal energy and is thus less efficient, leading to higher a-Si resistivity. The conductivity of a-Si can be modified by doping, although it is less efficient than in c-Si [27, 107]. This inefficiency arises because the lack of periodicity in the a-Si lattice limits *substitutiona*l doping, where dopants replace silicon atoms in lattice sites. In a-Si, dopants mostly occupy *interstitial* positions between silicon atoms, which increases the solubility limit compared to c-Si. This factor must be considered during the annealing process.
The annealing of a-Si has several effects, including *dopant activation*, *crystallization*, and *dopant in-diffusion*. Dopant activation is the process by which dopants become electrically active, donating or accepting charge carriers to enable conduction. During annealing, dopants typically move from unfavorable interstitial sites to substitutional lattice sites. Doping in a-Si is less effective than in c-Si due to reduced dopant diffusion, an increased number of traps, defects, and dangling bonds [108]. Consequently, a-Si is usually crystallized into poly-Si through thermal annealing, which will be discussed in the next section.

2.3.3. Poly-Si Properties

Poly-Si is characterized by many regions of uniform crystal orientation, known as grains or crystallites [109]. These grains are not necessarily oriented in the same direction, resulting in disruptions of the crystal, which are referred to as grain boundaries. Doping in poly-Si is primarily substitutional, as within individual grains the lattice is ordered periodically, similarly to c-Si. Thus, crystallization of a-Si to poly-Si is a crucial process for dopant activation, and these terms are often used interchangeably.

Annealing temperatures are generally kept below 1000°C, which is under the melting point of silicon. Under these conditions *solid-phase crystallization* (SPC) occurs, which is typically described by the Kolmogorov-Johnson-Mehl-Avrami (KJMA) model [110, 111]. This model assumes that nucleation centers form and grow at a certain rate until the grains meet or are otherwise constrained. The growth is time-dependent and driven by an activation energy, which is typically supplied through thermal annealing. Depending on the thermal budget of the annealing step, amorphous phases may still exist within the poly-Si. Thus, many properties of poly-Si arise from a combination of c-Si and a-Si.
Important factors influencing crystallization include temperature, doping, and stress. A higher temperature typically leads to a larger nucleation rate. Similarly, doping typically produces larger grains due to a smaller nucleation rate [112, 113]. However, most findings in literature refer only to long crystallization processes, where the sample is in thermal equilibrium. During short annealing processes, there is not enough time for the grain growth to limit itself by other grains, so the growth behavior might differ.
The terms a-Si and poly-Si are often used interchangeably. In this work, "as-deposited" refers to a-Si in its state immediately after deposition, before any thermal annealing.

2.3.4. Charge Carrier Transport Through the Poly-Si

The macroscopic properties of poly-Si, particularly its electrical conductivity, are strongly influenced by the characteristics of the individual crystallites and grain boundaries [114–117]. Two models are widely used to describe charge carrier transport in poly-Si: the *dopant segregation model* [118, 119] and the *charge carrier trapping model* [115].
In the dopant segregation model, grain boundaries act as sinks for impurity atoms, which become electrically inactive and result in inefficient doping. However, this model has several limitations, as it is difficult to verify experimentally and cannot explain all observed behaviors [120].
The charge carrier trapping model, first proposed by Seto in 1975, suggests that the high defect density in poly-Si leads to the formation of trapping states. When charge carriers are trapped at grain boundaries with a surface density of Q_t at an energy E_t, the number of free carriers is reduced. As shown in Figure 2.8(a) for (p) poly-Si, this trapping leads to electrical charging of the traps and creates a depletion width W around the grain boundary, due to the creation of an electric field repelling charge carriers and consequently creating a potential barrier. Furthermore, this reduces the mobility, which can be measured experimentally, as discussed in Section 3.3.2. To find an expression for the *mobility* μ in poly-Si, Seto's derivation assumes a uniform grain size L and total ionization of dopants, which are uniformly distributed with concentration N_D. The grain boundary thickness is assumed to

be negligible compared to the grain size. Using these assumptions, the band diagram for (p) poly-Si in Figure 2.8(b) can be determined.

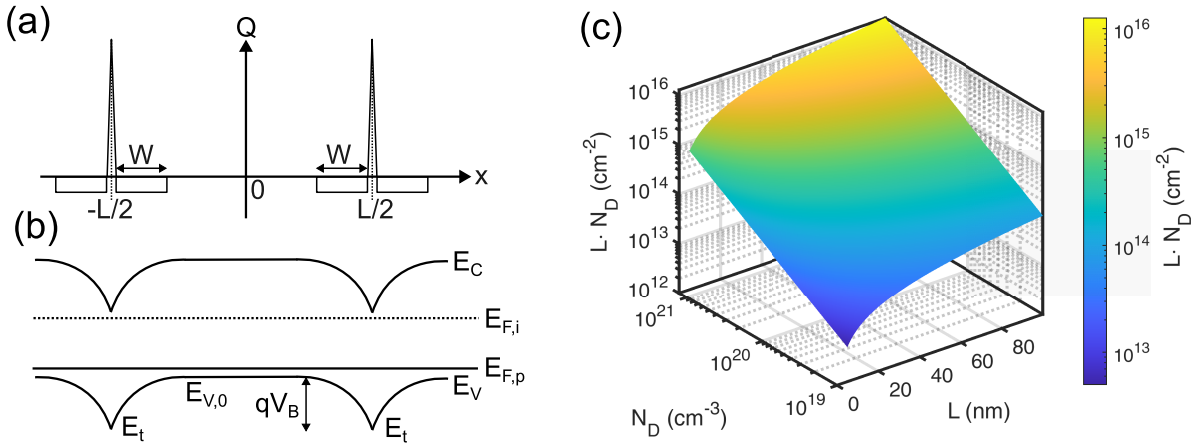

Figure 2.8.: *(a) Charge distribution for a (p) poly-Si crystallite with grain boundaries. (b) Band diagram for trapping states with energy E_t at grain boundaries, leading to a potential energy barrier V_B in the valence band. Figures adapted after [115]. (c) Product of crystallite size L and doping concentration N_D to evaluate the depletion regime.*

One can see that the trapping at the grain boundaries leads to a potential energy barrier V_B, hindering the transport from one grain to another. Different geometries have been considered, such as cylindrical or spherical grains [116, 121]. However, for the sake of transport properties, it is often sufficient to treat the problem in one dimension. This begins with Poisson's equation

$$\frac{\mathrm{d}^2V}{\mathrm{d}x^2} = \frac{\sigma}{\varepsilon} = \frac{qN_\mathrm{D}}{\varepsilon}, \tag{2.19}$$

where ε is the dielectric permittivity of poly-Si and σ is its charge carrier density. By solving Equation (2.19) with appropriate boundary conditions, the potential becomes

$$V(x) = \frac{qN_\mathrm{D}}{2\varepsilon}(x - L/2 + W)^2 + E_{\mathrm{V,0}}, \quad L/2 - d < x < L/2, \tag{2.20}$$

where $E_{\mathrm{V,0}}$ is the potential at the valence band edge. Two cases can be considered: (I) when $LN_\mathrm{D} < Q_\mathrm{t}$, the grain is completely depleted while the traps are not fully occupied, and (II) when $LN_\mathrm{D} > Q_\mathrm{t}$, only part of the crystallite is depleted of carriers. To understand which case applies for poly-Si layers used in this work, Figure 2.8(c) shows the product LN_D for different values of $L \in$ [1,100] nm and $N_\mathrm{D} \in$ [10^{19},10^{21}] cm^{-3} in a 3D plot. For passivating contacts, one typically finds $N_\mathrm{D} > 10^{20}$ cm^{-3} and $L >$ 10 nm. In this range, LN_D is at least 10^{14} cm^{-2}. For an estimation of Q_t, the empirical relation

$$Q_\mathrm{t} = (35 + 2.55L^{-0.363}) \cdot 10^{10} \tag{2.21}$$

can be used [122]. When $L \in$ [1,100] nm, Q_t ranges from (1-5) $\cdot$ 10^{13} cm^{-2} and decreases with larger crystallite size. Therefore, case (II) $LN_\mathrm{D} > Q_\mathrm{t}$ is sufficient for further calculations. By applying boundary conditions, when using Equation (2.20), one finds the expression

$$V_\mathrm{B} = V(L/2) - V(0) = \frac{qQ_\mathrm{t}^2}{8\varepsilon N_\mathrm{D}}. \tag{2.22}$$

It is evident from Equation (2.22) that higher doping concentrations and lower trap densities result in a lower barrier height. By employing Boltzmann statistics and assuming that the barrier height is comparable to or larger than $k_\mathrm{B}T$, the thermionic emission current density for an applied voltage across a grain boundary can be calculated. This thermionic emission refers to the process by which charge carriers gain sufficient thermal energy to overcome the potential barrier at the grain boundary. With the average charge carrier density n_avg, the grain boundary resistivity ρ_μ, and by using

$$\mu = \frac{1}{qn_\mathrm{avg}\rho_\mu}, \tag{2.23}$$

the mobility μ can be expressed as

$$\mu = Lq\sqrt{\frac{1}{2\pi m_\mathrm{eff}k_\mathrm{B}T}}\exp\left(-\frac{qV_\mathrm{B}}{k_\mathrm{B}T}\right), \tag{2.24}$$

where m_eff is the effective mass of the respective carrier type [115]. Equation (2.24) can be used to experimentally determine V_B, as described in Section 3.3.2.
However, for highly doped poly-Si, several additional factors should be considered [117]. Firstly, the effect of the depletion width on the transport properties may not be negligible. Various propositions have been made to incorporate the depletion region's effect. Colinge et al. considered a series combination of resistances that produced promising results [116]. However, this deviation is generally tiny when V_B is also small. Other approaches treat the grain as a sphere and calculate the critical radius $L_\mathrm{c} = \frac{3Q_\mathrm{t}}{N_\mathrm{D}}$ at which the grain is fully depleted of carriers [121]. According to [117], the depletion width W can also be defined using the implicit equation

$$W = \frac{Q_\mathrm{t}}{2N_\mathrm{D}\left(1 + \frac{2n_\mathrm{i}}{N_\mathrm{D}}\exp\left(-\frac{E_\mathrm{t}}{k_\mathrm{B}T}\right)\exp\left(\frac{q^2N_\mathrm{D}W^2}{2\varepsilon k_\mathrm{B}T}\right)\right)}, \tag{2.25}$$

where n_i is the intrinsic carrier density. This allows for the general definition of $V_\mathrm{B} = \frac{qW^2N_\mathrm{D}}{2\varepsilon}$. In the case of $W = L/2$, this represents the scenario where the grain is entirely depleted. Equation (2.22) is also recovered when the denominator of Equation (2.25) equals $2N_\mathrm{D}$. For high doping, this is typically the case, as $n_\mathrm{i}/N_\mathrm{D}$ is sufficiently small, resulting in a negligible

depletion width.
Secondly, for practical applications, the effect of layer thickness may also need to be considered, as thicker layers can increase mobility if transport is not confined to two dimensions. One extension suggests modifying the mobility via

$$\mu_{\text{layer}} = 0.75 \cdot \mu \frac{d}{l_{\text{c}}} \left(0.423 + \ln\left(\frac{l_{\text{c}}}{d}\right)\right), \tag{2.26}$$

where l_{c} is the mean free path length of the majority carriers, and d is the layer thickness [123].
Lastly, the resistivity of the crystallites themselves ρ_{Si} may not be negligible compared to the resistivity of the grains ρ_{μ}. Therefore, it has been suggested to modify the total resistivity ρ_{Total} via [117]

$$\rho_{\text{Total}} = \rho_{\text{Si}} \left(1 - \frac{2W}{L}\right) + \rho_{\mu}. \tag{2.27}$$

A discussion of these factors and their modification for highly doped (p) poly-Si layers is provided in Section 5.2.

2.4. Annealing

As already mentioned, annealing of a-Si is a critical processing step for the properties of passivating contacts and carried out after a-Si deposition (Figure 2.4). To ensure the desired contact properties, a cleaning step with ozone and piranha oxide is applied after the a-Si deposition, followed by various annealing steps to modify the *thermal budget* (TB) of the process. The term "thermal budget" is commonly used to quantify the total thermal energy supplied during a process. In literature, many models attempt to define TB [124–126]. Often, the area under the time-temperature curve of the annealing process is used to represent TB [126, 127]. Accordingly, the TB can be altered by changing either the temperature or the annealing duration.
However, for many processes, such as diffusion, crystallization, or pinhole formation, time and temperature may contribute differently due to the underlying Arrhenius dependence of the kinetic rates. For example, different combinations of temperature and time yielding the same area under the time-temperature curve have been shown to result in entirely different diffusion behavior [124]. Instead of merely integrating the temperature profile, definitions such as $\mathrm{TB} = A \exp\left(\frac{E_{\text{a}}}{k_{\text{B}}T}\right) t$ have been proposed [126]. In this expression, temperature contributes more heavily than time due to the exponential factor. However, this method requires knowledge of the activation energy E_{a} of the specific process as well as an additional constant A, which correlates to the initial state of the system. Some studies suggest that

only the temperature exceeding a certain reference value T_{ref} needs to be considered [128]. Hence, TB can be controlled by parameters such as the duration above T_{ref}, the peak temperature, and the ramp-up/cool-down rates [128]. Based on this, the definition

$$\mathrm{TB} = \int_{T_{\text{ref}}}^{T_{\text{max}}} T \, \mathrm{d}t \tag{2.28}$$

of the thermal budget is proposed. This equation represents a compromise between accurate TB determination and practical considerations. The reference temperature T_{ref} must be chosen based on physical principles but remains somewhat arbitrary.
In the context of this work, only annealing at temperatures above 700°C is applied. Key processes such as crystallization, pinhole formation, and dopant diffusion are known to occur significantly at temperatures in this temperature regime [68, 78, 129]. Consequently, T_{ref} is set to 700°C. A slight drawback of this approach arises when the difference between T_{max} and T_{ref} is large, which may lead to an underestimation of the contribution of high temperatures near T_{max}, where one would expect an Arrhenius-type temperature dependence.

One can roughly distinguish between four annealing cases for passivating contacts. Firstly, high-temperature annealing with a slow ramp-up over an extended period in a quartz tube furnace, leading to the standard high temperature passivating contact (HTPC), described in Section 2.4.1. Secondly, shorter annealing times with fast ramp-up rates in a rapid thermal processing (RTP) furnace, elaborated in Section 2.4.2. Thirdly, no annealing before further processing. In this scenario, samples are coated with a SiN_x layer via PECVD for passivation and are subsequently fired in a belt furnace, discussed in Section 2.4.3. The fourth case entails laser annealing. In the context of this work, both a bachelor's thesis and a master's thesis explored laser annealing for APCVD a-Si [130, 131]. This method was found to reduce the sheet resistivity of a-Si. However, maintaining high passivation levels proved challenging due to negative impacts on the interfacial oxide. Further research is required to integrate laser crystallization into APCVD-based passivating contacts, which will not be discussed further in this thesis.

2.4.1. High Temperature Anneal

Tube furnace annealing is commonly employed to produce passivating contacts and can serve as a reference for shorter annealing processes. Since various oxides are used in this work, the annealing conditions must be adjusted to accommodate the thermal stability of each oxide. To this end, three different temperature profiles are applied. Each profile maintains the same total annealing duration of 75 min to ensure comparable thermal budgets, with the primary difference being the peak temperature and the corresponding time spent

at that peak temperature. The annealing profiles include 820°C for 68 minutes, 870°C for 49 minutes, and 920°C for 30 minutes. All crystallization steps occur in an N_2 atmosphere, with a ramp-up rate of 8 K/min and a cool-down rate of 4 K/min.

2.4.2. Rapid Thermal Processing

For shorter annealing durations, a *rapid thermal processing* (RTP) furnace by Xerion Berlin Laboratories GmbH is used. The furnace can achieve ramp-up rates of up to 100°C/s, reaching a maximum temperature of 1000°C, with cool-down rates capped at 5°C/s. The wafer temperature is measured using a thermocouple, which feeds into a control loop with temperature-dependent PID (proportional, integral, derivative) parameters [132, 133]. Proper tuning of these PID parameters is critical to prevent temperature overshoot or oscillations around the set temperature. Additionally, the annealing process is sensitive to differences in wafer thickness and size, as these factors influence the thermal mass and consequently the temperature response of the wafer. For the temperature profiles shown in Figure 2.9, all RTP processes were carried out with 5 slm N_2 at ambient pressure.

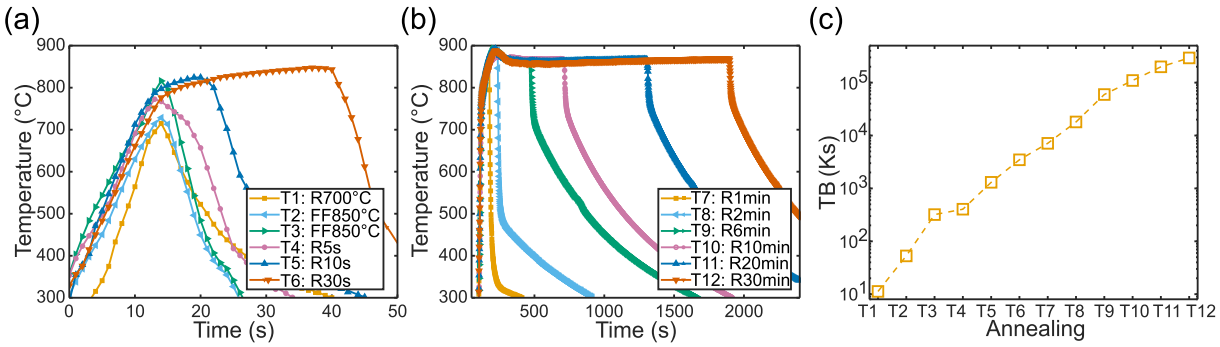

Figure 2.9.: *Different measured annealing profiles used throughout this work with increasing thermal budgets. (a) Short processes used for charge carrier transport determination in Section 5.1. (b) RTP profiles with increasing set time at peak temperature. (c) Thermal budgets for the individual annealing steps, calculated according to Equation* (2.28).

Figure 2.9(a) and (b) illustrate the RTP profiles resulting from a quick ramp-up, with the peak temperature set to 870°C. To achieve different thermal budgets, the duration at the peak temperature is varied between 5 s and 30 min and are referred to as R5s and R30min. For shorter annealing times of 5 to 10 seconds, the peak temperature is slightly lower than for longer processes, due to the high thermal mass preventing rapid heating. Moreover, for the profiles shown in Figure 2.9(b), there is a slight overshoot in temperature during the initial ramp-up. However, this deviation remains under 30°C and is unlikely to significantly impact the crystallization process.

2.4.3. Fast Firing

Even shorter annealing, such as T2 and T3 in Figure 2.9(a), can be realized through *fast firing*. This step is typically used to enhance chemical passivation via hydrogenation [8, 134]. To do so, samples are coated with a SiN_x layer, which is deposited using PECVD by adding NH_3 to the gas flow. Samples are subsequently fired, allowing hydrogen to diffuse to the poly-Si/SiO_x interface, where it saturates dangling bonds, improving the passivation quality. The here used firing furnace from centrotherm international AG consists of a belt that moves the wafers through six temperature zones, each with independently adjustable temperatures. Heating is achieved through infrared lamps. Consequently, the actual wafer temperature differs from the set one, which depends strongly on heat in-coupling, where several factors contribute.

Firstly, the thermal mass of the wafer reduces the reached temperature, as the firing process is not long enough to reach thermal equilibrium. Most importantly, the absorption of infrared radiation dictates heating of the wafers. In the context of this work, factors such as a-Si thickness, base thickness, and doping levels influence this absorption. To check the influence of sample configuration on the heating, the actual temperature of the wafer can be measured via a thermocouple attached to the wafer's surface.

This relationship is illustrated in Figure 2.10, where the measured peak firing temperature (MPFT) is compared to the set peak firing temperature (SPFT) for different sample types, with the remaining firing profile held constant. In Figure 2.10(a), various thicknesses of (p) a-Si on (n) Cz wafers are shown, along with the corresponding firing profile displayed in the inset. Notably, this firing profile was applied to all samples with dimensions smaller than 15.6x15.6 cm^2, specifically 5x5 cm^2 samples. These smaller wafers were placed on a 15.6x15.6 cm^2 dummy wafer to prevent metal contamination from the belt and to ensure uniform temperature distribution. On the other hand, 15.6x15.6 cm^2 samples were placed directly on the belt (with the only contact being at the sample's edges) and fired with the temperatures and firing profile displayed in Figure 2.10(b).

As expected, the measured temperature is consistently lower than the set temperature, with this difference slightly increasing at higher firing temperatures. A thicker a-Si layer results in a higher measured firing temperature, which can be attributed to increased absorption in the a-Si due to enhanced scattering at grain boundaries and defects [17, 27, 135]. In contrast, crystalline silicon absorbs significantly less in the infrared spectrum [12], leading to reduced heating, as shown in Figure 2.10(b). The base doping type also influences the measured firing temperature. A phosphorus-doped base, with a doping concentration of 5 Ωcm, shows less heating compared to boron-doped (1.7 Ωcm) and gallium-doped (1.1 Ωcm) Cz wafers. This is partially due to the lower thickness of P doped wafers ($\approx$ 125 μm) compared to

B or Ga doped bases ($\approx$ 150 µm). However, higher doping concentrations can also lead to increased scattering and absorption, thereby raising the measured firing temperatures. Additionally, the influence of surface morphology is apparent when comparing textured and planar surfaces for the phosphorus-doped wafers. Due to the enhanced light incoupling at the pyramids of textured surfaces (Section 2.1.2), heat absorption is greater, resulting in higher measured temperatures.

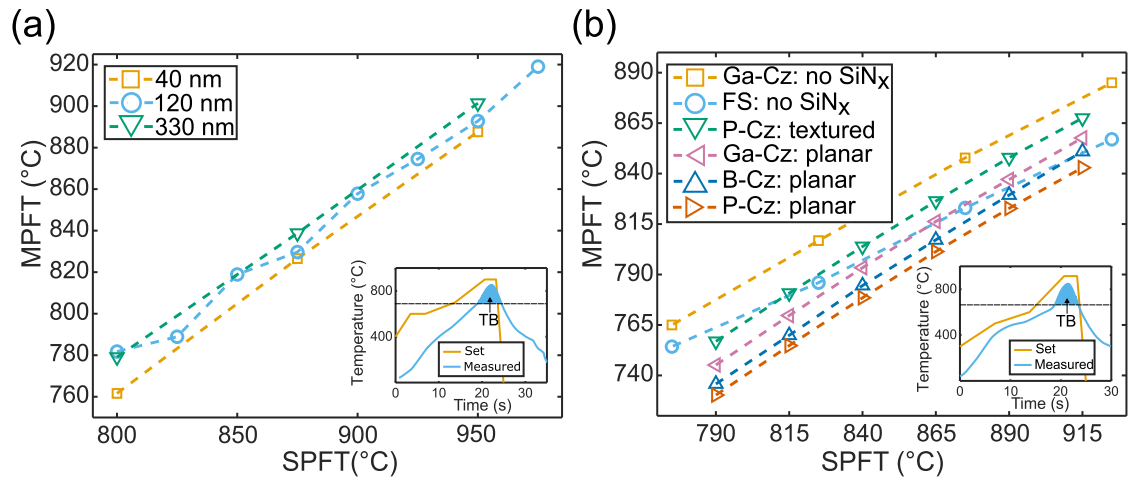

Figure 2.10.: *Relation between set and measured peak firing temperature for (p) a-Si layers with (a) different thicknesses and (b) different base substrates. The inset shows the set and measured firing profiles with the corresponding definition of the thermal budget* TB*.*

In some cases, samples are fired without a SiN_x layer, which typically leads to a higher measured temperature. This may be due to the relatively low thermal conductivity of SiN_x, which can reduce heat flux into the wafer [136]. Finally, when using a fused silica (FS) base without a SiN_x layer on top, the peak temperature is significantly lower, as almost all absorption occurs in the a-Si layer and FS absorbs very little infrared light [137, 138].
Heat in-coupling naturally varies between samples and can lead to asymmetrical heat distribution throughout the sample. This effect is not considered in the current discussion, because the uncertainty for temperature measurements in this furnace, as reported in other studies, is $\pm 10^{\circ}$C, which limits the ability for in-depth analysis [139]. Ideally, each fired sample would be tracked individually. However, this process may also influence the temperature due to an increased thermal mass during the measurement. Besides the practical aspect of tracking every individual sample, the thermocouple can also damage the surface and lead to metal contamination. Thus, for the remainder of this work, the set peak firing temperature (SPFT) is used to characterize the firing profile. Since the shape of the firing profile significantly impacts the measured peak firing temperature, only two ramp-up profiles (firing with and without a dummy wafer) are used to enable a meaningful comparison of different SPFTs.

2.5. Metallization

Metallization is a key process in solar cell production. To understand it on a fundamental level, metal-semiconductor contacts are briefly examined. A band diagram of such a contact on (n) Si is shown in Figure 2.11(a) before and in Figure 2.11(b) after contact formation. Important quantities are the metal work function ϕ_m, the electron affinity of the semiconductor χ_s, and the semiconductor work function ϕ_s. Similar to a pn-junction, when metal and semiconductor are brought into contact, the Fermi levels align, leading to band bending. In the case of (n) Si, this introduces a barrier height ϕ_B, which can be calculated according to the Schottky-Mott rule [140]

$$q\phi_\mathrm{B} = q(\phi_\mathrm{m} - \phi_\mathrm{s}). \tag{2.29}$$

This rule is seldom confirmed experimentally, as additional electronic states can occur at the interface, leading to an effect known as Fermi level pinning, where the barrier height is mostly independent of χ_s.

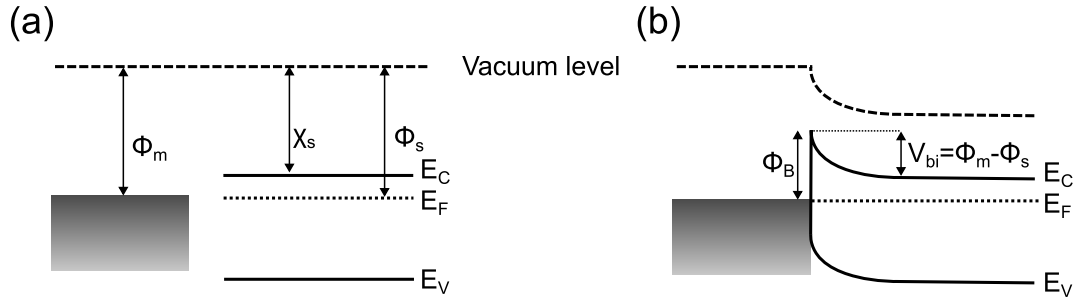

Figure 2.11.: *Band diagram for a metal-semiconductor contact (a) before and (b) after contact formation in the case of n-type Si. Adapted after [10].*

One can broadly distinguish between Schottky and ohmic contacts. For Schottky contacts, the condition $\phi_\mathrm{B} - \phi_\mathrm{s} > 0$ is fulfilled, which leads to rectifying behavior, meaning the contact allows current to flow easily in one direction (forward bias) but significantly restricts it in the opposite direction (reverse bias). An ohmic contact forms when $\phi_\mathrm{B} - \phi_\mathrm{s} < 0$, resulting in no significant energy barrier at the interface. Alternatively, it can form when the depletion region is sufficiently small, allowing favorable tunneling through the thin barrier. For (p) Si, these considerations still apply, but are reversed.

Ohmic contacts exhibit no rectifying behavior and show a linear $J-V$ curve. Depending on the specific application, different types of contacts are desirable. In the context of passivating contacts, the SiO_x reduces Fermi level pinning and the formation of a Schottky barrier at the interface between metal and semiconductor, which further boosts surface passivation and improves charge carrier selectivity [40].

There are different ways to metallize poly-Si-based passivating contacts. Some of these

methods include physical vapor deposition via evaporation (Section 2.5.1) [141], or screen-printing (Section 2.5.2) [142]. A brief literature review of poly-Si contacting for passivating contacts is given in Section 2.5.3.

Metallization is often carried out to produce metal fingers and busbars. Fingers are fine gridlines that collect current to the busbars, which are thicker lines transporting the collected current to an external circuit. As described in Section 2.1.2, a balance between shadowing losses and resistive losses must be struck for solar cell devices. Additionally, the cost of solar cells is heavily influenced by the usage of silver. Thus, several strategies to reduce silver consumption, such as reducing finger width, optimizing the printing process, or exploring alternative materials like copper, are being pursued. A key goal is to reduce cost while still maintaining efficient electrical conductivity.

2.5.1. Evaporation

Evaporation requires the use of shadow masks to achieve the desired structures. The samples, covered with masks, are placed in a sample holder inside a deposition chamber, while the metal pellets to be evaporated are placed in a crucible. After evacuating the chamber, an electron beam is directed onto the crucible, melting the metal. This process causes the metal to evaporate within the chamber. For this work, metal fingers with a width of 400 μm are realized through stacks composed of 50 nm thick titanium (Ti) and 1 μm thick silver (Ag), where Ti functions as an adhesion layer. In some layers, a 10 nm thick aluminum (Al) layer is deposited on top to ensure selectivity towards etching (Section 3.3.3). After evaporation, the samples are tempered at $\approx$ 200°C to improve contact quality. Unlike screen-printing, the metal-semiconductor contact is located only near the surface of the poly-Si layer.

2.5.2. Screen-Printing

Screen-printing is performed on 15.6x15.6 cm^2 wafers after SiN_x deposition and is the standard process in industrial solar cell production. A screen is covered with metal paste, where in this work Ag pastes were used. The desired pattern is produced using a squeegee to transfer the paste through the screen openings onto the sample. The printing process is strongly influenced by parameters such as squeegee hardness, pressure, and speed. After printing, the sample is immediately dried in a furnace at low temperatures of approximately 200°C for a few minutes. This is followed by a firing step, as explained in Section 2.4.3, to form the contact.

For this work, two different screens are used. The first one is employed to determine contact resistivities via transfer length method (TLM) measurements. This screen consists of 96 TLM patterns with finger widths of 30, 40, 50, and 60 μm, where each pattern has increasing finger spacings from 1 to 2.2 mm in steps of 0.2 mm. The second screen is used to determine the surface passivation after metallization ($J_{0,\text{Met}}$). This screen is composed of nine different 4x4 cm^2 areas with various metallization fractions between 0 and 21.8%. This variation is achieved by adjusting the equidistant spacing between the fingers, which have a width of 45 μm [17]. The actual metal fraction is determined through the measured finger width using optical microscopy images, which is usually slightly larger than the nominal width of the screen due to broadening during the printing and firing process.

2.5.3. Literature Review

As explained in Section 2.5.2, the metal paste is printed onto the wafer surface, on top of a SiN_x ARC layer, and rapidly heated and cooled in a firing step. The exact compositions of metal pastes are proprietary due to competitive patents, but they are typically composed of three key ingredients. Firstly, the glass frit, which is responsible for etching through the SiN_x layer and accounts for 1–10 wt% of the paste. Secondly, organic solvents and binders, which control the paste's viscosity and adhesion properties, and constitute about 10–15 wt%. The remainder consists of Ag microparticles of various sizes [143–145].
The contact formation during firing in conventional diffused emitter solar cells has been extensively studied over the past decades, and different models have been developed. These models will be briefly summarized and compared to those proposed for contact formation on TOPCon structures. For an in-depth discussion, one can refer to [17, 146].
At temperatures below 400°C, the organics "burn-out," which is essential for lowering the resistivity of the metal fingers. After this, the glass frit begins etching through the SiN_x layer. While the exact contact formation mechanism during firing remains a topic of debate, two leading hypotheses suggest electrochemical reactions are responsible. The first theory claims that the SiN_x layer is opened by the glass frit in the paste, often through PbO, via the redox reaction [147–149]

$$2\,\mathrm{PbO}_{\text{glass}} + \mathrm{SiN}_{\text{x,solid}} \longrightarrow 2\,\mathrm{Pb}_{\text{liquid}} + \mathrm{SiO}_{\text{2,glass}} + \frac{\text{x}}{2}\mathrm{N}_{\text{2,gaseous}}. \tag{2.30}$$

The second hypothesis suggests the dissolution of Ag as Ag^+ into the molten glass layer through the reaction of ambient O_2 [150]. This is followed by the diffusion of Ag^+ and O^{2-}

into the Si emitter, after etching the SiN_x layer via the reaction [146, 150]

$$4\,\mathrm{Ag_{glass}}^{+} + 2\,\mathrm{O^{2-}_{glass}} + \mathrm{SiN_{x,solid}} \longrightarrow 4\,\mathrm{Ag_{glass}} + \mathrm{SiO_{2,glass}} + \frac{\mathrm{x}}{2}\mathrm{N_{2,gaseous}}. \tag{2.31}$$

During the cooling phase of the firing process, the solubility of Ag in the glass is reduced. Thus, the enriched Ag atoms precipitate and grow into Ag crystallites [146]. This theory is based on observations that the number of free electrons at the silicon surface significantly influences the reaction and contact formation. For instance, a direct electron flow between the silver finger and the c-Si base has been found to hinder the formation of Ag crystallites, resulting in high contact resistivity. This phenomenon is known as the short-circuit effect [146, 150].

Both theories have their merits, though recent studies lean toward the Ag^+ ion etching mechanism. For example, adding Ag powder to the glass frit has been shown to suppress the PbO-based reaction [151]. Nonetheless, the glass frit continues to play a crucial role in adjusting the solubility of Ag^+ ions in the glass and in controlling the density of silver crystallites [150, 152]. Several studies have shown that these silver crystallites and colloids are crucial for current transport between the metal fingers and the silicon base [153–155].

For diffused c-Si emitters, the reactions during firing lead to isotropic etching of the silicon base. As a result, pyramid-shaped Ag crystallites are formed on the (100) surface, exhibiting an epitaxial relationship with the silicon crystal [153, 156, 157]. In the case of TOPCon cells, few investigations have been reported, primarily for LPCVD a-Si. Glatthaar et al. published results covering contact formation for APCVD (n) a-Si [17, 103, 152, 158]. It should be noted that the deposition method has a strong influence on the layer properties, which can lead to significant differences in contact formation.

Since large parts of this work are based on APCVD a-Si, a short overview of those results will be given. Although certain contact formation characteristics resemble those observed in diffused c-Si emitters, key differences are also apparent. Importantly, unlike in diffused emitters, no correlation between the crystal orientation of Ag and surrounding Ag crystallites has been observed [103]. This is to be expected, as poly-Si consists of differently oriented crystallites, with multiple poly-Si grains usually contacting a single Ag crystallite.

Similar to diffused emitters, glass frit etching of the SiN_x layer begins around 400°C. Above 600°C, etching through Ag^+ ions occurs, leading to selective etching in the poly-Si. Importantly, the cubic Ag crystallites typically stop at the interfacial oxide, which can be exploited to improve key solar cell parameters [103]. Common metrics for quantifying contact properties include the specific contact resistivity (ρ_C) and saturation current density in the metallized region ($J_{0,Met}$). For (n) poly-Si layers, ρ_C as low as 1 mΩcm^2 and $J_{0,Met}$ below 50 fA/cm^2 have been reported [152, 158–160]. However, contacting (p) poly-Si layers has proven

more challenging, with ρ_C often exceeding 2 mΩcm^2 and $J_{0,Met}$ above 150 fA/cm^2 [161–163]. Multiple factors contribute to this difference between (n) and (p) poly-Si. Firstly, for (p) poly-Si it is difficult to achieve similar doping concentrations of up to $3 \cdot 10^{20}$ cm^{-3} as in (n) poly-Si due to the lower solubility limit [164–166]. Especially the increased dopant in-diffusion for boron doped poly-Si presents a limiting factor, which decreases passivation due to increased Auger recombination [98, 163]. Secondly, a higher tunneling barrier height of 4.8 eV for (p) poly-Si compared to 3.1 eV for (n) poly-Si layers leads to a lower tunneling probability, which results in a higher contact resistivity (Equation (2.13)) and lower selectivity [77, 78]. Another contributing factor is the tendency for (p) poly-Si to form an electrically inactive boron rich layer during boron diffusion [167, 168]. This layer can limit charge carrier transport and increase ρ_C [150, 169]. Furthermore, it leads to an increased surface recombination and was speculated to degrade bulk lifetime [168, 170, 171].

Following the discussion of contact formation, the transport of charge carriers from the bulk Ag finger to the formed Ag crystallites will be briefly reviewed. Different conduction mechanisms can occur, which are expected to be similar between diffused emitters and poly-Si based contacts [17]. However, the contributions to transport vary depending on paste and firing conditions [172, 173]. In the case of textured surfaces, direct transport between finger and crystallites was found to be the dominating pathway, where the contact occurs increasingly at the pyramid tips [148, 172, 174]. This transport is usually limited through the contact area, as the conductivity of Ag itself is very high.

Another possible transport path is related to the glass frit, which often separates the finger and crystallites. As the glass frit usually is not conductive ($> 10^9$ Ωcm), it presents a barrier between the finger and the Si material below, which has to be overcome [153, 172]. This is usually done through tunneling. Direct tunneling requires a glass layer that is sufficiently thin (< 5 nm) [175]. For thicker glass layers, a multi-step tunneling step is more favorable, relying on metal colloids [176]. Finally, it might also be possible to design conductive glass frits which could lead to transport through the glass, as was speculated in [17]. Of course, a combination of all the described mechanisms can occur for transport between Ag finger and Ag crystallites.

2.6. Fired Passivating Contact

After discussing some key properties of TOPCon structures, a critical distinction must be made. In this work, the traditional poly-Si passivating contact with extended annealing is referred to as *high temperature passivating contact* (HTPC). This is to distinguish it from the *fired passivating contact* (FPC) approach, which will now be examined in detail. Sec-

tion 2.6.1 outlines the FPC principle, whereas Section 2.6.2 covers the main challenges and differences from the HTPC concept.

2.6.1. Principle

While the HTPC process employs a long annealing step at elevated temperatures ($> 800\,^{\circ}$C) for durations exceeding 30 min in a tube furnace, the FPC concept requires no such prolonged crystallization. It was first proposed by Ingenito et al. that a short annealing step could be sufficient to form a passivating contact junction [8]. This annealing step is comparable to the fast firing process used for metallization and hydrogenation (see Section 2.4.3). Ideally, the annealing is eliminated entirely and only the firing step remains. This step then combines metallization, dopant activation, partial crystallization, and hydrogenation, reducing both production time and cost [8, 68, 177].
Proof of principle was demonstrated by Ingenito et al. using PECVD (p) a-SiC$_x$ layers. The addition of carbon was done due to the high hydrogen content in the a-Si after deposition, which effuses during firing and can lead to layer delamination, referred to as blistering [27, 102]. Ingenito et al. achieved implied V_{OC} (iV_{OC}) values of up to 715 mV and saturation current density values of $J_{0,\mathrm{Pass}} = 11$ fA/cm^2 [8]. However, an additional firing step before SiN$_x$ deposition was still required to reduce blistering, diminishing the overall advantages of this technology. Merkle et al. demonstrated that APCVD (p) a-Si could achieve iV_{OC} values of up to 703 mV using only a single firing step after SiN$_x$ deposition [9]. This makes APCVD a promising candidate for further investigation. It has been shown that hydrogenation is crucial for achieving high passivation levels for FPC, even more so than for HTPC contacts [8, 134].
A key difference between FPC and HTPC is dopant in-diffusion, as this is a time-dependent process. This is evident in the doping profiles shown in Figure 2.12(a) for HTPC and FPC PECVD (n) a-Si samples, determined via electrochemical capacitance-voltage (ECV) measurements (described in Section 3.3.4). During the fast firing process, only a small amount of dopants diffuses through the oxide into the base. This results in a different band structure compared to well-crystallized layers, as depicted in Figure 2.12(b). For HTPC, the in-diffusion creates a buried junction, which ideally improves surface passivation by reducing minority carriers without increasing Auger recombination [8]. It further increases the tunneling probability through the oxide due to a decreased barrier height ΔE_{s}. According to Ingenito et al., the FPC concept compensates for the lack of in-diffusion by promoting an accumulation region at the wafer surface and maintaining a low defect density at the c-Si/SiO$_x$ interface. Crucially, accumulation of majority carriers is facilitated by partial crystallization during firing, as this directly activates dopants. The accumulation of carriers

enhances tunneling through the SiO_x. Similarly to HTPC, the number of minority carriers available for SRH recombination is reduced at the poly-Si/SiO_x/c-Si interface. The FPC approach may be particularly advantageous for (p) a-Si applications, as it avoids the formation of a boron-rich layer and prevents significant boron in-diffusion, which can limit passivation severely.

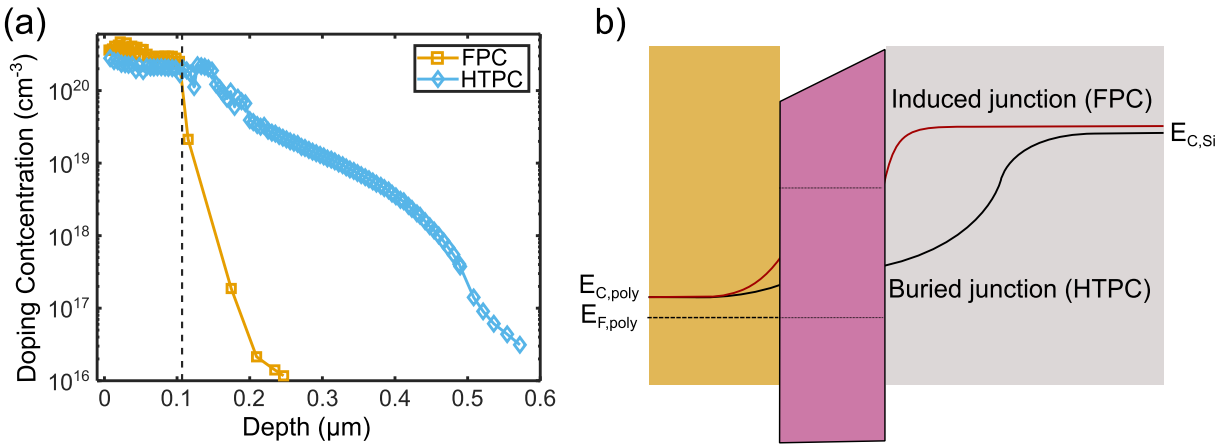

Figure 2.12.: *(a) Exemplary diffusion profiles determined via ECV measurements for a FPC and HTPC sample using PECVD (n) a-Si. (b) Conduction band edge for (n) poly-Si passivating contact for the HTPC and FPC approaches.*

2.6.2. Challenges

The FPC concept poses several challenges that must be addressed for successful implementation in solar cells. Despite the intriguing idea, many aspects of the FPC approach remain unexplored. Firstly, the understanding of passivation is still not complete. It is well-established that hydrogenation is crucial for achieving high passivation levels [8, 134]. However, it is unclear how firing temperature or shorter annealing steps before SiN_x deposition affect passivation, particularly for different interfacial oxides, which is investigated in Chapter 4.

Another challenge lies in reducing resistivity within the poly-Si layers both laterally and vertically, which is expected to be increased compared to HTPC samples due to only partial crystallization of the a-Si. A detailed understanding of transport mechanisms within the poly-Si layers and the process of dopant activation is necessary. Similarly, charge carrier transport through the oxide has been investigated only superficially for low thermal budgets, with no clear conclusions yet [68]. This property is crucial since the junction must allow charge carriers to reach the metal contacts. The interfacial oxide may require adjustments depending on the thermal budget to ensure adequate transport from the c-Si base to the poly-Si, while maintaining high passivation levels. These characteristics are examined in Chapter 5

In addition to passivation, achieving a low contact resistivity after firing is a key issue. Several attempts to contact FPC junctions have been made. Firat et al. reported a contact resistivity of 7 mΩcm^2 for LPCVD (n) a-Si using Ag screen-printing [178]. Although $J_{0,\text{Pass}}$ values were as low as 5 fA/cm^2, $J_{0,\text{Met}}$ values in the metallized regions exceeded 1000 fA/cm^2, which is insufficient for cell efficiencies $>$ 20% [68]. Similarly, Libraro et al. reported Al screen-printed PECVD (p) a-SiC$_x$ layers with contact resistivities down to 17 mΩcm^2 [179]. However, very high recombination at the metal contacts was observed, and an additional firing step before SiN$_x$ deposition was required, which reduces the advantages of the FPC approach. The challenge of screen-printing FPC samples while maintaining high passivation likely stems from lack of dopant in-diffusion during junction formation. In this work, the multilayer approach aims to mitigate passivation degradation after metallization, as discussed in Chapter 6.

3. Characterization Methods

In this chapter, the key characterization methods are described along with the analysis procedures. Section 3.1 covers measurements to determine the passivation quality, which was done through *photoconductance* decay (PCD) measurements and *photoluminescence* (PL) imaging. Next, methods to investigate the crystallite structure of the poly-Si are introduced in Section 3.2. These include *X-ray diffraction* (XRD) and *Raman effect* measurements to determine the poly-Si crystallite size and crystallinity, as well as a novel crystallite size imaging technique utilizing *scanning electron microscopy* (SEM). Electrical characterization via *four-point probe* (4PP), *transfer length method* (TLM), *Hall effect*, and *electrochemical capacitance-voltage* (ECV) measurements is introduced in Section 3.3.

3.1. Passivation

This section describes two measurement methods to quantify passivation of samples. In Section 3.1.1, PCD measurements for lifetime samples are described, while in Section 3.1.2 a method based on PL measurements to characterize the passivation of metallized samples is shown.

3.1.1. Photoconductance Decay

Photoconductance decay measurements were done using a Sinton lifetime Tester WCT-120. The sample is placed on a stage and illuminated with a light flash. This flash leads to an excess charge carrier density Δn, which alters the sample's conductivity $\Delta\sigma$ and is measured via an induction coil underneath the stage in a 3 cm diameter area [180]. The average excess charge carrier density Δn_{av} can be calculated by

$$\Delta n_{\mathrm{av}} = \frac{\Delta\sigma}{qd(\mu_{\mathrm{n}} + \mu_{\mathrm{p}})}, \tag{3.1}$$

where d is the thickness of the sample, and $\mu_{\mathrm{n/p}}$ the electron/hole mobility [181]. The generation rate G is determined via a reference cell. Using Equation (2.5) and the definition of

the effective minority carrier lifetime τ in Equation (2.6), the expression

$$\frac{d\Delta n_{\text{av}}(t)}{dt} = G - R = G - \frac{\Delta n_{\text{av}}}{\tau} \tag{3.2}$$

can be found [182]. Thus, the relationship

$$\tau = \frac{\Delta n_{\text{av}}}{G - \frac{\partial \Delta_{n_{\text{av}}}}{\partial t}} \tag{3.3}$$

can be obtained from Equation (3.2). PCD measurements are typically operated in one of two extreme conditions of Equation (3.3). Firstly, in the quasi-steady-state (QSS), where the light flash is long compared to τ. This leads to $\frac{\partial \Delta_{n_{\text{av}}}}{\partial t} = 0$, simplifying Equation (3.3) to $\tau = G/\Delta n_{\text{av}}$. Secondly, the transient mode uses a light flash that is short compared to τ, leading to $G = 0$ during the decay of Δn_{av} and simplifying Equation (3.3) to $\tau = \Delta n_{\text{av}} \left(\frac{\partial \Delta_{n_{\text{av}}}}{\partial t} \right)^{-1}$. PCD measurements have to be done for non-metallized samples and are ideally carried out using symmetric lifetime samples.

Implied Open Circuit Voltage iV_{OC}

In this work, the iV_{OC} is used to quantify the passivation quality of lifetime samples. It can be seen as an upper limit for the V_{OC} and can be calculated according to

$$iV_{\text{OC}} = \frac{k_{\text{B}}T}{q} \ln \left(\frac{\Delta n_{\text{av}}(\Delta n_{\text{av}} + N_{\text{base}})}{n_{\text{i}}^2} \right), \tag{3.4}$$

with the base doping N_{base} and the intrinsic carrier concentration n_{i} at 25°C [183]. Δn_{av} depends on the incoming photon flux. Consequently, iV_{OC} is evaluated at one sun illumination and is measured with a long flash throughout this work. Uncertainties were determined by standard deviation of at least three different samples.

Saturation Current Density J_0

The saturation current density J_0 from the one-diode model in Equation (2.1) can be seen as the sum of all recombination loss currents [184]. Different ways to extract J_0 via PCD measurements have been proposed. This evaluation follows the approach in [181] with adjustments after [185, 186]. When subtracting the intrinsic lifetime from the measured lifetime, one can find the corrected lifetime τ_{corr}. According to Equation (2.6), τ_{corr} is only a

function of τ_{SRH} and τ_{Surf}, yielding

$$\frac{1}{\tau_{\text{corr}}} = \frac{1}{\tau_{\text{SRH}}} + \frac{2(N + \Delta n_{\text{av}})}{qdn_{\text{i}}^2} J_0. \tag{3.5}$$

J_0 can be graphically extracted through a fit of Equation (3.5), giving J_0 as a fit parameter. This is typically measured using a short flash in transient mode on symmetrical samples. For an in-diffused emitter, J_0 refers to the saturation current density of the emitter. In the case of poly-Si/SiO_x based passivating contacts, the measured saturation current density is a mixture of the surface current density from emitter and surface [23, 40]. In the following, this combined saturation current density for passivating contacts without metallization is referred to as $J_{0,\text{Pass}}$.

3.1.2. Photoluminescence Imaging

Photoluminescence (PL) imaging can be used to determine the spatially resolved passivation level. The setup consists of a laser source (wavelength 808 nm) that irradiates the sample placed on a measurement chuck, which can also act as an LED illumination source, as shown in Figure 3.1(a). This method leverages the fact that radiative recombination is more pronounced when other recombination pathways are weaker, as illustrated in Figure 2.2. Consequently, regions with higher lifetimes exhibit a stronger PL signal. The emitted photons are then focused and detected by a camera. Typically, a standard PL setup allows only for qualitative imaging without elaborate calibration of the count rates [17]. To get quantitative results, a *time-resolved photoluminescence* (TRPL) approach is employed for metallized samples.

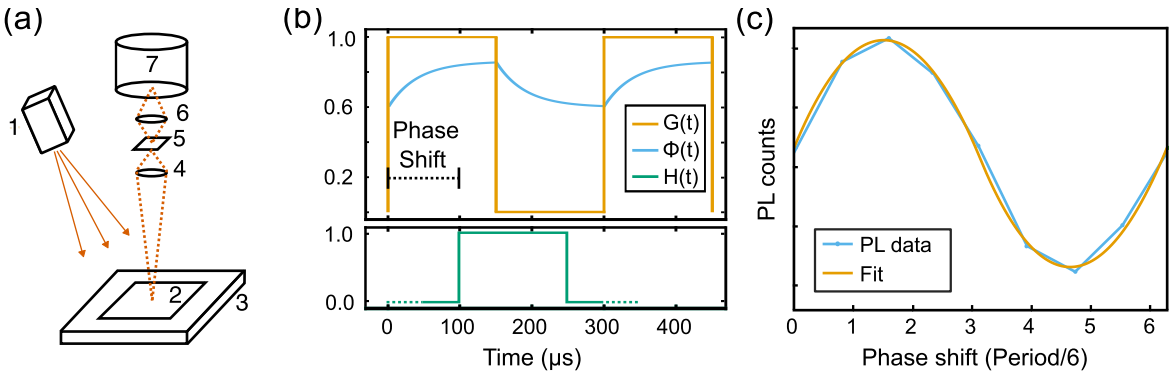

Figure 3.1.: *(a) Schematic of a PL setup with the (1) laser source illuminating the (2) sample placed on a (3) metal chuck. The emitted photons are focused by a (4) lens onto a (5) shutter wheel and refocused through a (6) lens onto the (7) CCD camera. (b) Generation signal G(t) modulated by the shutter wheel function H(t), leading to the PL signal Φ(t), and the corresponding phase shift. (c) Exemplary PL fit for different phase shifts via the intensity model in [180]. (a) and (b) adapted from [17, 180].*

A detailed description of this method can be found in [180, 187]. The measurement principle is based on a modulated generation $G(t)$ with the frequency f, as depicted in Figure 3.1(b). After each light pulse, the PL signal $\Phi(t)$ decays, which can be used to extract the charge carrier lifetime. To improve the time resolution, $\Phi(t)$ is not measured directly. Instead, a switchable image intensifier (shutter wheel) is placed in front of the camera to modulate the PL signal $\Phi(t)$ with the rectangular transmit function $H(t)$. This allows to scan the luminescence signal with different phase shifts between shutter wheel and excitation, where multiple images I_{n} with different phase shifts are recorded. Correspondingly, the camera signal $I_{\mathrm{n,i}} = \int_0^T \Phi_{\mathrm{i}(t)} H(t)\,\mathrm{d}t$ can be calculated for every pixel with the shutter period T [180]. Through an intensity model, the PL data can be fitted for every pixel of the recorded image, as shown in Figure 3.1(c) [180]. Finally, the excess charge carrier density Δn can be determined via

$$\Delta n = \frac{\tau(1-R)\int G(t)\,\mathrm{d}t}{d}, \tag{3.6}$$

where R is the reflectivity and d the sample thickness [188]. This requires choosing the frequency $G(t)$ in such a way that Φ(t) $\gg$ $\Delta\Phi$(t). It has been shown that this approach agrees well with results from PCD measurements [17].

TRPL measurements are used to determine the current density $J_{0,\mathrm{Met}}$ in the metallized area. As described in Section 2.5.2, different metallized area fractions are printed on one side of a symmetrical passivating contact structure and fired. To evaluate $J_{0,\mathrm{Met}}$, the non-metallized area in the middle of the wafer is measured via PCD. This is used to determine a suitable generation G for the measurement and correspondingly the illumination intensity of the laser. The frequency of G is estimated for every generation individually, where the thumb rule $f = 3/\tau$ can be applied. After calibrating the laser flux and focusing the sample, TRPL measurements are conducted at various injection levels and frequencies, resulting in lifetime maps for each injection level, as shown in Figure 3.2(a).

It is already apparent for this particular sample that an increasing metal fraction decreases the carrier lifetime, pointing towards a higher recombination underneath the metal contacts. These lifetime maps can be used to determine J_0 for every metallized region, similar to the PCD method, by plotting the inverse corrected lifetime against Δn. In high injection, this behavior is linear, and the slope leads directly to J_0, as is shown exemplarily in the inset of Figure 3.2(b) [183]. Finally, $J_{0,\mathrm{Met}}$ can be determined by a linear fit of the individual J_0 values as a function of the metal fraction. The extrapolation to a metal fraction of 100% yields the $J_{0,\mathrm{Met}}$ value, as shown in Figure 3.2(b) [189].

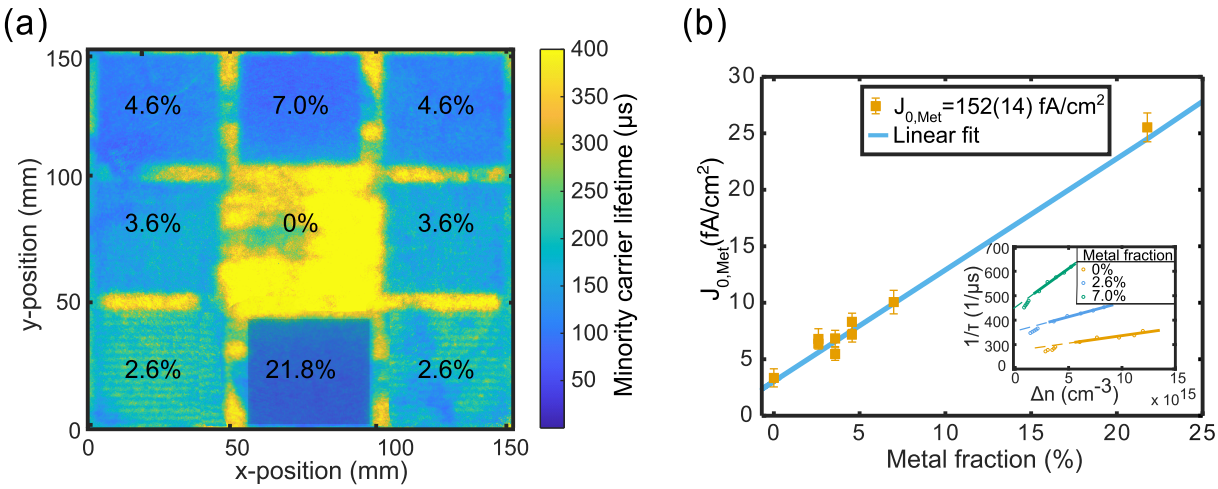

Figure 3.2.: *(a) TRPL image for an APCVD (p) a-Si sample recorded at 1 sun illumination. (b) Exemplary $J_{0,Met}$ determination for different metal fractions. The inset shows examples of the J_0 fitting procedure.*

Next, a brief summary of the limitations and uncertainties will be given. A detailed discussion can be found for instance in [17].

For TRPL measurements, the sample needs to be in high injection condition, where surface recombination is dominating. The usage of a lowly doped base substrate helps in achieving this condition even with a lower illumination intensity. As is indicated in the inset of Figure 3.2(b), for a lower injection the relationship between $1/\tau$ and Δn is no longer linear. This is especially an issue for samples with a low passivation level, where an accurate $J_{0,\mathrm{Met}}$ determination then is no longer possible. Another source of uncertainty is the fitting model to the PL data, where the assumption $\tau(\Delta n) \approx \tau$ is made. According to [188], the deviation between theoretical and measured Δn values is less than 8%, which is comparable to uncertainties of PCD measurements. Furthermore, a significant contribution to the measurement uncertainty is that Δn is assumed to be homogeneously contributed over the sample thickness. However, the relevant quantity is the carrier density directly at the metal contacts. Several different authors published results of Quokka simulations investigating this effect [17, 190, 191]. It was found that the deviation between different Δn distributions is especially significant for high injection levels $\Delta n > 1 \cdot 10^{16}$ cm^{-3}, which is typically not reached for this setup. This deviation is also notable for low metallization fractions with low lifetimes, where $J_{0,\mathrm{Met}}$ determination cannot be conducted reliably [17]. An additional consideration is the homogeneity of the a-Si across the entire sample. This can be an issue, especially for APCVD a-Si at the wafer's edges, and can lead to inaccuracies in determining the J_0 values of the individual metallized areas accurately. Consequently, every single 4x4 cm^2 area of the TRPL image was inspected during evaluation. If required due to inhomogeneities near the edges, these areas were excluded from the entire evaluation process.

3.2. Microstructure

The following section describe methods for obtaining information about the crystallite structure. A major focus is on XRD measurements, discussed in Section 3.2.1, which are used to determine the crystallite size and strain of poly-Si layers. For these characterization methods, no SiN_x layer should be present on the sample's surface. Consequently, the SiN_x layer was etched away in a 10% hydrofluoric acid (HF) solution or was not deposited at all. In Section 3.2.2, SEM imaging is introduced, which is mostly used to analyze contact formation of Ag crystallites or to determine pinhole densities in the interfacial oxides. Furthermore, SEM images can in some cases be employed to determine the crystallite size of the poly-Si layers, which may be utilized to confirm the validity of XRD measurements. Finally, Raman effect measurements, used for estimating the crystallinity of poly-Si films, are briefly explained in Section 3.2.3.

3.2.1. X-Ray Diffraction

Measurement Setup

The setup of the Bruker Advance D8 instrument used for XRD measurements is shown in Figure 3.3. It consists of an X-ray tube mounted on a goniometer, where electrons are accelerated toward a copper anode under a voltage of 40 kV and a current of 40 mA. X-ray radiation can be divided into two different spectra. Firstly, the *characteristic spectrum* emerges when an incoming electron collides with an electron from the inner shell ($n = 1$) of a copper atom, knocking it out of its orbit. To minimize the total energy of the system, this electron is replaced by one from an outer shell. The energy difference during this transition is released in the form of X-rays, and the wavelength depends on the shell from which the electron originated. Transitions from the second inner shell ($n = 2$) to $n = 1$ are referred to as K_α X-rays, while those from $n = 3$ to $n = 1$ are known as K_β X-rays. Cu K_α rays dominate the intensity spectrum and have an energy of 8.04 keV, corresponding to a wavelength of $\lambda = 0.154$ nm [192]. A second mechanism of X-ray production involves a continuous spectrum known as *Bremsstrahlung*, typically weaker than the characteristic spectrum. This occurs when an electron interacts with the electric field of the nucleus, causing it to decelerate. The loss of energy is then compensated by photon emission with an energy up to the initial kinetic energy of the electron.

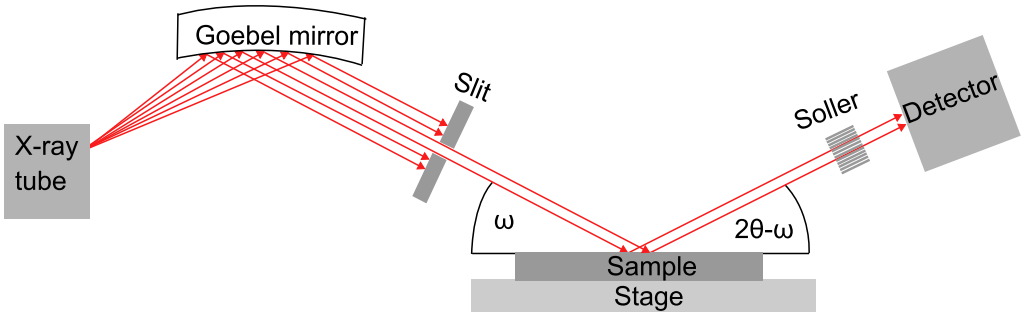

Figure 3.3.: *Experimental setup for XRD measurements. After generation of the X-rays via a Cu anode, a Goebel mirror produces a parallel beam that is further collimated via a divergence slit. The incident X-rays are projected onto the sample under the incidence angle ω, while the diffracted signal is picked up by the detector, which is scanned along the 2θ axis. Additional optics, such as divergence or Soller slits, can be placed in the beam path before the detector.*

After X-rays are generated, a Goebel mirror is positioned in the beam path. This parabolically bent mirror converts the divergent beam into a parallel one with low divergence, even when the beam strikes at different locations. This leads to monochromatization of the K_α radiation, while Bremsstrahlung is suppressed [193]. As shown in Figure 3.3, additional optics, such as divergence slits with widths ranging from 0.1-1.2 mm, further reduce beam divergence and prevent overspill. Inserting Soller slits, which consist of repeating blades that absorb most of the incoming X-rays, further enhances the beam quality [194]. These slits are classified by an angle $\alpha \approx 2d/l$ (in this case, 2.5°), where d represents the distance between blades and l their length [195]. However, using Soller slits also reduces the signal strength, extending the measurement time to maintain a high signal-to-noise ratio.
The sample was placed on a motorized x-y-z stage for measurement, where the spot size is influenced by the optics used. According to Snell's law, the incident and reflected angles must be equal when the beam interacts with the sample. Constructive interference of diffracted rays follows *Bragg's law*

$$n\lambda = 2d_{\mathrm{hkl}} \sin\theta, \tag{3.7}$$

where θ is the diffraction angle, and d_{hkl} refers to the distance between parallel lattice planes, known as Miller indices (hkl), which specify the orientation of the planes [109]. This interference occurs when the path length difference between waves scattered from adjacent planes equals an integer multiple of the wavelength, while destructive interference takes place if this difference is a half-integer multiple. In the case of an ideal crystal with an incident angle θ deviating from the Bragg relation, a deeper lattice plane within the crystal can always be found with a path length difference of 0.5λ, resulting in destructive interference, canceling out any scattering [109].

However, real crystals contain imperfections and often consist of differently oriented crystallites, which are coherently scattering domains [109]. In smaller crystallites, a plane cannot always be found to cancel out scattering at angles deviating from the Bragg condition. This leads to a broadening of the reflection for crystallites with sizes $<$ 100 nm. For a poly-Si layer, differently oriented grains can be observed through multiple diffraction peaks, as shown in Figure 3.4(a) for an APCVD (n) poly-Si sample. The lower limit for detection of crystallites through XRD measurements is in the range of 1-3 nm, where the peak broadens to the point of being indistinguishable from the background signal [109].
After the rays are diffracted, the signal is detected by a line detector composed of 191 channels. This detector has an angular opening of 2.92°, resulting in an angular resolution of 0.015°. Additional optics, such as a divergence slit or a Soller slit, can be inserted into the beam path before the detector to improve signal quality [196].
XRD measurements can be performed in different measurement settings. The most common one is the *Bragg-Brentano* ($\omega/2\theta$) configuration, where the incidence and detector angles are varied simultaneously, enabling a high signal output. Another prominent mode is *grazing-incidence-XRD* (GIXRD), where a constant low incidence angle ω is maintained, while the detector angle is varied by increasing 2θ. This technique is suitable for thin film investigations ($d <$ 1000 nm), as it increases the interaction volume of the X-rays with the poly-Si [196]. The penetration depth $z(\theta)$ can be calculated through

$$z(\omega) = \frac{-\lambda\sqrt{(\omega^2 - \omega_c^2) + \sqrt{(\omega^2 - \omega_c^2)^2 + 4\beta_a^2}}}{4\beta_a\sqrt{2}\pi}, \tag{3.8}$$

where ω_c is the critical angle for total reflection, and $\beta_a = \lambda\mu/(4\pi)$ is the absorption factor with attenuation length μ [196, 197]. The factor β_a is material-specific and heavily influenced by the crystallinity and doping of the poly-Si. Choosing an incidence angle near the critical angle results in a penetration depth of just a few nanometers. Hence, the incidence angle should be chosen in accordance to the poly-Si thickness. For example, using data from the NIST database with $\mu =$ 261.76 cm^{-1}, the penetration depth at $z(1°)$ is approximately 200 nm, while at $z(5°)$ it is about 1500 nm [198].

Scherrer Equation

The following discussion about measurement modes and their evaluation has been published in [199], where all major aspects of the work were carried out by the author, including experimental design, data collection, analysis, and manuscript preparation. In Figure 3.4(b), the (111) poly-Si peak is shown for different GIXRD incident angles of a $\omega/2\theta$ measurement for a 5DT (n) a-Si sample, corresponding to a thickness of 250 nm. Before each measure-

ment, the sample was aligned by a z-axis scan.

It is evident that the signal strength is enhanced for the GIXRD measurements compared to the $\omega/2\theta$ measurements. For even thinner layers ($<$ 100 nm), the Bragg-Brentano geometry becomes unsuitable due to insufficient signal strength. An additional advantage of GIXRD measurements is the suppression of background noise from the Cz wafer, which otherwise interferes with the poly-Si signal for the (400) peak at $2\theta \approx 70°$. Another clearly visible effect is substantial peak broadening at lower incidence angles due to the beam footprint on the sample [196]. It has been observed that this broadening effect is enhanced by the use of a larger divergence slit. Quantitatively, beam footprint broadening can be described by $G_{\mathrm{hkl}}(\omega) = \frac{180}{\pi}\frac{f\sin(2\theta-\omega)}{R\sin\omega}$, where f is the primary slit width and R is the goniometer radius [196, 200]. Inserting these parameters for the here used instrument, one gets $G_{111}(1°) = 1.94$ and $G_{111}(5°) = 0.37$, explaining the broadening at lower angles, which presents a challenge for crystallite size determination.

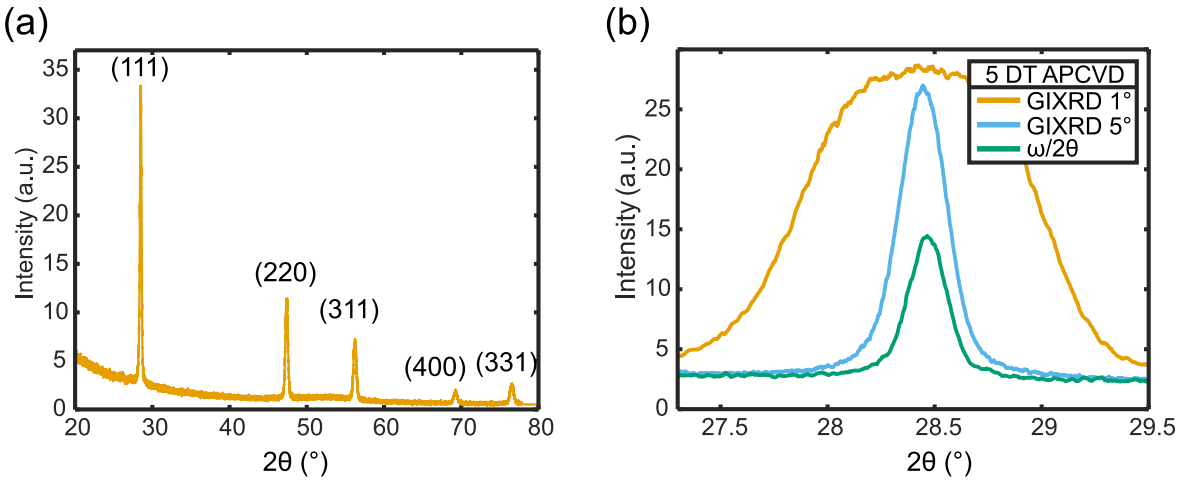

Figure 3.4.: *(a) Exemplary XRD spectrum for an APCVD (n) poly-Si sample after crystallization. (b) (111) poly-Si peak for different measurement modes for a 250 nm thick 5DT APCVD (n) poly-Si layer [199].*

This is due to the fact that the peak width can be interpreted as a measure of the poly-Si crystallite size L. To evaluate this quantitatively, Paul Scherrer formulated the *Scherrer equation* [201]

$$L = \frac{K\lambda}{\beta\cos\theta)} \tag{3.9}$$

for the individual peak width β, which is often used to determine crystallite sizes [202, 203]. In many publications the *full width at half maximum* (FWHM) is taken as a measure of β. However, it was found that the determination via FWHM tends to overestimate the crystallite size [109]. Instead, the *integral breadth* (IB) is used in this work to determine L. IB represents the width of a rectangle with the same height and area as the peak, and is calculated by dividing the line profile area by the profile height.

Rietveld Refinement

So far, only crystallite size has been considered as a peak broadening mechanism. However, the application of Equation (3.9) neglects different sources of broadening, such as those originating from the instrument itself, crystallite size distribution, or strain within the layer [109]. Strain quantifies the displacement of atoms from their ideal positions, and its effect on peak broadening is often overlooked in crystallite size determination. A quick way to estimate the strain ε for a given sample is through a *Williamson-Hall plot* [204, 205]. In this approach, the strain-related broadening β_{Strain} is added to the crystallite size broadening β_{Crystal} in Equation (3.9) to yield

$$\beta_{\text{Tot}} = \beta_{\text{Strain}} + \beta_{\text{Crystal}} \quad \Rightarrow \quad \beta_{\text{Tot}} \cos\theta = \varepsilon \sin\theta + \frac{K\lambda}{L}. \tag{3.10}$$

This relation takes advantage of the fact that strain and crystallite size have different angular dependencies. An estimation of strain can be obtained graphically by solving Equation (3.10), as shown in Figure 3.5(a). However, it is important to note that this method provides only a rough estimate due to the limited number of poly-Si XRD peaks (a maximum of five). For example, in the case of a 4DT 200 nm thick crystallized APCVD (n)a-Si layer, a crystallite size of $D \approx$ 78 nm and $\varepsilon \approx$ 0.007 is determined. This value is significantly larger than the crystallite size of 34 nm obtained using the simple Scherrer equation. Therefore, strain broadening should not be neglected when determining crystallite size.
An alternative evaluation method that considers these factors is known as the *Rietveld refinement* [196, 206] and was performed here using the commercial software *TOPAS* [207]. The procedure is based on adjusting an assumed structural model of the investigated sample. In this work, the structure was assumed to be a Fd-3m space group. A theoretical diffraction pattern was calculated, taking into account a polynomial background subtraction and additional fitting parameters, such as surface roughness after Pitschke et al. [208], zero error peak shift, lattice constant, scale factor, and crystallite size. Additionally, the instrumental contribution was modeled using the fundamental parameter approach (FPA), where the instrument configuration was specified [209]. Fit quality was evaluated using R-factors, which ensure the validity and comparability of the evaluation procedure between different samples. A more detailed explanation of this process can be found in [206, 210]. As a result, no concrete error has been determined for the XRD crystallite sizes. The diffraction profile was then fitted using a *pseudo-Voigt* function

$$V = nG_{\text{a}} + (1-n)L_{\text{o}}, \tag{3.11}$$

where G_a and L_o are Gaussian and Lorentzian functions. Only the integral breadth of the Lorentzian fit is used to determine the crystallite size, applying the Scherrer equation. The width of the Gaussian part β_{Strain} can be employed to calculate the strain ε via [202, 211]

$$\varepsilon = \frac{\beta_{\text{Strain}}}{\tan\theta}. \tag{3.12}$$

It has been reported that higher doping concentrations and longer annealing at high temperatures can increase strain within the layer, which may also be heavily influenced by the deposition and doping type [212–214].

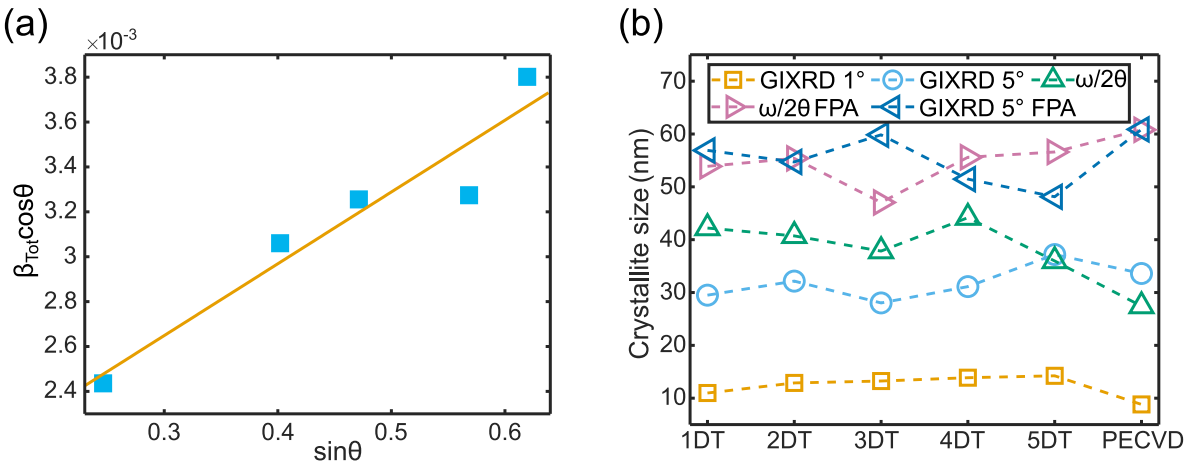

Figure 3.5.: *(a) Exemplary Williamson-Hall plot for a 4DT APCVD (n) poly-Si layer after crystallization for the respective XRD diffraction peaks. (b) Crystallite sizes for different measurement modes evaluated via Scherrer equation and Rietveld refinement for a different number of drive-throughs for APCVD (n) a-Si as well as a PECVD (n) a-Si layer [199].*

Comparison of Different Evaluation Methods

The effect of various measurement and evaluation methods is shown in Figure 3.5(b) for different DT of APCVD (n) a-Si and a PECVD (n) a-Si layer after crystallization at 920°C. As expected from the comparison of different measurement modes in Figure 3.4(b), GIXRD measurements at $\omega = 1°$ lead to a significantly underestimated crystallite size compared to the other measurement modes. On the other hand, GIXRD measurements at $\omega = 5°$ yields larger crystallite sizes, while the $\omega/2\theta$ mode gives slightly larger sizes by using just the Scherrer equation, which is due to the remaining peak broadening in the GIXRD configuration. However, especially for the 50 nm thick poly-Si layer, the signal strength is reduced significantly and requires a longer measurement time for a valid diffraction pattern.
One can further observe in Figure 3.5(b) that Rietveld refinement results in even larger crystallite sizes in the range of 50-60 nm, where the GIXRD and $\omega/2\theta$ mode widely agree with one another. There have been attempts to consider beam footprint broadening quantita-

tively in Rietveld refinements. With the current setup available at University of Konstanz this is not easily possible. However, the usage of a small divergence slit was found to minimize the broadening effect in the case of $\omega = 5°$. Thus, for most of this work, XRD measurements have been performed in the grazing incidence configuration, as this presents a good compromise between signal strength for thin poly-Si layers and peak broadening.
Finally, it should be stressed that the crystallite size mostly corresponds to layer scattering perpendicular to the surface [199]. Information about the crystallite shape and size distribution is not easily obtainable through XRD measurements, which can be acquired using imaging techniques.

3.2.2. Scanning Electron Microscopy

Often transmission electron microscopy (TEM) is used to determine the poly-Si crystallite size from images [103, 192, 215]. However, TEM requires time-intensive sample preparation, making it unfeasible to be used for a large number of samples [199]. Additionally, it was not possible to record TEM images in the scope of this work. Thus, a novel crystallite size imaging technique was used to assess the accuracy of XRD results. This technique relies on SEM imaging in combination with a HF etching step, which is briefly explained next. A detailed description can be found in [216].
SEM images overcome the optical resolution limit due to the shorter wavelength associated with electrons compared to photons. The main components of the SEM setup are an electron gun, various electromagnetic lenses, scan coils, two detectors, and a cathode ray tube [216]. After the emission of electrons from the electron gun, they are accelerated in a vacuum. The resulting electron beam is focused by the lens system and scanned across the surface by scan coils.
When the incident *primary electrons* hit the sample, different scattering interactions occur, leading to various types of electrons being detected. The most relevant in this work are *secondary electrons*, which originate from inelastic scattering in the surface region and typically have energies in the range of 2-5 eV. Another type of electron is the *backscattered electron*, produced by elastic scattering deeper within the sample, with energies exceeding 50 eV. Signals are detected by two types of detectors, both mostly sensitive to secondary electrons. The *Inlens* detector, aligned with the primary electron beam, is sensitive to low-acceleration voltage signals, while the *Everhart Thornley* detector, positioned nearly perpendicular to the primary beam, is better suited for capturing surface topography information.

HF-SEM Method

To examine the cross-section via SEM images, the sample is polished using argon *ion-milling* with an ArBlade 5000 from Hitachi High-Tech Corporation. During milling, the sample is rotated within a 60° range to avoid shadowing effects. The milling time depends on the polished area and layer thickness. However, even after ion-milling, SEM images do not provide sufficient contrast resolution to distinguish different poly-Si crystallites. Contrast was found to improve by dipping the sample in a 2.5% diluted HF solution for 1 s. This etching step is believed to etch the crystallite boundaries more quickly than the interior grains themselves, enhancing imaging contrast [199]. Dopant segregation at grain boundaries during crystallization likely contributes to this effect [17], as no crystallites could be resolved after short crystallization times or for intrinsic a-Si.
The short etching time is critical for obtaining adequate images. Increasing the etching time results in round etch artifacts covering the cross-section. *Energy-dispersive X-ray* (EDX) measurements indicate that copper contamination, caused by the combination of ion-milling and HF etching, contributes to these artifacts. This contamination can be significantly reduced by shortening the etching time to 1 s and using a silicon cover during ion-milling. Exemplary images obtained using this HF-SEM procedure are shown in Figure 3.6 for a 4DT APCVD sample and for a PECVD layer after crystallization.

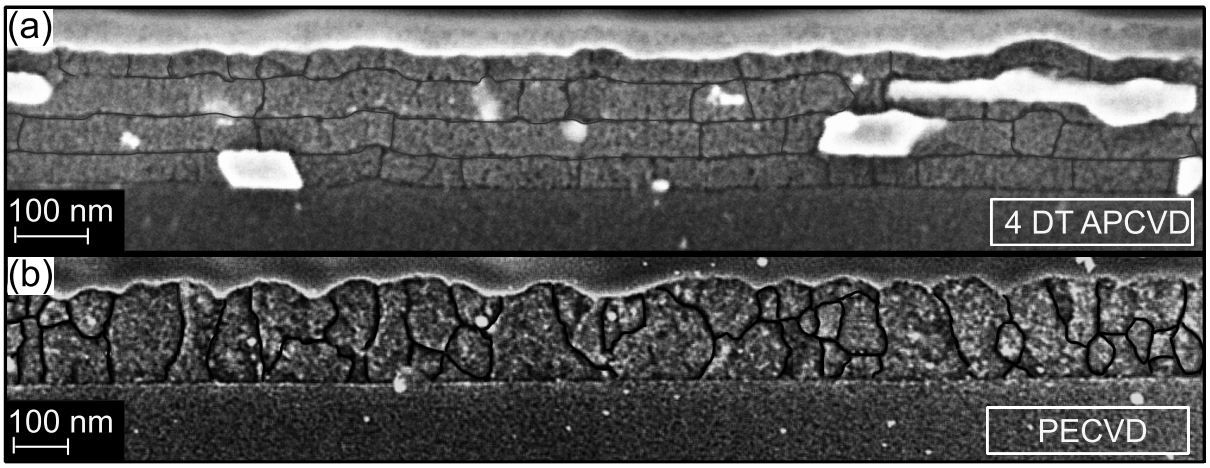

Figure 3.6.: *Exemplary HF-SEM images for an (a) 4DT APCVD (p) a-Si sample and a (b) 140 nm thick PECVD (n) a-Si sample after crystallization, SiN_x deposition, ion-milling, and HF etching [199].*

The image of the APCVD layer aligns well with TEM investigations of similar samples, as published in [103]. Notably, APCVD poly-Si crystallites generally exhibit a cuboidal shape, with a width greater than their height. This differs significantly from PECVD a-Si, as shown in Figure 3.6(b), where no clearly ordered structure is visible. Additionally, white spots can be observed within the poly-Si layer. These spots are present instead of the poly-Si

crystallites and are believed to represent crystallites with different orientations.

Evaluation of HF-SEM Data

Imaging techniques enable the extraction of width, height, and area of individual crystallites, along with their distribution, determined using a conventional image editing tool. Figure 3.7(a) illustrates examples of these distributions, showing crystallite heights and their relative frequencies. One can see that the distribution for APCVD layers is relatively narrow, with a mean value close to the a-Si layer thickness. For the PECVD layer the distribution is notably broader. These differences highlight a distinctive feature of each deposition technique for crystallized layers.

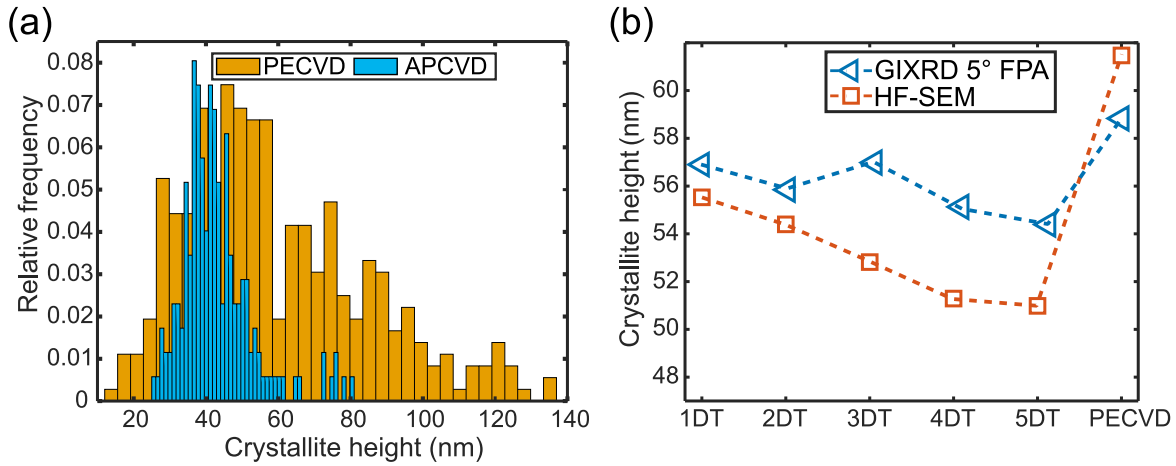

Figure 3.7.: *(a) Histogram of crystallite heights for PECVD and APCVD (n) a-Si layers determined via HF-SEM. (b) Comparison between HF-SEM and XRD evaluation via FPA Rietveld refinement for different numbers of DT and a PECVD sample after crystallization [199].*

SEM analysis, however, is prone to error due to manual determination and the limited statistics available. These errors can be reduced by averaging over multiple images, as was done here. Another issue is the resolution and quality of the images, which can sometimes make it difficult to clearly identify crystallite dimensions. Therefore, this technique is used here primarily to confirm the validity of XRD measurements. Figure 3.7(b) shows a comparison of crystallite sizes determined via XRD Rietveld refinement and the HF-SEM method for different layer thicknesses. The results largely agree, further validating the XRD evaluation. Additionally, with an increasing number of DT, the crystallite height decreases slightly. This is likely due to the reduced layer thickness with multiple DT, making it more difficult to accurately control the poly-Si thickness [17]. Due to the ease of XRD and the challenges associated with HF-SEM for non-crystallized layers, XRD was used to determine crystallite sizes for the remainder of this work.

3.2.3. Raman Effect

Apart from crystallite size, *crystallinity* is another quantity describing the crystal structure. It can be determined using the Raman effect, a nonlinear optical process in which incoming photons are scattered inelastically [217]. The basic principle involves photon collisions with atoms, leading to the excitation of rotational or vibrational energy modes. As the system relaxes back to the ground state, a photon is emitted, leading three possible outcomes. If the ground state energy after relaxation is identical to the one before excitation, it is referred to as *Rayleigh scattering*, which is elastically. However, when the vibrational energy level after relaxation is larger than the starting level, this is called a *Stokes shift*. Similarly, if the molecule is already excited and the initial energy level is higher than the final energy state, the shift is known as *anti-Stokes* [218].

A laser with a wavelength of 488 nm and a power of 1 mW, sufficient to prevent laser crystallization during the 60 s measurement, was used to excite the energy modes. Only the Stokes part of the spectrum was recorded by a WITec spectrometer in a Raman shift range of $\omega =$ 260 to 1200 cm^{-1}. Relevant Raman peaks appear at 480 cm^{-1} for a-Si and 521 cm^{-1} for c-Si [217, 219, 220], with an intermediate phase introduced due to phonon confinement at $\omega =$ 500 cm^{-1} [217, 220, 221].

A challenge in Raman measurements of a-Si layers is the background signal originating from the c-Si base. For this reason, measurements in this work were taken on a fused silica substrate. The evaluation procedure is described in detail in [27, 222], where subtraction of the fused silica spectrum followed the approach described in [222]. Crystallinity χ, defined as the ratio of the crystalline part to the total part of the spectrum, is obtained by fitting three Gaussian peaks to the data [27, 217], leading to

$$\chi = \frac{I_{500} + I_{521}}{I_{480} + I_{500} + I_{521}}, \tag{3.13}$$

where $I_{480/500/521}$ represents the respective Gaussian integral at the peak positions. Additionally, attempts have been made to estimate the crystallite size L via the shift of the crystalline peak $\Delta\omega_{521}$ through [217]

$$L = 2\pi\sqrt{\frac{2.24}{\Delta\omega_{521}}}. \tag{3.14}$$

It should be noted that deviations in crystallinity and especially crystallite size determination via Raman measurements, compared to other techniques such as TEM and XRD, have been reported [221, 223]. Therefore, absolute values should be interpreted with caution, while comparing Raman results for similar sample structures remains valid.

3.3. Electrical Properties

In the following sections, various methods to electrically characterize the samples are discussed. Section 3.3.1 begins with the 4PP measurement, a fundamental technique used to determine poly-Si sheet resistance and resistivity. A similar principle is employed in Hall effect measurements, as explained in Section 3.3.2. To assess contact quality, TLM measurements are used and described in Section 3.3.3. Lastly, Section 3.3.4 briefly covers ECV measurements, which are used to characterize electrically active dopant profiles.

3.3.1. Four-Point Probe

Resistivity ρ, the reciprocal of conductivity σ, is an important parameter for characterizing poly-Si layers. It is defined as the proportionality constant between the electric field E and current density J, described by [11]

$$E = \rho J. \tag{3.15}$$

Resistivity is commonly measured using 4PP measurements. In this configuration, a small current (typically $<$ 10 mA) is passed through the two outer probes, while the voltage is measured between the two inner ones. This method is superior to a two-point probe setup, where the voltage drop includes a contact resistance contribution, leading to inaccuracies. Assuming the sample width is significantly smaller than its lateral extension, resistivity is given by the expression

$$\rho = \frac{\pi d}{\ln\left(\frac{\sinh(d/s)}{\sinh(d/2s)}\right)} \frac{U}{I}, \tag{3.16}$$

where s is the probe spacing [224, 225]. For thin layers ($d < s/2$), Equation (3.16) can be approximated as [226]

$$R_{\text{Sheet}} = \frac{\pi}{\ln 2} \frac{U}{I}, \tag{3.17}$$

where the *sheet resistance* R_{Sheet} is introduced. Unlike resistivity, as defined in Equation (3.16), sheet resistance is independent of thickness and is expressed in units of Ω/sq rather than Ωcm.

3.3.2. Hall Effect

Hall effect measurements function similarly to simple four-point probe measurements but differ in the measurement geometry. Instead of four probes in a straight line, the metal pins can be placed arbitrarily on the sample using the *Van-der-Pauw geometry* [227], which

provides an average resistivity of the entire sample. In this work, 2x2 cm^2 fused silica samples are used for Hall measurements, where samples are contacted at each corner (at positions 1-4) as close as possible to the sample's edge to maintain symmetry [228].
This setup allows for measurements with and without a static magnetic field and can also be used to determine the resistivity or sheet resistance. For this, a current I_{21} is applied between two pins, while the voltage V_{34} is measured between the other two pins, yielding a resistance $R_{21,34} = V_{34}/I_{21}$. Afterwards, the polarity of the current is reversed to I_{12}, and V_{43} is measured. This process is repeated for the remaining six pin combinations, resulting in eight resistance values. Half of these values are redundant ($R_{21,34} = R_{12,43}$), allowing for the validation of measurements [229]. Finally, the sheet resistance can be calculated via [27]

$$R_{\text{Sheet}} = f \frac{\pi d}{\ln 2} \left(\frac{R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21}}{4} \right), \tag{3.18}$$

where $f = 1$ is a symmetry factor. Resistivity can be calculated as $\rho_{\text{HE}} = dR_{\text{Sheet}}$. For all measurements, the contact must be ohmic, which was checked via current-voltage curves between all pin combinations before each measurement. Every measurement was performed at least five times and averaged to reduce uncertainty.
During the measurement, a static magnetic field B is applied perpendicular to the sample's surface. For a p-type sample, the Lorentz force drives the majority carriers p (holes) downward, creating an electric field that counteracts the Lorentz force [11]. The magnetic field direction can be varied between positive and negative values. For instance, the Hall voltage $V_{24\text{P}}$ corresponds to a positive magnetic field for I_{13}, whereas $V_{24\text{N}}$ refers to a reversed magnetic field. The measurement principle is similar to that of resistivity. A positive magnetic field is applied while $V_{24\text{P}}$, $V_{42\text{P}}$, $V_{13\text{P}}$, and $V_{31\text{P}}$ are measured. After reversing the magnetic field, the corresponding voltages are recorded as well. This approach enables the calculation of the charge carrier sheet concentration

$$p_{\text{Sheet}} = \frac{IB}{q} \frac{8}{V_{24\text{P}} - V_{24\text{N}} + V_{42\text{P}} - V_{42\text{N}} + V_{13\text{P}} - V_{13\text{N}} + V_{31\text{P}} - V_{31\text{N}}}, \tag{3.19}$$

and the charge carrier concentration $p = p_{\text{Sheet}}/d$. A combination of measurements with and without the magnetic field enables determination of the thickness-independent carrier mobility

$$\mu = \frac{1}{q p_{\text{Sheet}} R_{\text{Sheet}}}. \tag{3.20}$$

Hall measurements can also be performed in a temperature-dependent manner by cooling the sample down to 80K using liquid nitrogen, and gradually heating it in steps of 10K up to 350K. The uncertainty of μ was determined by the standard deviation of five repetitions.

3.3.3. Transfer Length Method

The transfer length method (TLM), sometimes also called transmission line measurement, is used to determine the *contact resistance* R_{C} and *specific contact resistivity* ρ_{C}. An extensive description can be found in [224]. TLM is based on multiple 4PP measurement with increasing metal finger pitches. Typically, two types of TLM structures can be distinguished, as shown in Figure 3.8. The first, depicted in Figure 3.8(a), consists of equidistant fingers similar to those used for solar cell contacts. However, the current flow is disturbed by the intermediate fingers. An often more suitable TLM structure is shown in Figure 3.8(b), where the finger spacing $d_{1\text{-}6}$ gradually increases [230].
The measured total resistance R_{Total} can be divided into contributions from the metal itself R_{Metall}, the contact resistance R_{C}, and the sheet resistance R_{Sheet} via [224]

$$R_{\mathrm{Total}} = 2R_{\mathrm{Metall}} + 2R_{\mathrm{C}} + R_{\mathrm{Sheet}}. \tag{3.21}$$

Due to $R_{\mathrm{Metall}} \ll R_{\mathrm{C}}$, the resistance contribution from the metal can be neglected. The sheet resistance contribution can be determined by

$$R_{\mathrm{Sheet}} = \frac{R_{\mathrm{Sheet}} d_{1\text{-}6}}{Z}, \tag{3.22}$$

where Z is the strip width after disk sawing. Furthermore, the contact resistance R_{C} between the metal finger of length L_{F} and the poly-Si depends on the contact area $A_{\mathrm{C}} = ZL_{\mathrm{F}}$. To eliminate this dependency, the area-independent specific contact resistivity $\rho_{\mathrm{C}} = R_{\mathrm{C}}A_{\mathrm{C}}$, given in units of $\Omega\mathrm{cm}^2$, is often used [224].
To extract ρ_{C}, it must be considered that current flow into the metal finger is not homogeneous across the entire contact area, with current crowding occurring under the fingers, as shown in Figure 3.9(a). The potential distribution $V(x)$ under the metal finger is given by [230]

$$V(x) = \frac{I\sqrt{R_{\mathrm{Sheet}}\rho_{\mathrm{C}}}}{Z} \frac{\cosh\left(\frac{L_{\mathrm{F}}-x}{L_{\mathrm{T}}}\right)}{\sinh\left(\frac{L_{\mathrm{F}}}{L_{\mathrm{T}}}\right)}. \tag{3.23}$$

Here, the transfer length $L_{\mathrm{T}} = \sqrt{\rho_{\mathrm{C}}/R_{\mathrm{Sheet}}}$ is defined, which represents the distance from the contact edge to the point where the potential drops to $\frac{1}{e}$, giving the technique its name. Since the voltage between two contacts is measured at $x = 0$, using Ohm's law yields

$$R_{\mathrm{C}} = \frac{V}{I} = \frac{R_{\mathrm{Sheet}}\rho_{\mathrm{C}}}{Z} \coth\left(\frac{L_{\mathrm{F}}}{L_{\mathrm{T}}}\right) \quad \Rightarrow \rho_{\mathrm{C}} = R_{\mathrm{C}}L_{\mathrm{T}}Z \tanh\left(\frac{L_{\mathrm{F}}}{L_{\mathrm{T}}}\right). \tag{3.24}$$

The transfer length describes how the current is distributed along the finger. For low ρ_{C}, most of the current flows into the contact finger at the edge, while for higher ρ_{C}, this region

becomes wider. To determine these quantities, Equations (3.21) and (3.22) are combined to give

$$R_{\text{Total}} = 2R_{\text{C}} + \frac{R_{\text{Sheet}} d_{1\text{-}6}}{Z}. \tag{3.25}$$

This equation can be solved using a linear fit, as shown in Figure 3.8(c), where the slope provides R_{Sheet}/Z and the y-axis intercept gives $R_{\text{Total}} = 2R_{\text{C}}$. Additionally, extrapolation to $R_{\text{Total}} = 0$ gives $d_0 = -2L_{\text{T}}$. The value of ρ_{C} can be calculated using Equation (3.24).

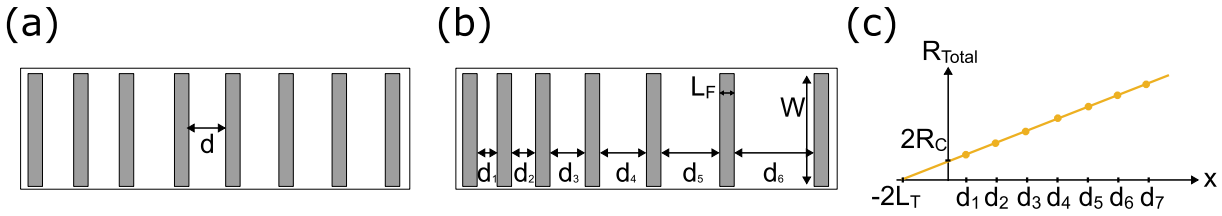

Figure 3.8.: *Schematic of TLM patterns with (a) equidistant and (b) increasing finger pitches. (c) TLM fit procedure to determine key parameters.*

Although this method is well-established, it has some limitations. Inhomogeneous sheet resistances in the poly-Si can lead to deviations in ρ_{C}, particularly under metal contacts for equidistant patterns. While corrections have been introduced, it is recommended to use a TLM pattern with increasing finger pitches whenever possible for more accurate ρ_{C} determination. Another restriction is that the conductive layer (e.g., poly-Si for passivating contacts) must be thin compared to the finger pitch, as Equation (3.24) is valid only in a one-dimensional case. To ensure this condition is met, an insulator can be deposited between poly-Si and the base, such as a thick SiO_x layer. Another option is to use a base material with opposite polarity to the poly-Si, as shown in Figure 3.9(a) for a pn-junction. In the case of a high-low junction with the same polarity for poly-Si and base material, Eideloth and Brendel proposed a correction via a geometry factor, which has proven effective for thick conducting layers, as illustrated in Figure 3.9(b) [231].

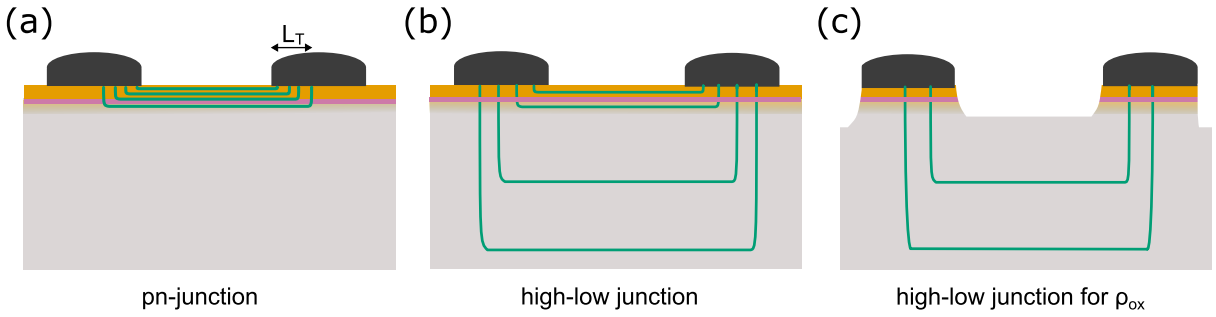

Figure 3.9.: *Current pathways for different TLM measurement geometries of poly-Si/SiO_x structures. (a) For a pn-junction, charge carrier transport occurs only in the poly-Si and in-diffused region. (b) In a high-low junction, current paths can occur in both the poly-Si and the base. (c) To determine the oxide contact resistivity and the transport mechanism, a geometry with removed poly-Si between the fingers is used. Adapted from [17].*

A practical limitation for TLM evaluation is the fit quality, as only up to six measurement points are available for the linear fit using the pv-tools setup. Each fit was evaluated individually and discarded if the fit error exceeded 10%. The uncertainty in contact resistivities was determined by a weighted error across all measurements, and ρ_C was calculated as the geometric mean of all contact resistivities.

T-TLM measurement

For passivating contacts, another resistivity contribution arises from the interfacial oxide. Consequently, ρ_C can be further divided into contributions from the poly-Si and the oxide. One method to determine the oxide contact resistivity is by selectively removing the poly-Si between the contacts, as well as the in-diffused region underneath, shown in Figure 3.9(c). Poly-Si can be selectively removed either by saw dicing or plasma etching. During plasma etching, an Al cover on top ensures selectivity between a-Si and metal fingers, as Al is not removed during the process. A radio frequency plasma is generated by ionizing the process gases SF_6, O_2, and N_2, with reactive ion etching taking place at a pressure of 100 Pa. The etching time determines the thickness of the removed layer.
This sample configuration is used to investigate the charge carrier transport mechanism, according to the theory described in Section 2.2.2. Since tunneling and pinhole transport exhibit different temperature dependencies, the mechanism can be identified via temperature-dependent TLM measurements using a self-made setup. A single TLM structure, as shown in Figure 3.9(c), is cooled to 80K using liquid nitrogen, and TLM measurements are performed between 100–350K in steps of 10K by heating the sample with a temperature control unit. TLM measurements are carried out using a pv-tool setup, and an AutoHotkey script is employed to control the measurements. Evaluation is conducted via the 2D model proposed by Eideloth and Brendel [231].
To determine the transport mechanism, either Equation (2.18) or Equation (2.15) is fitted to the data. For all samples, a fit via the tunneling model is attempted [232]. If the tunneling model does not provide a good match, a pinhole fit is applied. If neither fit works, a combined model is used, where the two transport mechanisms are combined using the parallel circuit equivalence $(\rho_{C,Comb})^{-1} = (\rho_{C,P})^{-1} + (\rho_{C,T})^{-1}$. An overview of the fitting parameters is given in Table A.1. For tunneling-dominated transport, ΔE_S and the oxide thickness d_{ox} are fitted, while the tunneling mass m_T is fixed at $m_T = 0.23\ m_e$ [76, 79]. The resistivity of the in-diffused region for pinhole samples is parametrized according to [233, 234] by varying the dopant concentration of the in-diffused region N_{diff} in discrete steps, from the base doping level up to $1 \cdot 10^{17}$ cm^{-3}. The pinhole radius and density are fitted according to Equation (2.18). Finally, the depth of the in-diffused region w is set to 100 nm, representing

an approximation of the plasma-etched region below the SiO_x/c-Si surface.
Galleni et al. demonstrated that current spreading occurs over the entire etched region [78]. Since most samples experienced a low thermal budget, the etched region typically is larger than the diffusion depth of phosphorus or boron atoms into the c-Si wafer [232]. Furthermore, it has been observed that w does not significantly influence the contact resistivity for small pinhole radii that are expected for short annealing times [79]. Results of T-TLM measurements are presented in Section 5.1.1.
Finally, it should be noted that no error is reported for the fit parameters. This is due to the large number of fit parameters, especially in the combined model. As a result, the fit parameters should be considered approximations and ideally verified using additional methods.

Table 3.1.: *Parameters and their respective ranges used for the T-TLM fitting procedure.*

Parameter	Value range
ΔE_{S}	0.1-500 meV
d_{ox}	1-2 nm
m_{T}	0.23 m_{e}
N_{diff}	$7.5 \cdot 10^{14}$-$1 \cdot 10^{17}$ cm^{-3}
r_{P}	1-10 nm
N_{P}	$1 \cdot 10^{5}$-$1 \cdot 10^{9}$ cm^{-2}
w	100 nm

3.3.4. Electrochemical Capacitance-Voltage Measurement

ECV measurements can be employed to determine the charge carrier concentration in poly-Si using a wafer profiler CV21 from WEP control. This technique provides insight into the active carriers contributing to charge transport and is based on capacitance-voltage measurements. A detailed description is omitted here but can be found in [235]. Depth resolution is achieved by using a conducting liquid as the primary electrode, which contacts the sample acting as the counter-electrode. This liquid gradually etches the poly-Si layer, with measurements taken at defined intervals throughout the process.
A key advantage of ECV measurements is that only electrically active dopants are detected, which may differ from the total doping concentration within the layer. In this work, ECV measurements are primarily utilized to examine dopant in-diffusion through the SiO_x layer into the base, as well as dopant activation within the poly-Si layer itself.
Measurement uncertainties are typically small ($< 5\%$) within the poly-Si layer but increase up to 20% at the base doping level. For clarity, error bars are not shown throughout this work.

4. Influence of Different Thermal Budgets without Metallization

Although many studies have investigated the influence of annealing temperature for long annealing processes [236–241], very limited investigations have been conducted for varying thermal budgets by changing the annealing time [241, 242]. Besides the importance of the thermal budget, it has been suggested in literature that the type of oxide can also significantly impact the passivation for different annealing conditions. Thus, in this chapter the influence of various thermal budgets on symmetrical poly-Si/SiO_x lifetime samples is investigated for non-metallized samples. Section 4.1 explores this by varying the annealing time. Following this, Section 4.2 examines the effect of annealing temperature during short firing processes, which is crucial for implementing the FPC concept.

4.1. Different Annealing Times

The effect of different annealing times is investigated in Section 4.1.1 for PECVD a-Si and in Section 4.1.2 for APCVD a-Si by considering passivation, resistivity, and microstructure.

4.1.1. PECVD a-Si

To assess the impact of varying annealing times, symmetrical samples were prepared using a 0.8 Ωcm Ga-doped base with four different interfacial oxides (Ozone $O_{1.7}$, Piranha $P_{1.5}$, Thermal $T_{1.5}$ and $T_{1.9}$), where the thickness is represented by the index. A 130 nm thick (n) a-Si layer was deposited on both sides. Different annealing conditions were realized, as outlined in Sections 2.4.1 and 2.4.2. All RTP annealing was performed at 870°C, with variations in the time at peak temperature (e.g. R30s, R2min). The thermal budget (TB) was further altered by diffusion furnace annealing at three different temperatures (D820°C, D870°C, and D920°C). The effect of annealing on the microstructure is examined first.

Microstructure

For each oxide-annealing combination, ECV measurements were conducted to determine the depth profile of active phosphorus atoms. Figure 4.1(a) shows exemplary measurements for different oxides after the D920°C process. The extent of in-diffusion depends strongly on the interfacial oxide, with oxide thickness playing the most significant role in limiting diffusion. Thinner oxides exhibit a "kink and tail" profile, similar to diffused emitters, which arises through a change from vacancy mediated diffusion via doubly negative vacancies at high concentrations to interstitially governed diffusion at lower concentrations [243]. In contrast, the $T_{1.9}$ oxide shows minimal in-diffusion.

Two primary mechanisms enable dopants to penetrate into the c-Si base. The first is direct diffusion through pinholes from the poly-Si layer into the c-Si base, which can enhance diffusion locally if the pinhole density is sufficiently high [244]. Krügner et al. demonstrated that pinhole densities below $1 \cdot 10^{10}$ cm^{-2} have no measurable macroscopic impact on doping concentration [244]. This suggests that diffusion through pinholes can become a significant pathway, especially for thinner oxides, where higher pinhole densities are expected. A more detailed discussion on pinhole formation and its effect on charge carrier transport is provided in Section 5.1.

The second mechanism is diffusion through the SiO_x layer itself, where the diffusion coefficient is much lower than in c-Si or poly-Si [245, 246]. This slower diffusion process through an intact oxide layer is generally considered the dominant pathway [76]. However, controlling pinhole formation is crucial, as pinholes can degrade passivation by physically disrupting the interfacial oxide, deteriorating the chemical passivation [98].

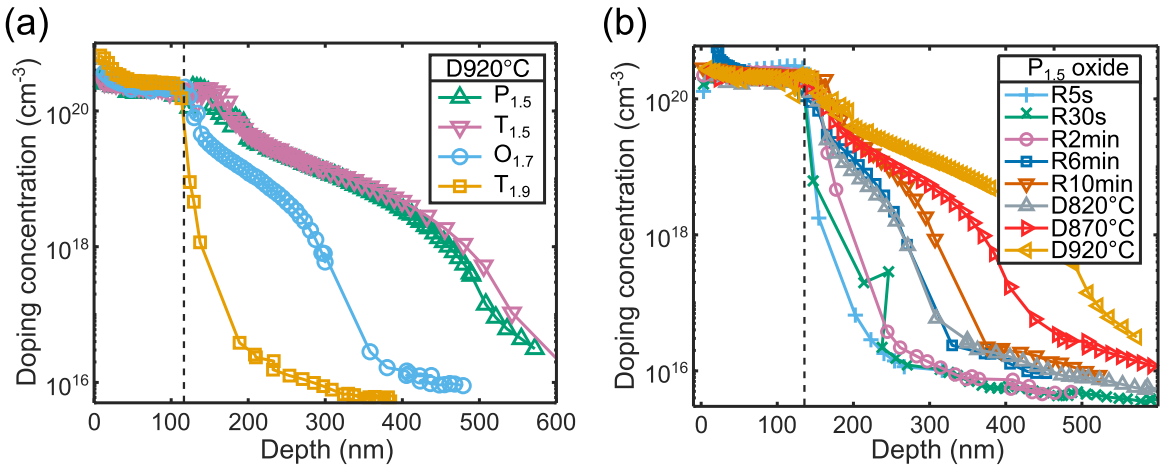

Figure 4.1.: *Active doping concentration determined by ECV measurements for (a) D920°C annealing with four different oxides and (b) different annealing conditions for the $P_{1.5}$ oxide.*

Annealing time also greatly impacts the extent of in-diffusion, as demonstrated in Figure 4.1(b) for the $P_{1.5}$ oxide. Longer annealing times significantly increase the diffusion depth, though the concentration within the poly-Si remains largely unaffected. On the other hand, the annealing temperature has a more pronounced effect on diffusion than total processing time, as is evident by the diffusion furnace processes, which exhibit increased diffusion with higher temperatures despite identical processing times. At the lowest thermal budgets (R5s), in-diffusion is minimal or non-existent, which will be examined in greater detail in Section 4.2.3. Nonetheless, the diffusion profile of active dopants can be precisely controlled by adjusting the annealing-oxide combination.

Resistivity

After evaluating in-diffusion, the properties of poly-Si itself are analyzed. Figure 4.2(a) presents the XRD crystallite size as a function of the thermal budget for the $T_{1.9}$ oxide. No notable differences in crystallite sizes were observed between different oxides, which is expected as it would indicate epitaxial growth during deposition or crystallization. Although PECVD a-Si is fully amorphous in its as-deposited state, even brief annealing times result in increasing crystallite sizes, which continues to increase with an increasing TB.
For long annealing times, crystal growth typically slows down. This is firstly due to the crystallization kinetics of the KJMA-model, as described in Section 2.3.3 [110]. Secondly, after deposition the phosphorus atoms are distributed approximately homogeneously throughout the a-Si layer. During annealing they tend to segregate at grain boundaries, where P atoms can cluster and become electrically inactive, hindering charge carrier transport [247, 248]. During annealing these atoms suppress further growth, for instance through Zener pinning of grain boundaries [249, 250]. However, in the here investigated range of TB no clear slow-down of crystal growth is visible.
Alongside crystallite size, electron mobility of the poly-Si layer in Figure 4.2(a) follows the same trend, increasing significantly with longer annealing times. This is consistent with Equation (2.24), as for larger crystallites the grain boundary density is lower, which leads to less trapping of charge carriers at these boundaries. Moreover, increased dopant in-diffusion effectively thickens the conductive layer, further enhancing mobility. This correlation between mobility, crystallite size, and resistivity will be discussed in more detail in Section 5.2.
Figure 4.2(b) shows the sheet resistance for all oxide-annealing combinations. For clarity, errors are not displayed but are less than 10% for all samples. Since the a-Si was deposited on a Ga base, no charge carrier transport occurs through the pn-junction during 4PP measurements, as there is no forward or reverse bias across the junction. R_{Sheet} decreases with

higher thermal budgets, largely due to an increase in crystallite size, which reduces poly-Si resistivity (Sections 2.3.4 and 5.2). Thinner oxides yield lower resistances due to increased in-diffusion, which creates an effectively thicker conductive layer. The difference between the $T_{1.5}$ and $P_{1.5}$ oxides at lower annealing times indicates a weaker thermal stability for the $T_{1.5}$ oxide, despite similar thickness, which will be explored further in Section 5.1. The last three data points correspond to the D820°C, D870°C, and D920°C annealing steps, respectively. For these processing steps, a more pronounced decrease in resistivity is observed. Similar to the extent of in-diffusion, this further underscores the greater importance of temperature, rather than process duration, for many temperature-dependent processes such as crystallite growth and resistivity changes. As discussed briefly for the definition of the thermal budget in Equation (2.28), the impact of temperature tends to be underestimated in this definition of the thermal budget.

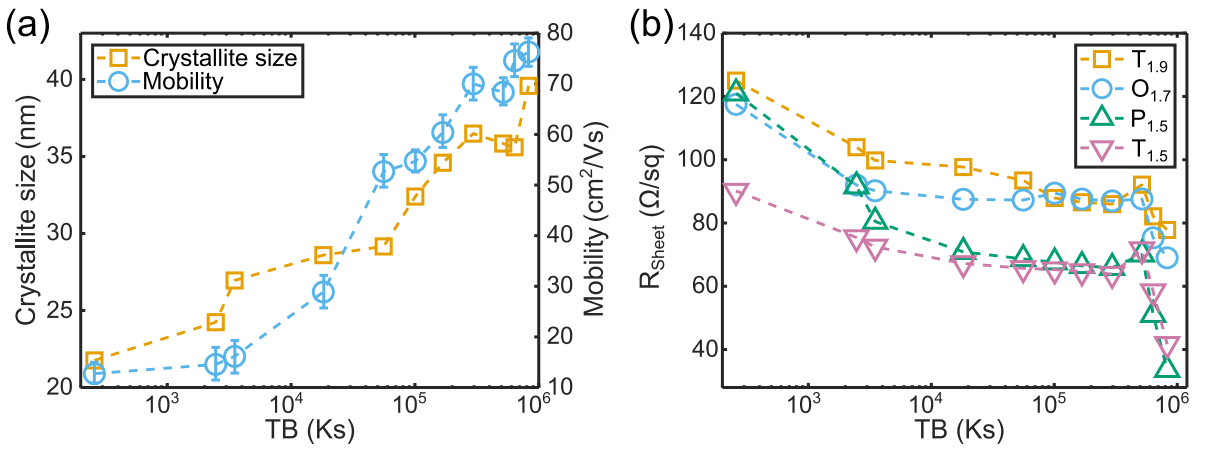

Figure 4.2.: *(a) XRD crystallite size as a function of the thermal budget* TB *for the* $T_{1.9}$ *oxide, along with the measured Hall mobility. (b) Sheet resistance* R_{Sheet} *for different oxides and annealing in dependence of the thermal budget.*

Passivation

In addition to microstructure and resistivity, passivation is a critical factor for evaluating junction quality, particularly for solar cell applications. Figure 4.3(a) illustrates exemplary iV_{OC} values after different processing steps, including annealing, SiN_x deposition, and fast firing (FF) at SPFT $=$ 800°C. Passivation improves with a higher thermal budget following annealing but decreases at even higher thermal budgets due to excessive dopant in-diffusion, which damages the oxide through pinhole formation, increasing defect density at the poly-Si/SiO_x interface, and impairing chemical passivation [251, 252].
After SiN_x deposition, the overall passivation level significantly improves, especially for low thermal budgets where iV_{OC} increases by more than 100 mV. This highlights the importance

of saturating dangling bonds at the poly-Si/SiO_x interface for low TB. Interestingly, passivation decreases after completing hydrogenation via fast firing, a phenomenon frequently reported in many publications [253–256]. Hydrogen diffusion is believed to play a key role in this degradation. Hollemann et al. speculated about the creation of a new hydrogen-induced defect [255], while Polzin et al. identified thermal instability of the SiN_x layer as a possible contributing factor [256], which can be mitigated by lowering the firing temperature.

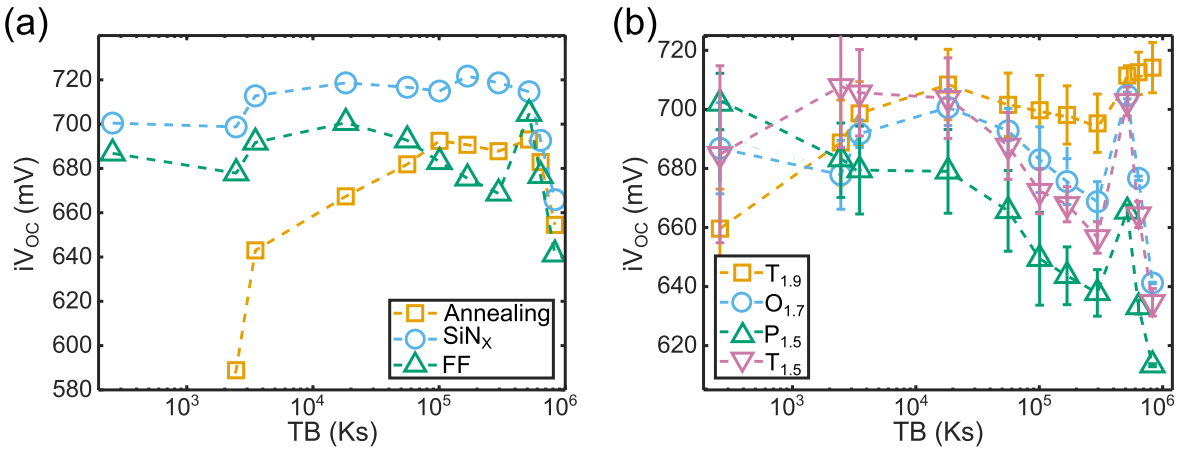

Figure 4.3.: *(a) iV_{OC} values as a function of the thermal budget after annealing, SiN_x deposition, and fast firing (FF) for the $O_{1.7}$ oxide. (b) iV_{OC} values for different oxide-annealing combinations depending on* TB.

Figure 4.3(b) shows the impact of TB on passivation for different oxides after firing. Except for the $P_{1.5}$ oxide, passivation increases with a higher thermal budget, peaking before declining again. While some in-diffusion can enhance surface passivation, the degrading passivation can be attributed to heavy detrimental dopant in-diffusion into the base, which damages the oxide and increases Auger recombination. These observations are underlined by the fact that the D820°C process leads to a higher passivation for all oxides, which drastically decreases for the $O_{1.7}$, $P_{1.5}$, and $T_{1.5}$ oxides at higher annealing temperatures. Only the $T_{1.9}$ oxide maintains a high passivation level for annealing at higher temperatures, even reaching its maximum passivation for the D920°C annealing due to its thermal stability. On the contrary, the iV_{OC} for the $P_{1.5}$ oxide gradually decreases with longer annealing time, pointing to the thermal instability of the oxide. These results indicate that both oxide and annealing conditions must be carefully optimized to achieve high passivation levels.

4.1.2. APCVD a-Si

After investigating PECVD a-Si, the next section focuses on APCVD a-Si to assess whether findings are applicable to a different deposition method and doping type. In this study, 30 nm

APCVD (n) a-Si and 100 nm (p) a-Si was deposited on different oxides and annealed at different annealing times. Additionally, a D920°C annealing reference process was done to realize the high temperature passivating contact (HTPC) route.

Microstructure

First, the doping profile was investigated, as shown in Figure 4.4(a) for APCVD (p) a-Si on the $P_{1.5}$ oxide. A unique characteristic of APCVD a-Si is observed for short annealing times. Unlike PECVD a-Si, dopants are not homogeneously distributed throughout the layer. Instead, a maximum concentration occurs in the middle of the layer immediately after deposition, likely resulting from an uneven distribution of precursor gases in the deposition zone. As illustrated in Figure 2.7, deposition gases are injected onto the sample in the middle of the deposition zone, potentially leading to a higher concentration of B_2H_6. This spatial gradient may cause an increased doping level in the middle of the layer, a phenomenon also observed for APCVD (n) a-Si in ECV measurements and glow discharge optical emission spectroscopy (GD-OES) profiles [17, 257].

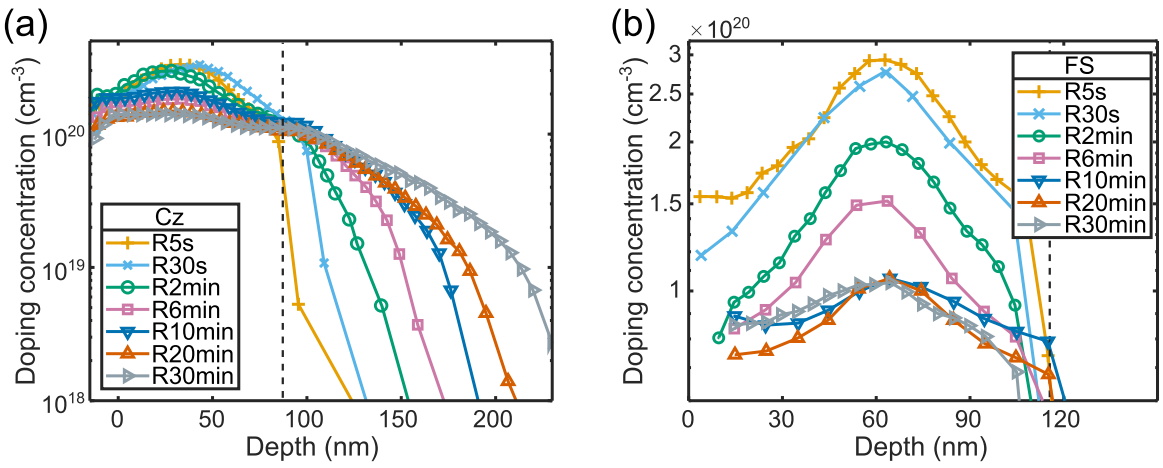

Figure 4.4.: *ECV doping concentration for different annealing times on a (a) Cz wafer with a $P_{1.5}$ oxide and (b) an FS substrate for APCVD (p) a-Si.*

Such a concentration gradient can promote significant diffusion within the poly-Si layer during annealing, as seen in Figure 4.4(a) for the $P_{1.5}$ oxide on a Cz base and in Figure 4.4(b) for (p) a-Si on an FS base. The doping peak nearly disappears after R6min annealing with the $P_{1.5}$ oxide. Similar to PECVD (n) a-Si, longer annealing results in more in-diffusion into the base. However, unlike P diffusion, which occurs mainly interstitially, boron predominately diffuses substitutionally or via pairing with vacancies [258]. Consequently, no "kink and tail" profile is observed for (p) a-Si, and a more shallow profile is expected since substitutional diffusion typically is slower than interstitial diffusion [11], supported by

a typically lower activation energy for boron diffusion compared to phosphorus [129]. In literature, excessive in-diffusion has been reported for boron-doped a-Si during annealing, attributed to boron atoms penetrating the oxide [17, 98]. Therefore, dopant pile-up at the poly-Si/SiO_x interface is less prevalent with boron doping compared to phosphorus, as B atoms tend to segregate homogeneously into the SiO_x, enhancing charge carrier transport [258]. This effect can counteract the slower diffusion of boron compared to phosphorus in silicon itself. However, as one can see for the samples deposited on the FS substrate with the chemical form SiO_2, this glass layer still presents a meaningful diffusion barrier. The maximum of the doping profile in the poly-Si layer is still visible even after 30 minutes annealing, which is not the case for samples on a thin oxide. However, there is still diffusion within the poly-Si layer and in-diffusion into the FS base, where boron becomes electrically inactive. This is discussed in more detail in Section 5.2.

Resistivity

Similar to PECVD (n) a-Si, APCVD (p) poly-Si also exhibits changes in crystallite size during annealing, shown in Figure 4.5(a). The crystallite sizes range from approximately 30 nm to 60 nm, which is larger than those of PECVD a-Si with about 20-40 nm. Despite phosphorus doping generally promoting faster crystal growth than boron doping due to a reported larger nucleation rate, APCVD (p) a-Si exhibits larger crystallites here. This difference can mainly be attributed to the higher deposition temperature of $\approx 700^{\circ}$C, which induces partial crystallization during deposition and formation of cuboidal crystallites, as confirmed by HF-SEM measurements (Section 3.2.2). On the other hand, HF-SEM measurements for PECVD (n) a-Si revealed a more disordered structure.

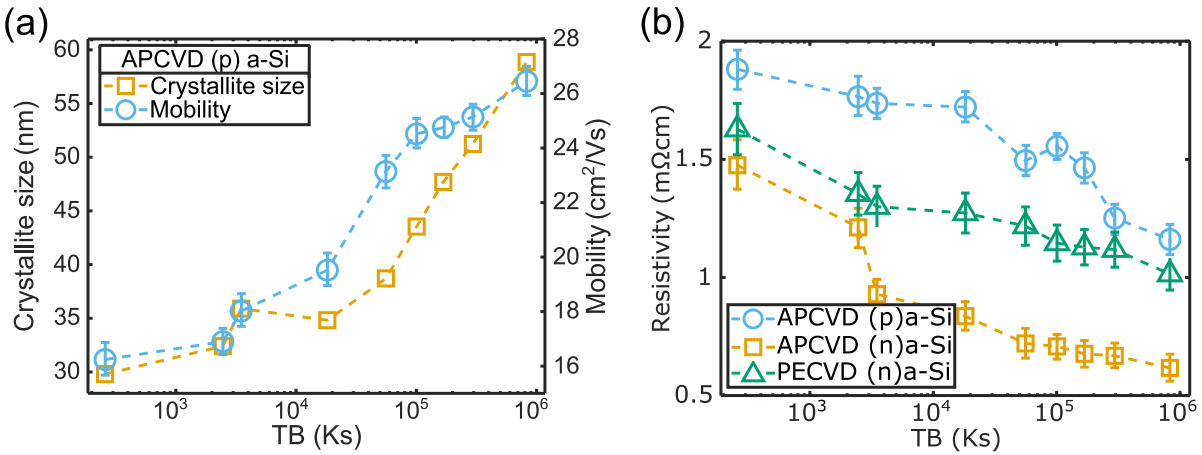

Figure 4.5.: *(a) XRD crystallite size and Hall mobility for APCVD (p) a-Si as function of the thermal budget. (b) 4PP resistivity for APCVD (n) and (p) a-Si, as well as PECVD (n) a-Si layers.*

Hall mobility measurements for APCVD (p) a-Si follow a similar trend to those of PECVD (n) a-Si. However, APCVD (p) a-Si exhibits a smaller mobility range of about 16-26 cm^2/Vs, compared to 10-60 cm^2/Vs for PECVD (n) a-Si. Despite larger crystallite sizes, the lower mobility for (p) a-Si may be attributed to the higher effective mass of holes compared to electrons and more complex band structure in the valence band [259], leading to increased phonon scattering [233, 234, 260]. Additionally, the possible formation of a boron-rich layer during extended annealing might negatively impact charge carrier transport and reduce the mobility [169]. This issue can be mitigated by minimizing the thermal budget, for example through the FPC route. Interestingly, for short annealing times, the mobility of APCVD (p) a-Si is higher than that of PECVD (n) a-Si, which may be due to the larger crystallite sizes [261].
Figure 4.5(b) shows the poly-Si resistivity of APCVD (p) and (n) a-Si, measured on a $T_{1.9}$ oxide with opposite base polarities, along with PECVD (n) a-Si for comparison. ρ_{Poly} decreases with a higher thermal budget for all samples. Consistent with reports in literature, phosphorus doping shows a lower resistivity than boron doped a-Si. This is presumably the result of higher mobility and larger crystallite size, decreasing the resistivity according to Equation (2.23). The resistivity of APCVD (n) a-Si is lower than that of PECVD (n) a-Si, which is consistent with the larger crystallite sizes typically reported for this deposition technique.

Passivation

Figure 4.6 shows the passivation quality for APCVD (n) a-Si in terms of iV_{OC} values for different annealing times after firing with a SiN_x layer at 750°C SPFT on various oxides. The dependence on the thermal budget is similar to that of PECVD a-Si. For the $P_{1.5}$ oxide, a longer annealing significantly decreases passivation, while for $O_{1.7}$ and $T_{1.5}$ oxides a maximum in the range of R30s up to R6min can be found. The $T_{1.9}$ oxide is additionally displayed for (p) a-Si, where for both doping types the passivation increases for longer annealing time with a rather low passivation level for (p) a-Si at low thermal budgets.
The overall passivation level for APCVD a-Si, with values up to 736 mV, is higher than that of PECVD layers, partly due to the use of a 5 Ωcm (n) c-Si base, which exhibits higher base lifetimes than the Ga base used for the deposition of PECVD (n) a-Si and can offset the passivation level. This is supported by similar minimum $J_{0,\text{Pass}}$ values of $\approx$ 10 fA/cm^2 for APCVD and PECVD (n) a-Si. Another factor is the lower firing temperature for APCVD a-Si. As discussed in Section 4.1.1, this can help to prevent defect formation during firing.
In conclusion, a suitable combination of the interfacial oxide and annealing conditions should be selected, regardless of deposition method or doping type. Furthermore, one

can see that even at a low TB a high passivation quality can be achieved. As indicated for PECVD a-Si in Figure 4.3(a), the hydrogenation step is of utmost importance for the passivation, which is especially true with a low TB. One key parameter for hydrogen release into the layer is the peak firing temperature, which will be explored in the next section.

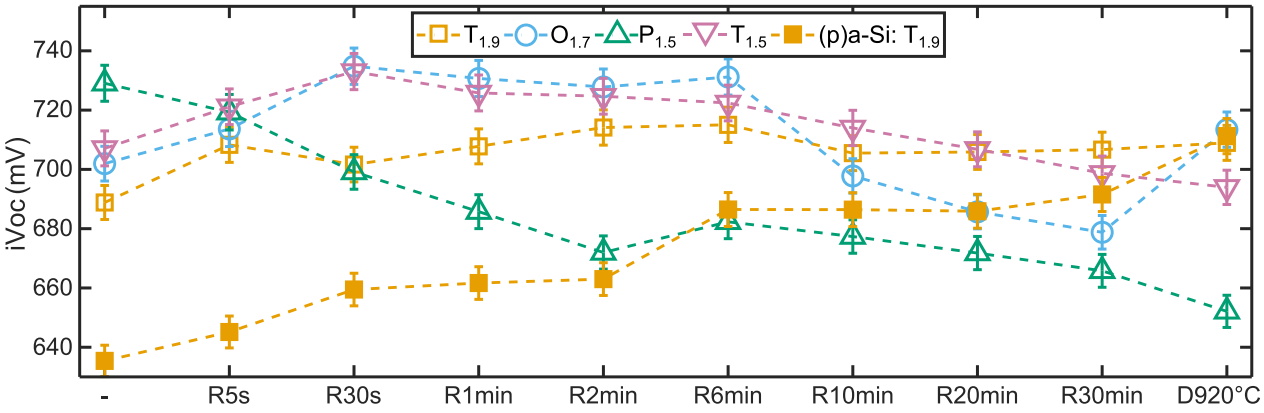

Figure 4.6.: *iV_{OC} values for APCVD (n) a-Si for different oxide-annealing combinations, with (p)a-Si on a $T_{1.9}$ oxide as comparison. All samples are coated with a SiN_x layer and fired at 750°C SPFT.*

4.2. Different Fast Firing Temperatures

For implementation into solar cells and a lean process flow it is beneficial to omit the annealing step before SiN_x deposition. The only way to then vary the thermal budget is by changing the firing profile parameters, specifically the peak firing temperature, which is the focus of this section.

When trying to implement the FPC approach for PECVD (n) a-Si layers, one key issue occurs. Despite varying the oxides and firing temperatures between 750°C and 900°C, the passivation level remains low after SiN_x deposition and firing. For the lowest firing temperature used (750°C), highest iV_{OC} values of up to 650 mV can be found, whereas the passivation for the thinner oxides is slightly higher ($\approx$ 20-30 mV) than that of the thicker $T_{1.9}$ oxide. However, as the firing temperature increased beyond 800°C, iV_{OC} values decrease down to approximately 500 mV. This is due to formation of blisters, as can be seen in optical microscope images for the $P_{1.5}$ and $T_{1.9}$ oxides in Figure 4.7.

These blisters form due to the effusion of hydrogen out of the a-Si layer at temperatures above 300°C [102, 262, 263]. At these temperatures, hydrogen bonds rupture and form molecular hydrogen, which escapes from the layer [8]. During the rapid heat-up, hydrogen accumulates in the layer and suddenly lifts off the substrate, thereby negatively affecting passivation [8, 68]. Thus, blisters can be mitigated by reducing hydrogen content before firing. One way to achieve this is through annealing before SiN_x deposition. As shown in

Figures 4.7(a) and 4.7(d), the number of blisters is significantly reduced after a R5s anneal compared to no prior thermal treatment and firing at 850°C (Figures 4.7(b) and 4.7(e)). Additionally, thinner oxides are less prone to blistering, as exemplified by comparing the $P_{1.5}$ and $T_{1.9}$ oxides. This is consistent with literature reports and may be attributed to thicker SiO_x layers functioning as hydrogen diffusion barriers into the underlying Cz base, thereby increasing the extent of blistering. The correlation between hydrogen in-diffusion and blister formation is further supported by the reduced blistering observed at a lower firing temperature of 750°C, corresponding to less and slower hydrogen in-diffusion during firing (Figures 4.7(c) and 4.7(f)).

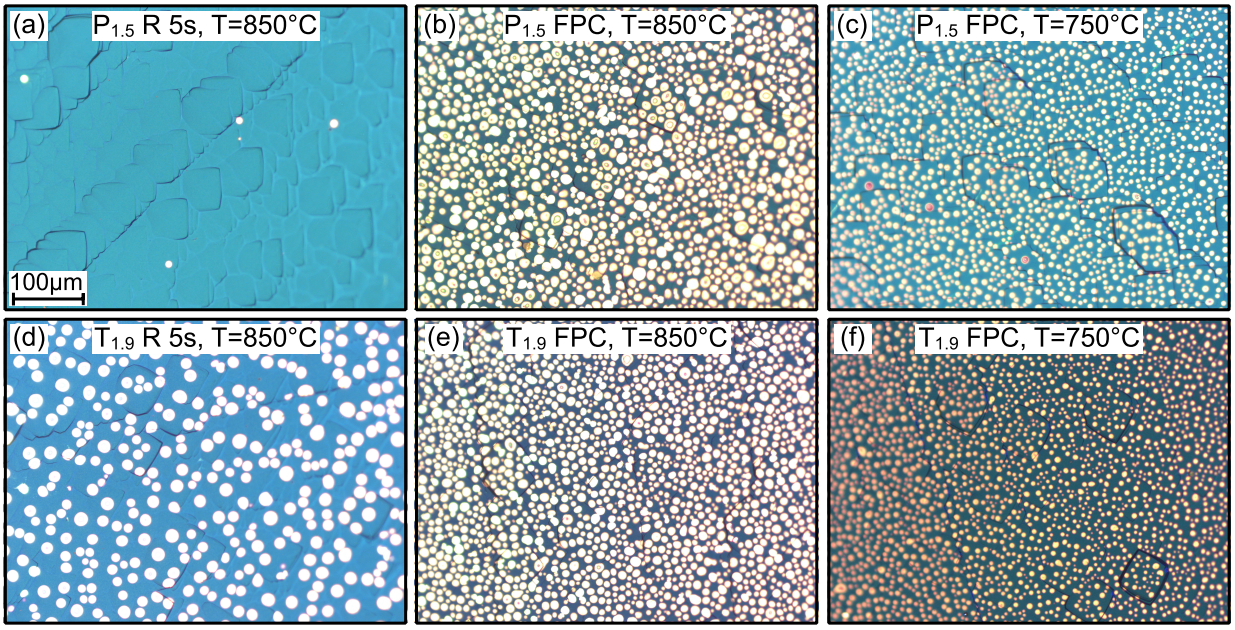

Figure 4.7.: *Optical microscope images for PECVD (n) a-Si after SiN_x deposition and fast firing for (a)-(c) $P_{1.5}$ oxide and (d)-(f) $T_{1.9}$ oxide.*

Another strategy to reduce blisters is the strengthening of hydrogen bonds, for instance by adding carbon atoms to the amorphous network, which was attempted by Ingenito et al. [8, 68]. However, an additional short annealing step before SiN_x deposition still was necessary to prevent blistering.

Consequently, due to the lower hydrogen content through deposition at higher temperatures, APCVD a-Si appears to be a more promising candidate for implementing the FPC concept. In Figure 4.6, APCVD (p) a-Si showed relatively low passivation levels which has potential to be improved upon. Therefore, Section 4.2.1 investigates the impact of different firing temperatures with varying a-Si doping, while Section 4.2.2 addresses the effect of a-Si layer thickness. Finally, Section 4.2.3 discusses the influence of different interfacial oxides onto passivation.

4.2.1. a-Si Doping

This section explores the effect of varying fast firing temperatures on different a-Si doping levels. Symmetrical 80 nm thick APCVD (p) a-Si layers were deposited on a $T_{1.9}$ oxide on top of an (n) c-Si base. The optimal doping concentration for (p) a-Si has been extensively discussed in the literature, showing significant impacts on conductivity and the ability to form a reliable contact with the layer [161, 163, 178]. Two different doping concentrations were achieved for (p) a-Si by varying the B_2H_6 flow during deposition, referred to as "low" and "high" doping. GD-OES profiles, available in the Appendix A.1, indicate a sevenfold difference in relative intensity, corresponding to a maximum doping concentration of $2{\cdot}10^{21}$ cm^{-3}, according to ECV profiles. For both doping levels, a similar dopant distribution with a peak in the middle of the layer was observed. These results are compared to a 100 nm thick APCVD (n) a-Si layer, processed in the course of a master's thesis [257], where the author was responsible for data collection, analysis, and manuscript writing. Additionally, a 130 nm thick PECVD (n) a-Si layer is used to examine the impact of the deposition method on crystal structure.

Microstructure

XRD measurements taken after fast firing and SiN_x removal in a 10% HF solution are shown in Figure 4.8(a). The crystallite size increases with higher SPFT for all layers, though doping affects this behavior. Similar to the last section, P doping leads to larger crystallites than B doped a-Si. In the case of lowly doped (p) a-Si a saturation occurs at SPFTs above 900°C, reaching $\approx$ 35 nm. For higher doped (p) a-Si and (n) a-Si the crystallites grow further, even at higher firing temperatures.

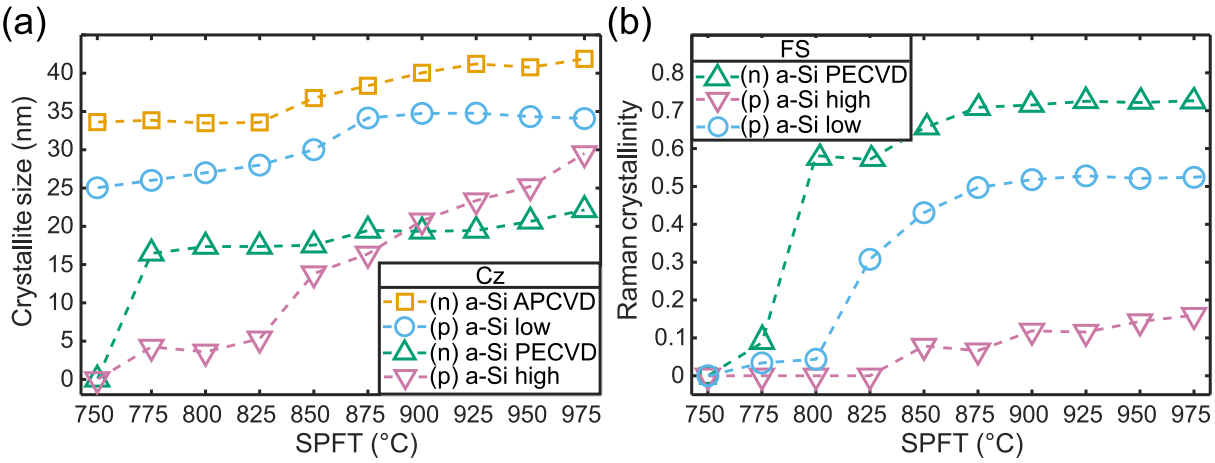

Figure 4.8.: *(a) Results of XRD measurements on Cz substrate for APCVD (n) a-Si, lowly and highly doped APCVD (p) a-Si, as well as PECVD (n) a-Si for different fast firing temperatures [105]. (b) Raman crystallinity on fused silica substrates.*

One significant aspect is the crystallite size in its as-deposited state or at the lowest firing temperature (750°C). While for lowly doped (p) a-Si and APCVD (n) a-Si crystallite sizes are $\approx$ 25 nm and $\approx$ 30 nm, respectively, PECVD (n) a-Si and highly doped (p) a-Si remain completely amorphous at 750°C. For PECVD (n) a-Si, this aligns with expectations based on the literature due to its lower deposition temperature [264]. In the case of highly doped (p) a-Si, crystal growth is even further inhibited due to the formation of boron clusters and pinning at grain boundaries, resulting in smaller crystallites compared to lower doped (p) a-Si. Interestingly, between 750°C and 800°C, the crystallite size increases rapidly for the previously amorphous network. The seemingly enhanced growth rate compared to APCVD (n) a-Si and APCVD lowly doped (p) a-Si may be explained by a larger nucleation rate of the crystalline phase. Due to the high firing temperature, the crystallites can grow more before growth becomes self-limiting or Zener-pinning effects dominate.
XRD results are supported by Raman crystallinity measurements on FS substrates in Figure 4.8(b). Crystallinity follows the same trend as crystallite size, with a sudden increase in crystallinity occurring around 800°C, pointing toward an activation energy for crystallization. The crystallization is slightly delayed compared to XRD measurements, which may result from lower firing temperatures for layers on FS substrates compared to Cz bases (Section 2.4.3). A similar sudden increase in crystallinity has also been observed for SiC_x layers in a similar temperature range [68]. It should be noted that the different base material can also impact the deposition itself. Consequently, APCVD with lowly doped (p) a-Si is completely amorphous after firing at SPFT of 750°C on FS substrates, while already showing relatively large crystallites for XRD measurements on Cz substrates.
Using Raman measurements to determine crystallite sizes according to Equation (3.14) led to significantly smaller crystallite sizes (not shown here). Discrepancies arise because the Raman shift equation does not account for mechanisms like strain, which can produce an additional offset of the peak shift. Strain determined from XRD results shows minimal variation with temperature (Appendix A.1). However, strain values differ significantly between deposition methods. For PECVD a-Si, an average strain value of 0.056(5)% is found for all annealing conditions, while for APCVD a-Si strain values of 0.113(8)% for (n) a-Si, 0.147(9)% for lowly doped (p) a-Si, and 0.234(17)% for highly doped (p) a-Si are determined. These values are consistent with reported strain levels for LPCVD and PECVD poly-Si layers [265]. This indicates that strain is most and foremost dependent on the deposition technique and increases with higher disorder corresponding to a higher doping level but is not influenced significantly by the thermal budget. While the crystallite size is impacted substantially through different firing temperatures, no measurable in-diffusion was detected via ECV for samples with the $T_{1.9}$ oxide. In-diffusion for varying interfacial oxides is briefly discussed in Section 4.2.3.

Resistivity

The resistivity of poly-Si layers ρ_{Poly} after SiN_x removal for APCVD (n) and (p) a-Si is shown in Figure 4.9(a) for different firing temperatures. Across all layers, ρ_{Poly} decreases as the firing temperature increases. A notable difference is observed between the highly doped and lowly doped (p) a-Si layers. Typically, higher doping levels are expected to increase conductivity [233, 234]. However, in this case the highly doped (p) a-Si exhibits resistivity values one order of magnitude higher than the lower doped (p) a-Si.
This deviation can be partly explained by the smaller crystallite sizes in highly doped (p) a-Si, where charge carriers are more likely to be trapped at grain boundaries. According to the relationship described in Section 2.3.4, there should be an inverse proportionality between crystallite size and resistivity. However, the high boron concentration, which exceeds the solubility limit in poly-Si [266], may lead to the formation of large, electrically inactive boron clusters, impeding charge carrier transport [261]. During subsequent (partial) crystallization the solubility limit is presumably decreased, likely promoting dopant trapping and segregation in interstitial defects, further reducing dopant activation in the poly-Si layer [261, 267]. The drop in resistivity from over 200 mΩcm at 800°C down to $\approx$ 10 mΩcm at 975°C correlates with an increase in crystallite size from $\approx$ 3 nm to $\approx$ 30 nm. These high resistivities, corresponding to a minimum sheet resistance of 1250 Ω/sq, make highly doped (p) a-Si layers less ideal for passivating contacts.
For lowly doped (p) a-Si and (n) a-Si layers, ρ_{Poly} decreases also significantly with higher firing temperatures. In the case of (p) a-Si, resistivity drops from $\approx$ 10 mΩcm to $\approx$ 3 mΩcm (375 Ω/sq) at 975°C. For (n) a-Si, the resistivity decreases less, starting at $\approx$ 5 mΩcm and falling below 3 mΩcm. Both layers show a substantial decrease in resistivity up to a firing temperature of 900°C, after which the decline slows down. This behavior aligns with the crystallite size and crystallinity trends discussed earlier, indicating that both mobility and resistivity are influenced by the crystallite size as well in this temperature range. The relationship between resistivity and crystallite size will be explored in-depth in Section 5.2.

Passivation

The impact of firing temperature on passivation is shown in Figure 4.9(b) through iV_{OC} values for different doping. Different temperature dependencies are observed for each sample type. For highly doped (p) a-Si, passivation quality gradually increases from about 600 mV at 800°C to a maximum of around 680 mV at the highest firing temperature. In contrast, lowly doped (p) a-Si starts at a higher iV_{OC} of $\approx$ 650 mV and reaches a maximum of 712(8) mV at 900°C. Further increasing the firing temperature leads to a sharp decline in

passivation, which can be attributed to excessive hydrogen release, causing blistering in the SiN_x layer.

For phosphorus-doped a-Si, passivation behaves differently, with a maximum $iV_{OC} \approx 700$ mV observed between 800°C and 850°C. At higher firing temperatures, passivation decreases due to the formation of blisters, already visible starting at 875°C. This suggests that (p) a-Si is less susceptible to blistering at higher firing temperatures compared to (n) a-Si, allowing for higher firing temperatures that increase crystallization and conductivity. One possible explanation is a higher defect density in (p) a-Si, which can act as a sink for hydrogen atoms, particularly in higher doped (p) a-Si. This is consistent with findings by Kang et al., who also reported increased degradation at higher firing temperatures for (n) a-Si compared to (p) a-Si, likely due to the lower hydrogen diffusivity in (p) a-Si [253, 254].

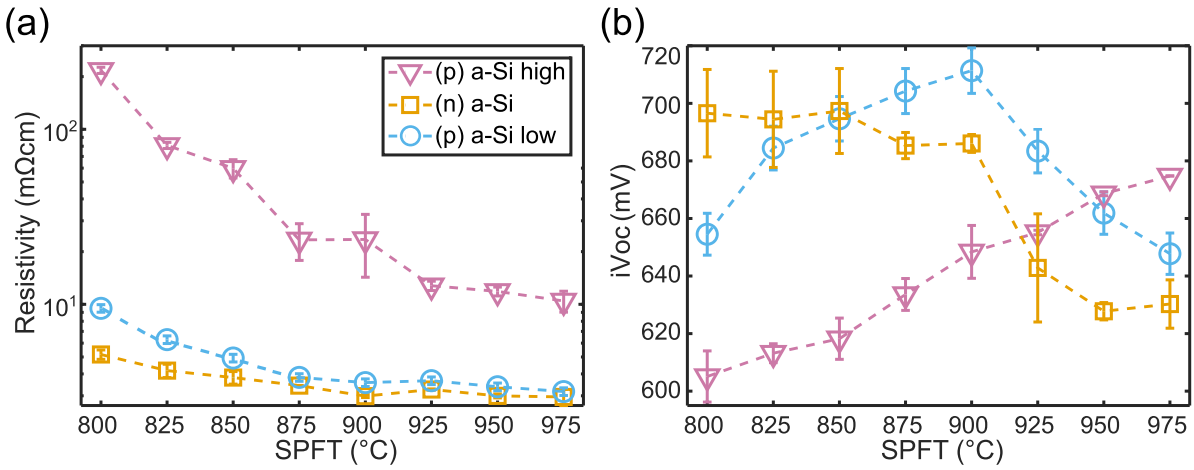

Figure 4.9.: *(a) Resistivity after SiN_x removal and (b) iV_{OC} values after firing for differently doped APCVD a-Si layers [105, 257].*

It is important to note that firing without SiN_x deposition does not significantly improve passivation, where iV_{OC} values remain below 600 mV. Hydrogenation is critical for achieving high passivation levels, as previously demonstrated by Ingenito et al. [8, 134]. These results suggest that a low thermal budget can be sufficient to achieve high passivation levels, although (n) a-Si is not easily compatible with high firing temperatures due to a decrease in passivation quality. In contrast, (p) a-Si is better suited for implementation into the FPC concept, as it can undergo higher firing temperatures, which enhances crystallization and conductivity. Furthermore, (p) a-Si is promising for integration into solar cell devices, where it has been difficult to achieve good contact quality with the HTPC approach. Thus, the subsequent sections focus primarily on (p) a-Si.

4.2.2. a-Si Thickness

While the results for (p) a-Si are promising, there is still room for improvement, particularly in reducing sheet resistances. This is especially important when trying to contact the layers via screen-printing. Thicker a-Si layers have been shown to reduce contact resistivity (ρ_C) and saturation current density ($J_{0,Met}$) values for both boron- and phosphorus-doped APCVD and PECVD layers [17, 160, 161, 163]. As outlined in Section 2.3.1, the a-Si thickness was varied through multiple drive-throughs (1-5DT), each with a thickness of 60 nm. Additionally, the belt speed was varied to achieve a-Si thicknesses of 40, 80, 120, and 330 nm for highly doped (p) a-Si. All layers were deposited on a $T_{1.9}$ oxide, followed by a 75 nm thick SiN_x deposition and firing at different set peak temperatures. Results of the belt speed variation have been published in [105], but XRD measurements were repeated at an incidence angle of 5° instead of 1°. The author was responsible for data collection, analysis, and writing.

Microstructure

The effect of multiple drive-throughs on the doping profile is shown in Figure 4.10(a) for both FPC and HTPC (D920°C) annealing. A similar distribution of active dopants within one drive-through as in Section 4.1.2 is observed for multiple DT, reduced for HTPC due to dopant in-diffusion. For the two lowest firing temperatures, no ECV profile could be recorded for the 1DT and 2DT samples because of a high contact resistivity to the a-Si, pointing towards low dopant activation. However, this is not the case for 3, 4, and 5DT, where the ECV profiles are mostly identical at lower temperatures, as illustrated in Figure 4.10(a). This suggests that multiple drive-throughs can already promote dopant activation during the deposition process.

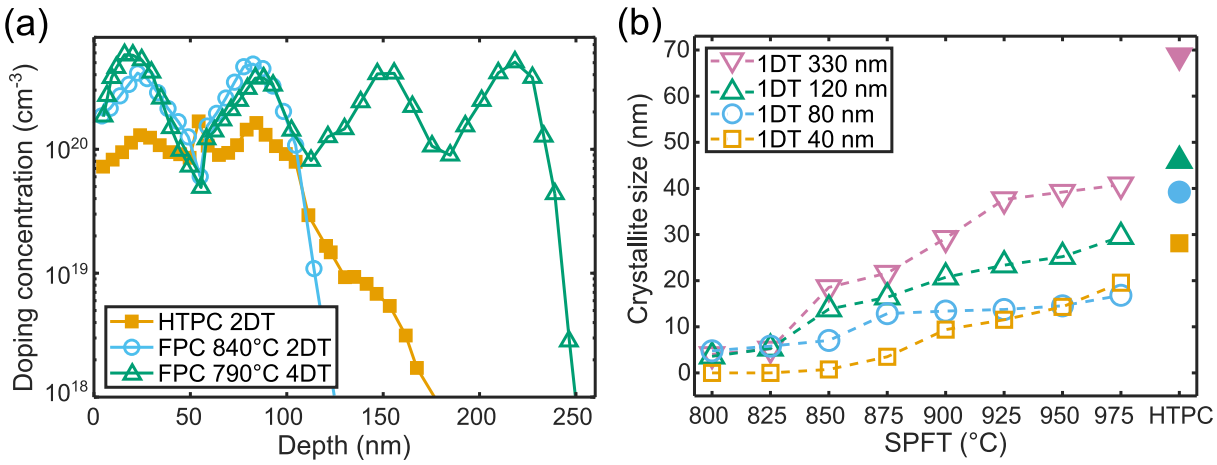

Figure 4.10.: *(a) ECV measurements of a 2DT (p) a-Si layer after firing at 840°C and D920°C annealing, as well as a 4DT layer fired at 790°C. (b) Crystallite sizes for different a-Si thicknesses and firing temperatures for highly doped (p) a-Si.*

In-between those DT a difference between HTPC and FPC is visible in Figure 4.10(a). In the case of FPC, the doping concentration continues to decrease due to the formation of a native interlayer oxide $SiO_{x,inter}$ at 700°C outside of the deposition zone in ambient conditions. In contrast, the HTPC layer exhibits a distinct increase in dopant concentration in the middle of the layer. During annealing, boron diffuses toward the interlayer oxide, creating a concentration peak at the oxide interface. This profile is typical for multiple drive-throughs in both (p) and (n) a-Si [17].
Figure 4.10(b) shows crystallite sizes for different highly doped (p) a-Si thicknesses achieved with 1DT. As expected, the crystallite size increases with higher firing temperatures, while HTPC crystallization produces even larger crystallites. Additionally, thicker layers result in larger crystallites, as crystal growth is inhibited and self-limiting for thinner a-Si layers by the a-Si thickness. In the case of multiple drive-throughs, only a small impact on crystallite size has been found in HF-SEM images in Figure 3.7 for crytallized APCVD (n) a-Si layers. This most likely also applies for FPC (p) a-Si samples, where no meaningful differences in XRD crystallite sizes due to multiple drive-throughs were observed. However, particularly at lower firing temperatures an increasing crystallinity may be induced through several drive-throughs, similar to low temperature firing in Figure 4.8(b).

Resistivity

A key goal is to further decrease the sheet resistance of the layers. Thus, in Figure 4.11 R_{Sheet} values are shown for different thicknesses accomplished by 1DT for highly doped (p) a-Si, as well as multiple DT for lowly doped (p) a-Si.
While the overall resistances shown in Figure 4.11(a) are relatively high, useful conclusions can still be drawn. Firstly, R_{Sheet} decreases across the temperature range for all thicknesses, with a few outliers. Secondly, thicker layers show lower sheet resistance, which is expected due to the larger cross-sectional area for charge carrier transport. When normalized for layer thickness, the resistivity ranges between approximately 200 and 10 mΩcm for all but the thickest a-Si layer, where R_{Sheet} is between 250 and 70 Ω/sq, corresponding to resistivities between 7 and 1.5 mΩcm. This deviation for the thick layer points towards different a-Si properties immediately after deposition due to the significantly lower belt speed leading to a more ordered structure and presumably easier dopant incorporation into the Si network. However, the total amount of doping is not changed according to GD-OES measurements (Appendix A.1). Overall, varying a-Si thickness through belt speed does not drastically change the material properties, but increasing thickness helps to reduce R_{Sheet}. Layers deposited with slower belt speeds may exhibit different characteristics, which is not explored further due to the impracticality of a long deposition process.

The effect of multiple DT, each with a thickness ob about 60 nm, on R_{Sheet} is shown in Figure 4.11(b). Sheet resistances decrease at higher firing temperatures, although the extent varies depending on the number of drive-throughs. At lower temperatures, the resistance is higher for samples with fewer DT, which corresponds to thinner layers. However, R_{Sheet} decreases significantly for higher firing temperatures, from about 10000 Ω/sq down to 240 Ω/sq at the highest firing temperature. In contrast, the thickest layer only shows a reduction from 120 Ω/sq at 790°C to 80 Ω/sq at 915°C, resulting in a lower R_{Sheet} compared to thinner layers.

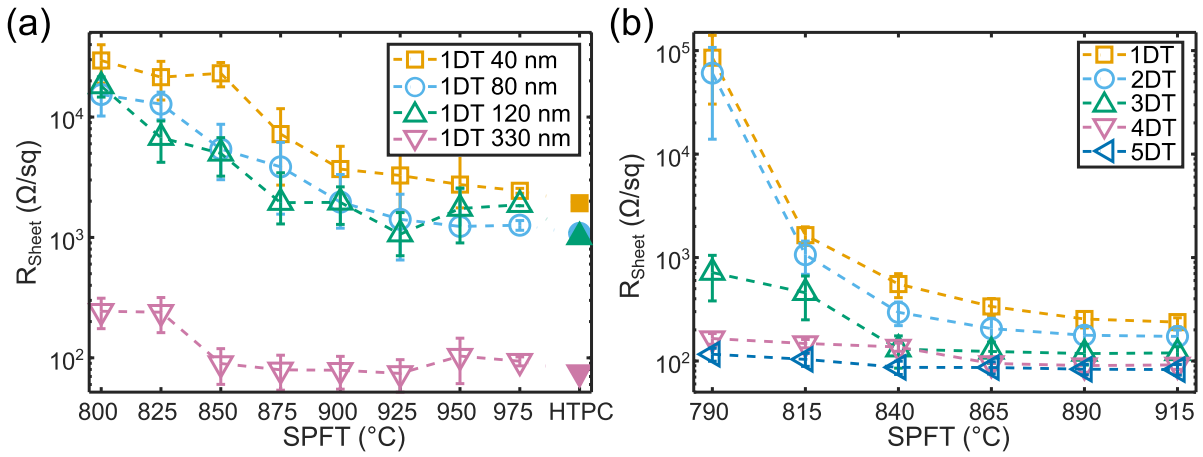

Figure 4.11.: *Sheet resistances R_{Sheet} for different thicknesses accomplished with (a) 1DT for high doping [105] and (b) 1-5 DT in the case of low doping in dependence of the fast firing temperature. In (a) and (b) different firing profiles were used, as (a) was processed for 5x5 cm^2 samples and (b) with 15.6x15.6 cm^2 size wafers.*

Several factors contribute to these observations. Firstly, the lower sheet resistance in thicker layers can be attributed to the larger cross-sectional area for charge transport, similar to variations with 1DT in Figure 4.11(a). However, unlike the thickness variation for 1DT, the normalized resistivity increases slightly with more drive-throughs. For instance, at 915°C the resistivity increases from ≈ 1.9 mΩcm at 1DT to ≈ 3.3 mΩcm at 5DT when considering the total thickness of all drive-throughs combined. This is because the native interlayer oxide formed in-between drive-throughs introduces an additional resistivity contribution. As a result, the resistivity of the poly-Si material cannot be accurately compared by simply multiplying the measured sheet resistance with a-Si thickness. Secondly, the differences at lower firing temperatures are likely related to dopant activation and possibly an increasing crystallinity. This was suspected from ECV measurements, as multiple DT increase the thermal budget during deposition. When the firing temperature rises, resistivity decreases further due to a combination of dopant activation and crystallite growth.

Passivation

Figure 4.12 shows iV_{OC} values for different thicknesses in dependence of the SPFT. For the highly doped 1DT samples in Figure 4.12(a), several observations can be made. A clear thickness dependence is visible with higher passivation for thicker a-Si layers. This is likely because hydrogen diffuses faster to the poly-Si/SiO_x interface in thinner layers. However, the impact of a-Si thickness is reduced at higher firing temperatures. If hydrogen diffusion speed is in fact the passivation-limiting factor at lower temperatures, this could further explain these thickness and temperature dependencies. For a high thermal budget (HTPC), hydrogenation is not as crucial. Consequently, the samples show a diminished thickness dependence with overall higher iV_{OC} values compared to the FPC samples. Another contributing factor to the thickness dependence may be that thicker layers result in a slightly lower measured temperature on the wafer, as was seen in Figure 2.10. A lower temperature could correspond to reduced hydrogen content at the poly-Si/SiO_x interface due to the temperature dependence for hydrogen diffusion out of the SiN_x layer.
The firing temperature dependence is also very clear, with increased iV_{OC} values at higher temperatures for all but the 1DT 40 nm sample, which reaches a maximum iV_{OC} of 708 mV at 900°C. At higher temperatures, passivation decreases for the thinnest layer due to blistering from excess hydrogen in-diffusion into the poly-Si. For thicker a-Si films, no blisters are observed, allowing passivation to improve further at higher firing temperatures.

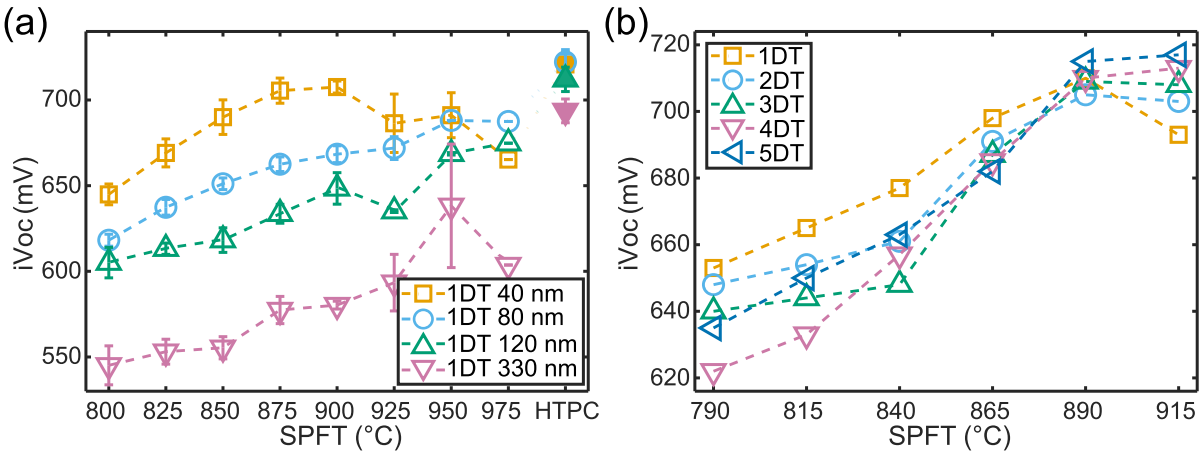

Figure 4.12.: *iV_{OC} values for different (p) a-Si thicknesses for (a) 1DT with highly doped (p) a-Si [105] and (b) 1-5DT with lowly doped (p) a-Si.*

For lowly doped (p) a-Si with multiple DT, the same trends hold. As shown in Figure 4.12(b), higher firing temperatures result in better passivation for all thicknesses. At lower temperatures, similar to the 1DT samples, thicker layers generally lead to a lower passivation. This might presumably be due to the hydrogen content being relatively low and its

diffusion speed being too slow to saturate dangling bonds at the poly-Si/SiO_x interface efficiently for thicker layers. This is no longer true at higher temperatures. For instance, at 915°C the highest iV_{OC} of 714 mV is obtained for the 5DT layer, while for 1DT it is lower with 693 mV. Thus, for multiple drive-throughs high passivation values can be accomplished. Importantly, high passivation levels are only possible in a narrow temperature range at higher firing temperatures, which is not typically the case for HTPC samples.

4.2.3. Interfacial Oxides

Besides the effect of a-Si thickness, the interfacial oxide plays an essential role for the properties of passivating contacts, as already demonstrated in Section 4.1 for long annealing times. This section focuses on the impact of different oxides on passivation and dopant distribution during firing at varying temperatures. To examine this, four different oxides were grown on an (n) c-Si base, and an 80 nm thick lowly doped (p) a-Si layer was symmetrically deposited on both sides. A 75 nm thick SiN_x layer was then deposited, followed by firing at different temperatures.

Microstructure

A variation in the underlying oxide exhibited no measurable impact on the XRD profiles, and thus no distinguishable differences in crystallite sizes compared to those presented in Figure 4.8(a). Similarly, ECV measurements did not reveal significant differences between the interfacial oxides, indicating minimal dopant in-diffusion. However, ECV measurements are not ideally suited for accurately determining in-diffusion in the presence of steep doping profiles, where two main reasons can be found. Firstly, the spatial resolution of the ECV technique is constrained due to difficulties in controlling the etching process, leading to an averaging effect that underestimates the steepness of the doping profile. Secondly, the capacitance in ECV measurements is linked to the depletion region at the semiconductor-electrolyte interface. In cases of steep doping profiles, the depletion region may span a wide range of doping concentrations, resulting in a less defined profile.
To overcome these limitations, dopant in-diffusion has been simulated in different studies using various approaches [98, 258]. When intending to compare different interfacial oxides, a key issue for an accurate simulation is the exact knowledge of simulation parameters. Especially the activation energy for and diffusivity in the respective materials is difficult to determine. Thus, in the following literature results for diffusion through oxides will be used to understand the impact of annealing onto boron in-diffusion for different interfacial oxides.

Previous studies have established an enhanced diffusivity for boron diffusion in thinner oxides, particularly when hydrogen or oxygen is introduced into the atmosphere during oxide growth [268–270]. This sensitivity can be attributed not only to oxide thickness but also to differences in activation energy. While Feldmann et al. used an activation energy of 3.5 eV to simulate diffusion through a thermal oxide [258], a lower activation energy of 3 eV has been reported for boron diffusion through a thermal oxide grown in a hydrogen-containing atmosphere [270]. In chemical oxides, the activation energy may be reduced even further. This can be explained by the fact that chemical oxides are typically less dense, more porous, and offer additional diffusion pathways for boron atoms. Fair proposed that boron primarily diffuses via peroxy linkage defects (PLDs), where boron atoms occupy oxygen vacancies, providing pathways for diffusion through the oxide layer [268]. The prevalence of PLDs is linked to oxygen distribution within the SiO_x layer, suggesting that interfacial oxide stoichiometry plays a critical role in boron diffusion. Due to the thermal instability of the chemical oxides used in this study, the stoichiometry is likely to differ between thicker thermal oxides and thinner chemical oxides, potentially leading to more PLDs and enhanced diffusion in chemical oxides.
Thus, the combination of lower activation energy and reduced oxide thickness in chemical oxides can explain the increased dopant in-diffusion observed in Section 4.1. A similar behavior likely applies to in-diffusion during firing, particularly at higher firing temperatures, where small amounts of in-diffusion may occur. This is expected to be more pronounced in chemical oxides compared to thermal oxides. Even minor in-diffusion can enhance passivation by contributing to field-effect passivation, as discussed in the following.

Passivation

Figure 4.13 demonstrates the impact of different oxides and firing temperatures on iV_{OC} values. Error bars are omitted for clarity and because the errors for all data points are $<$ 10 mV. An overall higher passivation level is found for the chemical oxides compared to the thermal ones across nearly all firing temperatures, with a maximum $iV_{OC} >$ 720 mV. The temperature dependence is similar for all oxides, where the passivation increases to a maximum at 875-900°C and decreases at higher temperatures. This decrease is likely related to hydrogen induced defects and blisters detected via optical microscopy.
For comparison, samples were also fired without SiN_x deposition, resulting in a significantly lower passivation level of $iV_{OC} \approx$ 540 mV for all oxides and firing temperatures. This reduction can be attributed to insufficient chemical passivation due to the absence of hydrogen released from the SiN_x layer during firing, highlighting the importance of hydrogenation for FPC layers further. Due to a suspected increased dopant in-diffusion in chemical oxides

compared to thermal ones, a simultaneous increase in chemical passivation via hydrogenation and field-effect passivation through minimal dopant in-diffusion seems likely to explain the differences in Figure 4.13. Even small amounts of in-diffusion can lead to enhanced field-effect passivation, thereby producing higher iV_{OC} values.

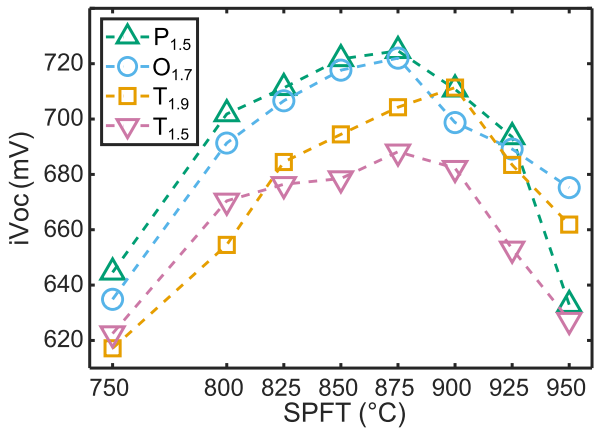

Figure 4.13.: *iV_{OC} values for different interfacial oxides after SiN_x deposition and firing.*

In addition to diffusion through an intact oxide, chemical oxides are less thermally stable during annealing (Section 4.1), which can result in pinhole formation. It remains unclear whether pinholes can form during short annealing at high temperatures. If so, pinhole formation could lead to enhanced local dopant in-diffusion and promote charge carrier transport through the oxides, potentially improving passivation by increasing band bending and field-effect passivation. Thus, in Chapter 5, charge carrier transport through the interfacial oxide is discussed in detail.

4.3. Chapter Summary

This chapter explored the influence of different thermal budgets on properties such as dopant in-diffusion, crystallization, sheet resistance, and passivation. The first part focused on various annealing times and interfacial oxides for PECVD and APCVD a-Si. It was found that oxide type and annealing times significantly impacted the doping profile and needed to be carefully matched to one another, as thinner oxides led to more significant in-diffusion at long annealing times than thicker oxides. For phosphorus doping, a "kink-tail" profile was observed due to in-diffusion into the base. In the case of APCVD (p) a-Si, a maximum doping concentration was found in the middle of the layer due to the deposition process. Additionally, XRD measurements revealed increasing crystallite sizes with longer annealing times, where APCVD a-Si produced larger crystallites than PECVD, attributed to the higher deposition temperatures in APCVD processes. Moreover, sheet resistance decreased with

thinner oxides and longer annealing times. It was observed that the sheet resistance of (p) a-Si was higher than that of (n) a-Si, consistent with the literature. Finally, passivation was greatly influenced by the hydrogenation step via SiN_x deposition and fast firing. Thicker oxides allowed for higher thermal budgets while maintaining good passivation, whereas thinner oxides enabled high passivation values above 700 mV with minimal annealing for both APCVD and PECVD a-Si, regardless of doping type.

The second part of this chapter examined the impact of different firing temperatures on non-metallized contact properties. A significant finding was that PECVD a-Si layers were not well-suited for the FPC concept due to severe blistering after firing with a SiN_x layer. In contrast, APCVD a-Si did not suffer from this limitation due to its lower hydrogen content. Crystallinity and crystallite size increased significantly at a critical firing temperature around 800°C, after which crystal growth slowed down with higher firing temperatures. Furthermore, doping concentration and type also affected crystallization kinetics, with higher boron concentrations slowing down crystallization and producing smaller crystallites compared to lower doped (p) a-Si or even (n) a-Si. The increase in crystallite size corresponded with a decrease in sheet resistance at higher firing temperatures. However, a higher boron concentration led to increased sheet resistance, possibly due to inactive boron in the a-Si layer. Similar to various annealing times, (n) a-Si showed a lower sheet resistance overall, though (p) a-Si exhibited a more substantial decrease in resistance at higher firing temperatures. Passivation decreased for (n) a-Si at higher firing temperatures, making it less suitable for the FPC concept, while (p) a-Si exhibited improved iV_{OC} values at higher temperatures. However, without proper SiN_x design to prevent blistering, passivation degraded towards higher firing temperatures.

A variation in a-Si thickness showed little impact on crystallization or doping profiles. Even when using multiple DT, a doping maximum in every individual DT remained. Thicker a-Si layers further reduced sheet resistances due to a larger area available for conduction. However, an additional resistive contribution from the interlayer oxide was noted. Passivation decreased slightly for thicker a-Si layers in the case of one drive-through. However, increasing the number of drive-throughs at high firing temperatures improved passivation, achieving iV_{OC} values above 710 mV due to efficient hydrogenation during firing.

Varying the interfacial oxide led to higher passivation levels for chemical oxides compared to thermal oxides, with a maximum iV_{OC} exceeding 720 mV for 1DT layers. However, at the highest firing temperatures, passivation levels decreased, likely due to hydrogen-induced defects and blistering during firing. A discussion of boron diffusion through oxides suggested in-diffusion already during firing at higher temperatures. This may enhance field-effect passivation, especially for thinner chemical oxides.

5. Charge Carrier Transport

This chapter aims to generalize the impact of low thermal budget annealing on charge carrier transport. Two major transport pathways can be distinguished. Firstly, transport through the *interfacial oxide*, discussed in Section 5.1.1. The second pathway is transport through the *poly-Si* layer, discussed in Section 5.2.

5.1. Transport Through the Oxide

This section focuses on charge carrier transport through the interfacial oxide, which can occur either by *tunneling* through the oxide or via *pinholes* in the oxide. For passivating contacts, it is particularly important to maximize the selectivity of the contact, which refers to the ability to collect majority carriers at the contact without hindrance, while impeding the recombination of minority charge carriers [76]. A too thick oxide can increase the contact resistance and the series resistance of the entire cell. Therefore, the oxide must be thin enough to allow charge carriers to pass but still maintain high passivation.
In the case of HTPC different methods are available to tune the transport mechanism. Apart from choosing an interfacial oxide thickness and type, the annealing time and temperature can be varied accordingly to achieve optimal results. This allows for a wide processing range to enable high passivation and low sheet resistances. However, for the FPC approach the process window is much narrower, as the firing temperature is the only way to adjust the thermal budget of the whole process. Moreover, high passivation and lower sheet resistances are found at high firing temperatures, further limiting the ability to fine-tune optimal annealing conditions. Therefore, it is essential to choose an interfacial oxide suitable for the short annealing step.
One key parameter for finding optimal oxide-annealing combinations for charge carrier transport is the oxide thickness. If the oxide is too thick ($>$ 2 nm), the tunneling probability decreases significantly and charge carrier transport must occur through pinholes created during annealing. For thinner oxides the transport mechanism depends on the annealing conditions. It has been observed that a shift from tunneling-dominated to pinhole-dominated

transport can occur during extended annealing due to pinhole creation [76, 78, 79]. If passivation remains unaffected, this shift is often favorable for transport properties, as pinhole transport typically results in lower contact resistivities [78, 79]. Interestingly, these studies suggest that the total annealing duration might not be the primary factor for this transition, but rather the process temperature.

The goal of this study is to investigate the speed at which this shift occurs and whether the total duration or temperature of the process is the dominating factor. To explore this, 30 nm APCVD (n) a-Si layers were deposited on one side of different SiO_x layers and annealed using various thermal budgets by varying the time and peak temperature of the annealing profiles. After annealing, Ti/Ag/Al TLM patterns were evaporated and the poly-Si was selectively removed between the fingers using plasma etching. T-TLM measurements were then conducted (described in Section 3.3.3) to distinguish between tunneling, pinhole, and combined transport mechanisms, which is presented in Section 5.1.1. Additionally, the a-Si layer was removed using tetramethylammonium hydroxide (TMAH) to magnify pinholes for SEM imaging, detailed in Section 5.1.2. The results of T-TLM and pinhole investigations have been published in [232], where all major aspects of the work were carried out by the author, including experimental design, data collection, analysis, and manuscript writing.

5.1.1. Temperature-Dependent TLM

This section examines the impact of different annealing profiles, shown in Figure 2.9, on different oxides. Fit parameters for every oxide-annealing combination can be found in the Appendix A.2. Figures 5.1(a) and 5.1(b) show the T-TLM measurements and fits corresponding to the annealing processes for the (a) $P_{1.5}$ and (b) $O_{1.4}$ oxides after undergoing the R700°C, R5s, R30s, and D920°C processes.

For both oxides, the R700°C process can be described by the tunneling model. In the case of the $P_{1.5}$ oxide in Figure 5.1(a), an activation energy $\Delta E_s = 66$ meV is found, aligning with literature values, where a range of 20-200 meV has been reported [76, 78, 79]. When choosing the oxide thickness as fitting parameter, $d_{ox} = 1.5$ nm is obtained, which matches the results from ellipsometry measurements and further validates this evaluation method. Interestingly, the temperature dependence of the contact resistivity changes for the R5s annealing, showing an increase in resistivity with higher measurement temperatures (note the logarithmic y-axis). This temperature dependence is well described through the pinhole model, yielding good agreement at a doping level of $N_{diff} = 7.5 \cdot 10^{14}$ cm^{-3}, which is close to the measured base doping level of approximately 5 Ωcm [233]. The pinhole density is determined to be $N_P = 1 \cdot 10^8$ cm^{-2}, with a pinhole radius of 4.2 nm. Further increasing the annealing time by using the R30s process leads to only slight changes in the resulting

T-TLM data and fit parameters. Even with a significantly increased thermal budget through the D920°C annealing, the course of ρ_C is only affected at low measurement temperatures due to increased dopant in-diffusion into the base.

Similar observations can be made for the $O_{1.4}$ oxide in Figure 5.1(b), where the temperature behavior also shifts with higher TB. However, the contact resistivity after R5s annealing decreases marginally over the entire temperature range, as opposed to the exponential decay seen for treatment at lower temperatures. Likewise, the R30s annealing introduces a temperature dependence with a maximum around 300K. As neither the pinhole nor tunneling model provides a good fit to the data, the combined model was used, which yielded a pinhole density of $N_P \approx 1 \cdot 10^7$ cm $^{-2}$. Thus, for both oxides in Figure 5.1 a shift from tunneling to combined transport or pinhole transport occurs in a short time frame. When comparing this to the D920°C annealing, one once again sees pinhole-dominated transport with a higher pinhole density of $N_P \approx 1 \cdot 10^8$ cm^{-2}, similar to the $P_{1.5}$ oxide. While Folchert et al. previously observed a combination of pinhole and tunneling transport for extended crystallization, such a combination has not been reported for short annealing times [79].

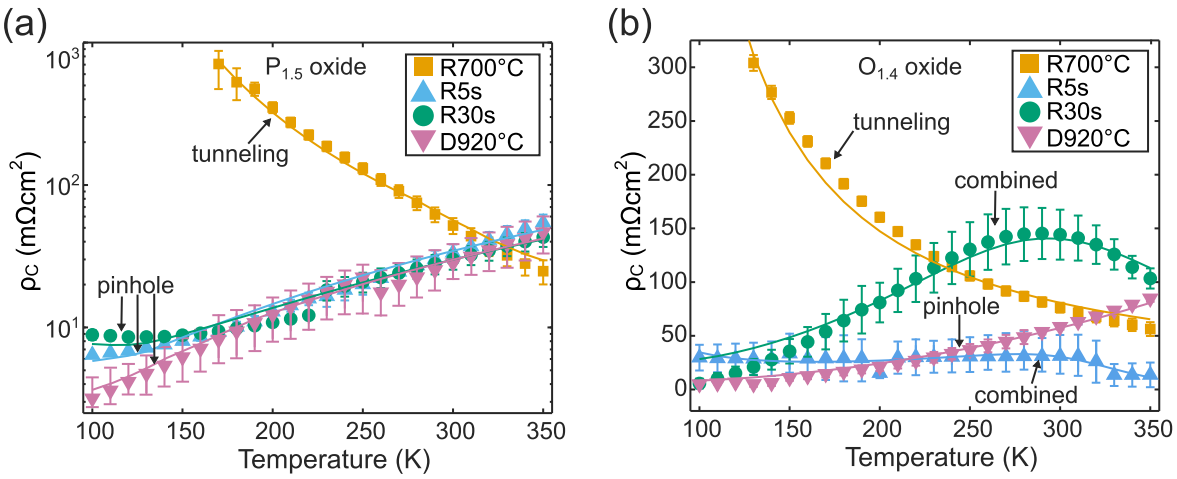

Figure 5.1.: *T-TLM measurements and fits for the (a) $P_{1.5}$ and (b) $O_{1.4}$ oxides after R700°C, R5s, R30s, and D920°C annealing steps for APCVD (n) a-Si [232].*

For the $O_{1.7}$ and $T_{1.5}$ oxides in Figures 5.2(a) and 5.2(b), a firing step at 850°C SPFT (FF850°C) is shown instead of the R700°C process. The main difference between the FF850°C and R5s profiles is an approximately 20°C higher peak temperature for the firing process and on the other hand an overall longer process for the R5s annealing. Importantly, although the thermal profiles of the FF850°C and R5s annealing processes are quite similar, the resulting T-TLM data differ significantly, pointing to an increased influence of temperature onto the transition properties.

For both oxides in Figure 5.2, the firing step results in behavior best described by the combined model. On the other hand, the R5s annealing leads to mostly tunneling-dominated

transport. For the $T_{1.5}$ oxide in Figure 5.2(b), a slight deviation from the exponential decay is observed at lower temperatures, which can only be modeled by the combined model, though the transport is still predominantly tunneling driven. As the thermal budget increases further via R30s annealing, the transport mechanism shifts once again to pinhole-dominated transport. By comparing the R5s annealing for the $O_{1.7}$ and $O_{1.4}$ oxides, one can observe that the thicker oxide requires a higher thermal budget for the transition from tunneling to pinhole transport to occur.

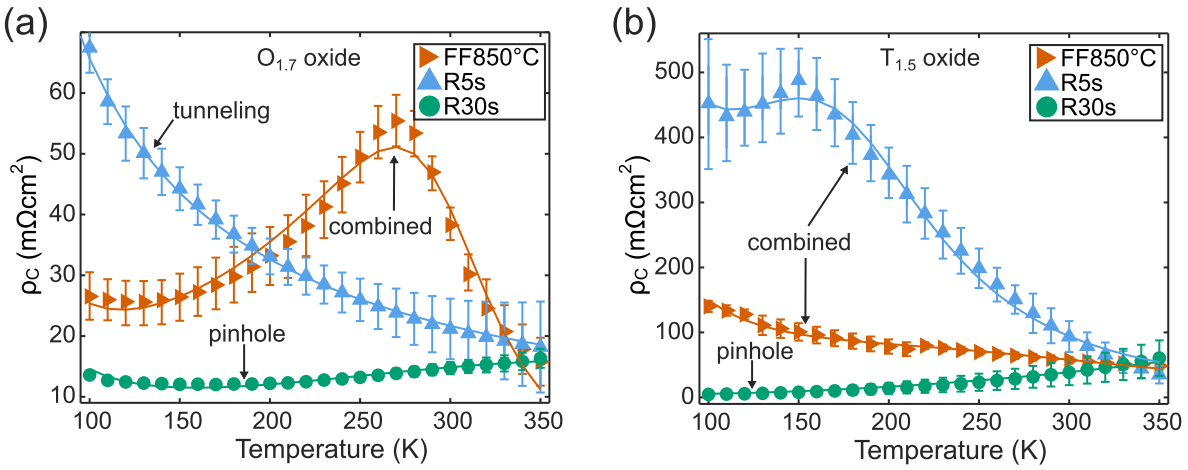

Figure 5.2.: *T-TLM measurements and fits for the (a) $O_{1.7}$ and (b) $T_{1.5}$ oxides after firing at 850°C SPFT, R5s, and R30s annealing for APCVD (n) a-Si [232].*

To confirm that these shifts from tunneling to pinhole regime for every oxide are indeed related to changes within the oxide layer and are not induced through the APCVD deposition itself, these results are compared to 130 nm thick PECVD (n) a-Si layers. Figure 5.3 shows T-TLM measurements for PECVD (n) a-Si deposited on the $P_{1.5}$ and $O_{1.7}$ oxides for different annealing conditions.

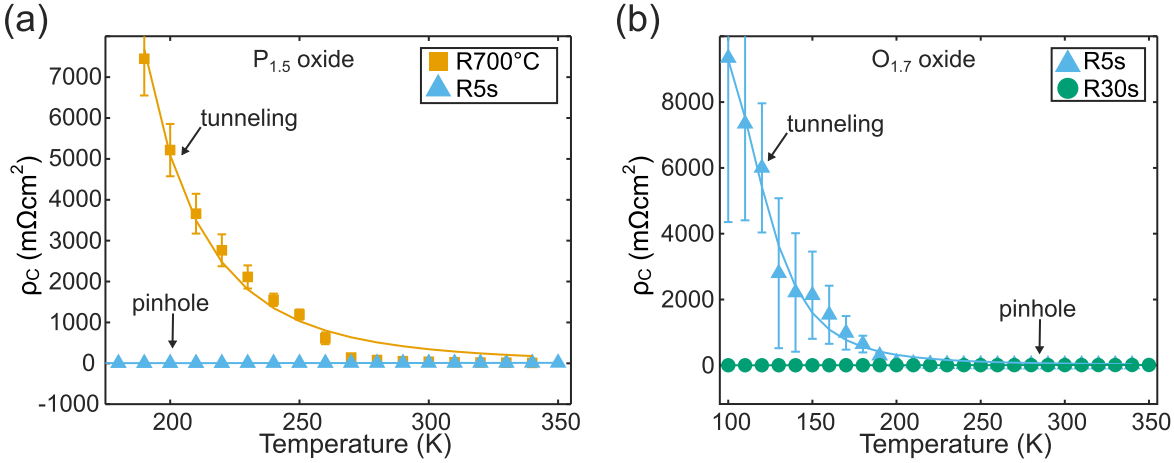

Figure 5.3.: *T-TLM measurements and fits for the (a) $P_{1.5}$ and (b) $O_{1.7}$ oxides with PECVD (n) a-Si for different annealing steps.*

For both oxides, a shift from tunneling- towards pinhole-dominated transport is observed as the thermal budget increases. This is the case despite differences in the properties of APCVD and PECVD a-Si layers, such as thickness and doping concentration. Interestingly, a transition from tunneling to pinhole regime occurs under the same annealing conditions as for APCVD a-Si in Figures 5.1 and 5.2. Based on these findings, it is assumed that the change in transport mechanism is primarily linked to the properties of the oxides themselves, rather than being a consequence of the a-Si deposition technique, thickness, or doping concentration.
Thus, a transition from tunneling- to pinhole-dominated transport is observed for all oxides. While the exact conditions of this transition vary from oxide to oxide, it surprisingly takes place in the scope of just a few seconds.
To better understand these observations, Figure 5.4 illustrates the pinhole fraction

$$f_{\mathrm{P}} = \frac{\rho_{\mathrm{C}}(T)}{\rho_{\mathrm{C,P}}(T)} \tag{5.1}$$

in dependence of the thermal budget at room temperature. The individual tunneling and pinhole contributions to the contact resistivity are considered in the calculation of f_{P} [79]. A pinhole fraction of $f_{\mathrm{P}} = 1$ corresponds to fully pinhole-dominated transport, while $f_{\mathrm{P}} = 0$ indicates no contribution from pinholes. It is evident from Figure 5.4 that a higher thermal budget generally leads to a larger pinhole fraction for all studied oxides. Importantly, the shift from tunneling to pinhole regime happens significantly faster than previously assumed.

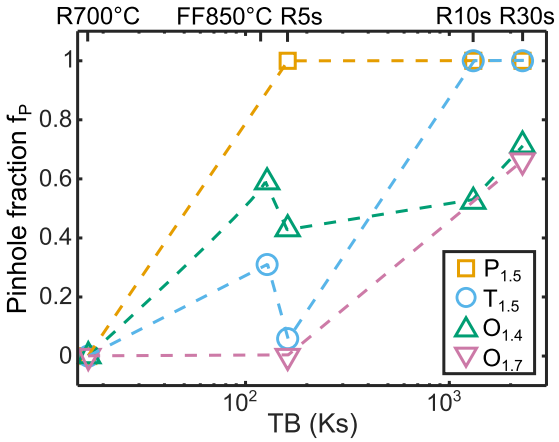

Figure 5.4.: *Pinhole fraction f_P, calculated according to Equation* (5.1) *at room temperature, is shown as a function of the thermal budget for different oxides and annealing steps [232].*

Additionally, one notable observation from Figure 5.4 is the distinction between the effects of the FF850°C firing step and the R5s annealing. Although the firing process corresponds to a lower thermal budget, it induces a more rapid transition to pinhole-dominated transport. This suggests that the higher peak temperature of the firing step during annealing plays a

more critical role than the total duration of the process. Creation of pinholes in such short time spans, with a heightened sensitivity to temperature, is a novel observation and will be explored further in the next section.

5.1.2. Pinhole Investigation

The formation of pinholes was examined using SEM top-view imaging, requiring the removal of the a-Si layer. In recent years, tetramethylammonium hydroxide (TMAH) has been identified as a suitable candidate for pinhole magnification studies [271, 272]. This is due to its high selectivity between poly-Si and SiO_x, which leads to an etch stop at the interfacial oxide while still etching poly-Si [271, 273, 274]. After the poly-Si is etched away, TMAH begins to etch the c-Si base beneath the regions where the interfacial oxide is disrupted, thereby magnifying existing pinholes and enabling detection via SEM. The etching rate is increased by several factors, including higher TMAH concentration, TMAH temperature, sample crystallinity, and lower doping concentration [271, 272]. In [257] varying etch rates for poly-Si were observed for differently doped and crystallized a-Si layers. The study found that the etch rates differ between (n) a-Si and (p) a-Si as well as between HTPC and FPC samples. Additionally, for 2DT layers the effect of the interlayer oxide was evident, as the poly-Si thickness stagnated with increasing etching time. In the case of high boron doping concentrations, the etch rate can be significantly reduced and may even lead to an etch stop, especially in the case of possible boron-rich layers after crystallization. [169, 274–276]. Thus, (n) a-Si was used in this investigation to investigate pinhole formation during annealing.

SEM Investigation

The following results were obtained using 30% diluted TMAH at an etching temperature of 70°C. Examples of SEM images are shown in Figure 5.5 for the $P_{1.5}$ oxide after R700°C and R5s annealing. For samples where tunneling is the dominant transport mechanism according to T-TLM measurements, such as in Figure 5.5(a), no pinholes are visible. This observation holds even when the etching time is varied. In contrast, when pinhole dominated transport occurs, as shown in Figure 5.5(b), pinholes can be detected in SEM images. Similar behavior is observed for the other oxides as well, supporting the results from T-TLM measurements.

When trying to determine the pinhole density from SEM images, several issues occur. Firstly, the oxide varies in thickness throughout the sample, which can lead to an earlier disruption on some points during annealing and etching [272]. Secondly, a-Si thickness and doping inhomogeneity might affect the local etch rate, further leading to a differing

amount of pinholes being visible. This leads to a broad distribution of pinholes, as can also be seen in Figure 5.5(b).

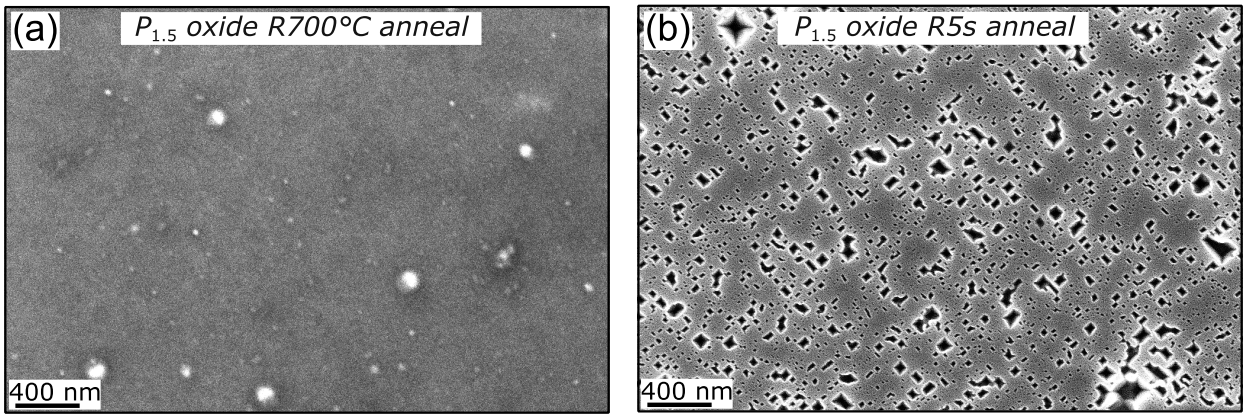

Figure 5.5.: *SEM images after 60 s TMAH etching at 70°C for the $P_{1.5}$ oxide after (a) R700°C and (b) R5s annealing [105].*

Estimating the pinhole density with a simple imaging tool can yield different values, depending on the size of pinholes considered. For instance, the estimated pinhole density is found to be $N_P \approx 1 \cdot 10^8$ cm^{-2} when one considers only the larger pinholes with an edge length $>$ 50 nm. When including all visible holes one finds a larger pinhole density $N_P \approx 2 \cdot 10^8$ cm^{-2}. These values are consistent with T-TLM results, where a pinhole density of $1 \cdot 10^8$ cm^{-2} was found. It is noteworthy that a longer etching time can further increase the amount of pinholes visible, pointing to the formation of additional pinholes during etching due to the differing oxide thickness. For instance, by extending the etching time to 2 min, the pinhole density goes up to $N_P \approx 1 \cdot 10^9$ cm^{-2} for the large pinholes. As the TMAH etching rate is influenced by the crystallinity and thus annealing conditions, it was not possible to accurately compare pinhole densities between different types of samples. However, the overall agreement between T-TLM results and SEM investigation in this particular case clearly points towards the creation of pinholes during short annealing.
While the existence of pinholes in chemical oxides has been observed previously, this was primarily for well-crystallized a-Si layers [271]. The rapid pinhole formation seen here at short annealing times appears to contradict the widely recognized pinhole growth model by Ajuria et al., which will be discussed next [87].

Pinhole Growth

According to this pinhole growth model, growth of pinholes is governed by the time-dependent rate Equation (2.16). After parameterizing the annealing profile, this equation can be solved numerically using FlexPDE. The pinhole growth rate is largely influenced by temperature,

oxide thickness, and the activation energy E_A, corresponding to the energy necessary for the process to start. Few studies have been conducted on pinhole growth for short annealing times, and it is unclear whether this model needs to be modified in this case.

To understand the influence of these parameters on pinhole growth, Figure 5.6(a) illustrates the dependence of pinhole radius on activation energy for R30s annealing with $\beta = 4.6 \cdot 10^{-26}$ cm^4/s [87]. It is clearly visible that a larger activation energy significantly decreases the pinhole radius. Ajuria et al. reported activation energies ranging from 0.8 to 2.2 eV [87]. Even when taking the lower limit of $E_A = 0.8$ eV arbitrarily, one can find a pinhole radius of ≈ 1 nm after the R30s annealing, which is smaller than those determined by T-TLM measurements. This deviation is even more apparent when considering Figure 5.6(b), where the temporal evolution of the pinhole radius for different temperatures is shown with $E_A = 0.8$ eV. One can see that the pinhole growth is heavily facilitated by a higher annealing temperature. However, for short annealing times (< 1 min), the pinhole radii are considerably smaller than those reported by experimental T-TLM measurements or SEM pinhole analysis.

Of course, the simulation parameters are chosen somewhat arbitrarily and are not adjusted to the specific layers used in this investigation. However, these findings indicate that the rather simple pinhole growth theory in Equation (2.16), which is based on a slow diffusion process, can not accurately describe the pinhole formation observed in T-TLM and SEM measurements. While the theory seems to work for extended crystallization [77, 98, 272], a modification of the model is required for short high-temperature annealing steps, where a sudden temperature-induced break-up of the oxide is observed, which is not reliant on diffusion of atoms through the oxide.

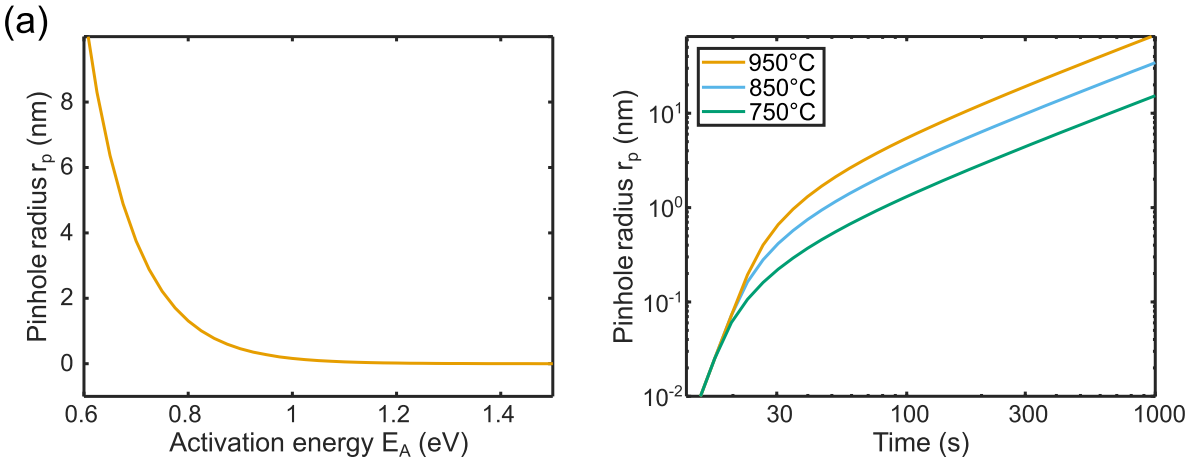

Figure 5.6.: *(a) Calculated pinhole radii for different activation energies after R30s annealing. (b) Temporal development of pinhole radius for annealing at different temperatures with $d_{ox} = 1.5$ nm, $E_A = 0.8$ eV, and $\beta = 4.6 \cdot 10^{-26}$ cm^4/s.*

One possibility to incorporate these findings into the existing model is to define different

growth regimes, where growth parameters vary depending on time and temperature. This would allow early-stage growth to be described by a different set of parameters than the long annealing processes, while still providing consistent description for extended annealing.

5.2. Transport Through the Poly-Si

After discussing transport through the oxide in the previous section, this section addresses lateral charge carrier transport through the poly-Si layer itself. In Chapter 4 it was found that a lower thermal budget leads to a lower crystallintiy and crystallite size as well as higher sheet resistance, which can increase the series resistance in a solar cell device, reducing the overall power output of the cell. The importance of the XRD crystallite size for the lateral sheet resistance R_{Sheet} is exemplified in Figure 5.7 for a 130 nm thick (p) a-Si layer on Cz and FS substrates. It is visible that the sheet resistance decreases with larger crystallite size for most samples, in particular on the Cz base. For the highly doped (p) a-Si layer in Section 4.2.1, this relationship could be described using a simple inverse proportionality between crystallite size and resistivity [105]. However, the slight increase in R_{Sheet} towards larger crystallite sizes, especially for the FS base, suggests that additional factors need to be considered. A model to describe charge carrier transport in poly-Si is described in Section 2.3.4, which has proven successful to describe lightly doped poly-Si layers [115]. However, it remains unclear whether this model is applicable for thin and highly doped a-Si layers that are typically used in poly-Si based passivating contacts.

To conduct the first part of this investigation, fused silica is chosen as base substrate. This is done in order to focus on charge carrier transport within the poly-Si layer itself without interference from the base. Since FS is a dielectric material, preventing charge carrier transport through the base material, the bare poly-Si layer can be investigated by electrical characterization techniques, such as Hall and 4PP measurements. Even if in-diffusion into the base occurs, those dopants do not or only very little contribute to charge carrier transport.

However, the deposition of a-Si onto FS substrates, followed by additional processing, might produce layers with varying characteristics compared to those deposited on Cz substrates, as mentioned in Section 4.2.1. This difference is mainly due to the higher thermal mass of FS samples, leading to an altered deposition and processing temperature. Although the resulting thicknesses were found to be comparable to films on Cz substrates, the primary difference lies in the doping profile and possibly crystallinity within the a-Si. This was evident in Figure 4.4, where a sharper doping peak was observed within the poly-Si layer on FS bases compared to Cz bases.

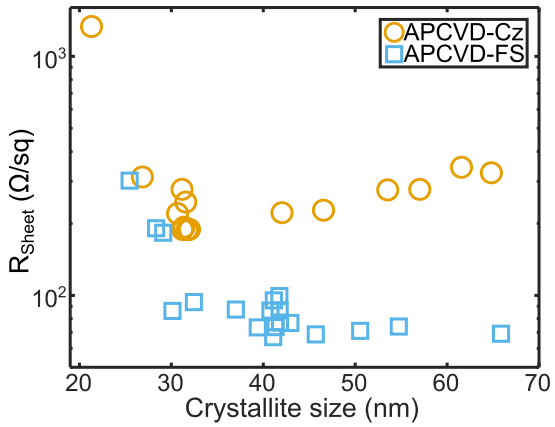

Figure 5.7.: *Relationship between XRD crystallite size and 4PP sheet resistance for APCVD (p) a-Si after different annealing steps for FS and Cz base material.*

The following description builds upon the model formulated by Seto [115] (Section 2.3.4) and aims to relate the experimentally determined sheet resistance with the calculated theoretical resistance R_{theo} obtained through mobility and crystallite size measurements. This is done in three steps. Firstly, the relationship between mobility and crystallite size in Equation (2.24) requires determining the barrier height V_{B} between crystallites. This value is extracted in Section 5.2.1 through temperature-dependent Hall measurements, where different evaluation strategies are discussed. Secondly, the average carrier density n_{avg} is required to connect mobility to resistivity, which is obtained through ECV measurements. Lastly, to determine the theoretical resistance R_{theo}, the contributions from the depletion region and the crystalline regions may need to be considered according to Equation (2.25) and Equation (2.27). These factors are accounted for in Section 5.2.2 for APCVD (p) a-Si layers on an FS base and then briefly investigated for a 1DT (p) a-Si layer on a Cz substrate.

5.2.1. Microscopic Investigation of Resistivity

Figure 5.8(a) shows examples of temperature-dependent Hall measurements in a range between 100-350K, where the mobility is displayed as a function of the inverse thermal energy $\frac{1}{k_{\text{B}}T}$ for different annealing conditions. It can be seen that shorter annealing times and lower firing temperatures, corresponding to a lower TB, result in reduced mobilities over the entire measured temperature range. This is in agreement with results for Hall mobilities at room temperature in Section 4.1.

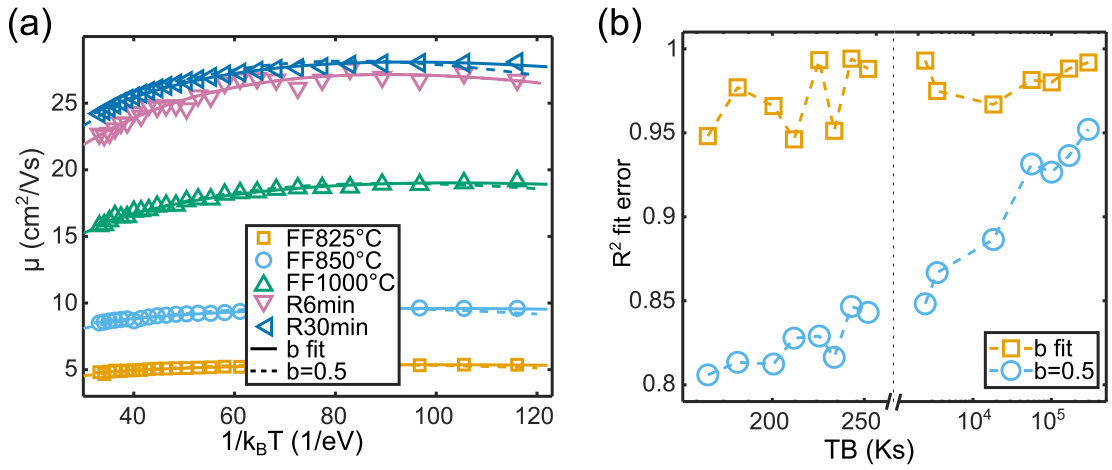

Figure 5.8.: *(a) Examples of T-Hall measurements for APCVD (p) a-Si on FS substrates with corresponding fits according to $\mu = ax^b \exp(-cx)$ with $b = 1/2$ and b as independent fit parameter. (b) R^2 fit error in dependence of the thermal budget for $b = 1/2$ and with b as fit parameter.*

Evaluation of T-Hall measurements

There are different ways to evaluate T-Hall measurement to obtain the barrier height V_B. One method, proposed by Colinge et al., assumes a "boundary mobility" and relies on a parametrization of the mobility [116]. However, this approach only applies in cases where crystallites are fully depleted and is therefore not employed here. Rather, the temperature dependence of Hall measurements is modeled via Equation (2.24), which is based on the current density

$$J = q^2 n_{avg} \sqrt{\frac{1}{2\pi m_{eff} k_B T}} \exp\left(-\frac{qV_B}{k_B T}\right) V \tag{5.2}$$

for a small applied voltage $V < k_B T$ across a grain boundary [115]. This equation bears a resemblance to the Richardson-Dushman Equation (2.13) for thermionic emission, but is modified empirically to account for the presence of grain boundaries via a different temperature dependence. Instead of a $J \propto T^2$ relationship, Seto proposes a $J \propto T^{-0.5}$ relationship for charge carrier scattering at grain boundaries, which has been experimentally confirmed for lightly doped poly-Si layers with doping concentrations between $1 \cdot 10^{16} - 5 \cdot 10^{19}$ cm^{-3} [115, 117, 277]. J can be used to calculate the in Section 2.3.4 found mobility expression

$$\mu = JL/qn_{avg}V = \mu = Lq\sqrt{\frac{1}{2\pi m_{eff} k_B T}} \exp\left(-\frac{qV_B}{k_B T}\right), \tag{5.3}$$

resulting in a $\mu \propto T^{-0.5}$ dependence [115]. However, in the case of high doping, a different temperature dependence than that proposed by Seto may occur, which will be investigated in the following.

Equation (2.24) can be written as $\mu = ax^b \exp(-cx)$, with $x = 1/k_B T$, $a = Lq\sqrt{\frac{1}{2\pi m_{eff}}}$,

$b = 0.5$, and c being the barrier height V_B in units of eV. Following the approach by Seto, this equation is fitted to the T-Hall data in Figure 5.8, where a and c are now treated as independent fit parameters. A slight deviation between the fit and data is noticeable at low temperatures, particularly for samples with lower thermal budgets. This is reflected in the R^2 fit error, shown in Figure 5.8(b), where an R^2 value of 1 represents a perfect fit, while lower values indicate worse fit quality. The data points on the left of Figure 5.8(b) correspond to different set peak firing temperatures, while those on the right reflect varying annealing times in the RTP furnace.

Possible reasons for this small deviation could include the higher doping concentration in this study and the larger temperature range between (100-350K), whereas most studies focused on lower doping concentrations ($< 5 \cdot 10^{19}$ cm^{-3}) and a narrower temperature range around room temperature [115, 117]. It is to be expected that a wider temperature range produces more deviations, since Equation (2.24) is an empirical approximation. At lower temperatures, the tunneling contribution across grain boundaries increases relative to thermionic emission, as fewer carriers are thermally excited. This causes mobility to be less sensitive to temperature changes, which could lead to a lower value of b.

Additionally, Equation (2.24) does not account for mobility contributions within individual crystallites, which may become significant if the depletion region is much smaller than the crystallite size, as is the case for high doping conditions. In the case of monocrystalline silicon within a particular grain, different scattering mechanism occur, such as phonon, impurity, or carrier-carrier scattering. It has been suggested that carrier-carrier scattering tends to dominate the temperature behavior of mobility in highly doped materials ($> 10^{19}$ cm^{-3}), due to the increased probability of scattering events [278, 279]. Furthermore, the temperature dependence of this mechanism was found to be relatively weak compared to other mechanisms, which could further point towards a smaller value for b.

Besides different scattering mechanisms, so far the assumption of a completely crystalline material has been made. Raman measurements indicate that there still might be an amorphous phase present, especially at lower thermal budgets (Figure 4.8). In amorphous phases, as discussed in Section 2.3.2, conduction via trap states can take place according to Mott's law in a $\ln(\mu) \propto T^{-\frac{1}{d+1}}$ dependency for disordered systems, depending on the dimension d [280, 281].

Given these considerations and the the fit results with $b = 1/2$, additional fits were performed by allowing the parameter b to vary over the entire measured temperature range to find a more suitable value for b under these high doping conditions in a relatively broad temperature range. This additional fit parameter produced better agreement between the fit and the experimental data, as shown in Figures 5.8(a) and (b).

The fit parameter b is displayed in Figure 5.9(a) for different thermal budgets. It can be

seen that b ranges from 0.29 up to 0.34, with a very slight increase for samples processed at higher thermal budgets. However, the overall scatter is quite low and the mean value $b_{\text{avg}} = 0.31 \pm 0.11$ suggests a deviation from Seto's original equation. Thus, in the following evaluation $b = 1/3$, instead of $b = 1/2$, is proposed as the empirically determined temperature dependence. The fit parameter c, corresponding to the barrier height V_{B}, is discussed next.

Barrier height and trap density

The barrier height V_{B} is shown in Figure 5.9(a) for the evaluation with $b = 1/3$ and $b = 1/2$. In the first case, the average barrier height is $V_{\text{B}} = (3.1 \pm 0.4)$ meV, whereas no clear trend is visible across different annealing conditions. When evaluating the data with $b = 1/2$, the barrier height increases to $V_{\text{B}} = (6.69 \pm 0.9)$ meV, though the scattering of data points remains similar. Seto reported values of $V_{\text{B}} \approx 5$ meV for boron doped poly-Si layers after ion implantation and annealing at 1100°C for 30 min at a doping concentration of $5 \cdot 10^{19}$ cm^{-3}. One would expect a lower barrier height for a higher boron concentration in this study, as is indicated through Equation (2.22). This further supports the usage of $b = 1/3$ instead of the original $b = 1/2$.

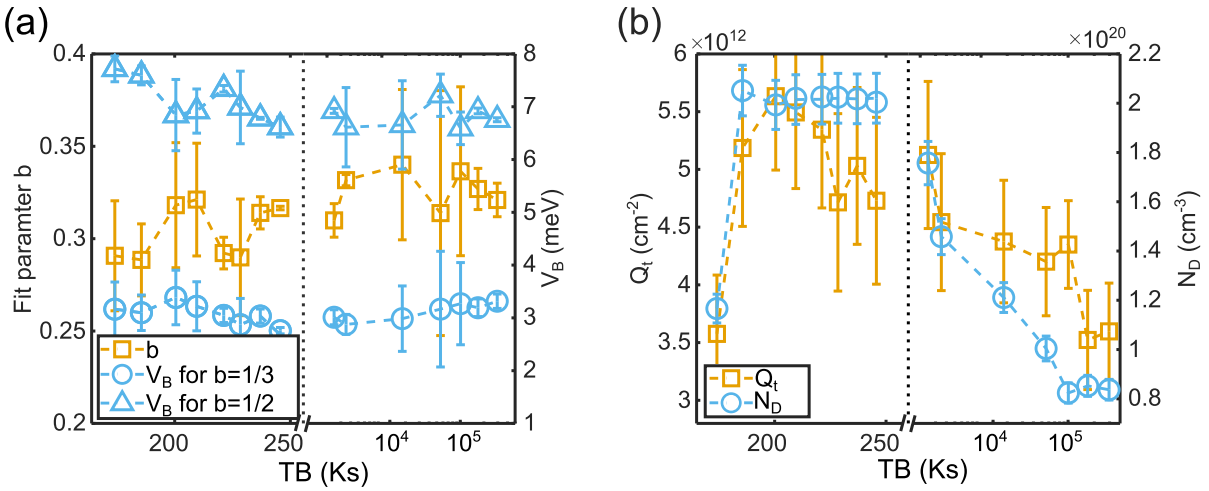

Figure 5.9.: *(a) Fit parameter b and barrier height V_B in dependence of the thermal budget for $b = 1/3$ and $b = 1/2$. (b) Calculated trap density Q_t and doping concentration N_D, determined through ECV measurements.*

In addition to calculating the theoretical sheet resistance in the next section, the barrier height can be used to determine the trap density Q_{t} using Equation (2.22). Since $Q_{\text{t}} \propto V_{\text{B}}/N_{\text{D}}$, any variation in the barrier height and doping concentration translates directly into a change in trap density. Since V_{B} is mostly constant for different TB, the doping

concentration N_D is largely responsible for a variation in Q_t. N_D is determined by averaging the ECV hole concentration within the poly-Si layer (see Figure 4.4) and is displayed in Figure 5.9(b). N_D increases at low thermal budgets, most likely due to dopant activation (see Figure 4.8). By increasing TB further, N_D get smaller, which is attributed to dopant in-diffusion into the FS base, where dopants become incorporated into the SiO_2 network without contributing to charge carrier transport. Q_t resembles this trend and decreases from approximately $5.5 \cdot 10^{12}$ cm^{-2} to $3.5 \cdot 10^{12}$ cm^{-2} with higher TB when using $b = 1/3$. Such a behavior is also expected when considering the increasing crystallite sizes at higher TB in Figures 4.5 and 4.8. These larger crystallites correspond to fewer grain boundaries, which reduces the likelihood of charge carrier trapping, thus lowering Q_t. Reported trap densities for boron- and phosphorus-doped a-Si layers vary between 1.9-$3.6 \cdot 10^{12}$ cm^{-2} [115, 117, 282]. The trap densities observed in this study are slightly higher, which may be due to higher doping concentrations, leading to more trapping of carriers at the grain boundaries. Although the trap density might be slightly elevated for the highly doped APCVD (p) a-Si layers studied here, the barrier height is more crucial for charge carrier transport, as it directly affects carrier mobility via Equation (2.24). Therefore, dopant activation is essential in order to control the resistivity. This is relatively easy to achieve for APCVD a-Si, even with a limited thermal budget. Next, the influence of the remaining fit parameter a is discussed.

Scale factor

To obtain an accurate expression for the mobility, the fit factor $a = Lq\sqrt{\frac{1}{2\pi m_{\text{eff}}}}$ has to be analyzed. Assuming L corresponds to the XRD crystallite size L_{XRD} and inserting these values into the expression for a, it becomes evident that the calculated values overestimate a compared to the fitted ones. This discrepancy has also been observed in previous studies [115, 117]. Consequently, a scale factor f has been proposed in [115], resulting in the expression $\mu = fax^b \exp(-cx)$. This factor is determined by comparing the XRD crystallite size L_{XRD} to the one determined through the fit parameter via $L_{\text{fit}} = a/(q\sqrt{\frac{1}{2\pi m_{\text{eff}}}})$, resulting in $f = L_{\text{fit}}/L_{\text{XRD}}$. f is shown in Figure 5.10(a) for the cases $b = 1/3$ and $b = 1/2$. In both cases, similar behavior across different thermal budgets is observed, with an offset factor of almost 2. The scale factor decreases slightly at lower TB but remains relatively constant overall, with an average value of $f = 0.101 \pm 0.016$ for $b = 1/3$ and $f = 0.057 \pm 0.009$ when $b = 0.5$. In other studies, the scale factor has been reported to range between 0.06 and 0.15 for significantly lower doping levels ($< 1 \cdot 10^{20}$ cm^{-3}), which overall agree with the here found values [115, 117]. The physical meaning of this scale factor was motivated by a modification of the effective Richardson constant in disordered structures and accounts for

the influence of the effective mass m_{eff}, which heavily impacts f [11, 283].
Defining a single effective mass m_{eff} for holes in silicon, particulary in poly-Si, is challenging. This arises from the anisotropic nature of the valence band structure [259]. Rather than having a fixed value, the effective mass of holes varies with crystallographic direction due to the band curvature, leading to a distribution of effective masses. In silicon, the valence band is split into light-hole and heavy-hole bands by spin-orbit coupling [259]. Since the effective mass is inversely related to the band curvature, a flatter band yields a higher effective mass (heavy holes), while a steeper curvature results in a lower effective mass (light holes) [11]. In crystalline silicon, one can typically find $m_{\text{eff,lh}} = 0.16\ m_0$ for light holes and $m_{\text{eff,hh}} = 0.49\ m_0$ for heavy holes [284].
Depending on the application, these different sub-bands are accounted for in various ways. In some cases, the density of states effective mass $m_{\text{eff,DOS}} = 0.56\ m_0$ is used, while for transport phenomena, the conductivity effective mass $m_{\text{eff,con}} = \left[\frac{1}{3}\left(\frac{1}{m_{\text{hh}}} + \frac{1}{m_{\text{lh}}}\right)\right]^{-1} = 0.37\ m_0$ is more suitable [284]. Besides these considerations, the band structure can also change with temperature, which impacts the effective mass. However, in the temperature range of 100-350K studied here, this effect can be neglected, and m_{eff} is assumed to be temperature independent [285]. A more significant impact arises from high doping levels and the corresponding high carrier concentrations. Under these conditions, the Fermi level shifts into the valence band, altering the distribution of carriers in the sub-bands. Band gap narrowing, which refers to the reduction in the energy gap between the conduction and valence bands, further modifies the band structure and the effective mass [286]. Finally, at high carrier concentrations, the valence band can become non-parabolic. The effective mass approximation for a parabolic band is no longer valid, and m_{eff} may vary with energy, making it more challenging to define a single value [287, 288].
Following this line of thought and the empirical nature of Equation (5.3), the need for an additional scale factor f becomes clear, which is calculated according to Seto's approach using $m_{\text{eff}} = m_0$. Without the scale factor, matching theoretical calculations to experimental results would require setting the effective mass to $m_{\text{eff}} \approx 115\ m_0$, which deviates significantly from typical values.
An alternative empirical correction that does not require a scale factor has been proposed in Equation (2.26) to account for the influence of film thickness [123]. This correction factor is highly dependent on the mean free path length of holes within the layer, a value that is difficult to determine accurately. For instance, a path length of 100 nm corresponds to a correction factor of approximately 0.22, while an 80 nm path length results in a correction factor of about 0.02. As a result, the validity of this empirical approach is limited and challenging to apply to poly-Si layers annealed under different conditions.

5.2.2. Correlation Between Crystallite Size and Resistivity

After examining the microscopic effects of the barrier height on charge transport, this section builds on these findings to break down the measured sheet resistance into its constituent components. The resistivity contribution due to mobility variation can be calculated using Equation (5.3) through

$$\rho_{\mu} = \frac{1}{f}\frac{1}{qn\mu} = \frac{1}{f}\frac{\sqrt{2\pi m_{\text{eff}} k_{\text{B}} T}}{Lq^2 n_{\text{avg}}} \exp\left(\frac{qV_{\text{B}}}{k_{\text{B}}T}\right), \tag{5.4}$$

where the average carrier density $n_{\text{avg}} = N_{\text{D}} - 2Q_{\text{t}}/L$ is used [115, 117]. Given the high doping level in this study, the approximation $n_{\text{avg}} \approx N_{\text{D}}$ can be applied.
Additionally, the effects of both the single crystallite resistivity and the depletion width must be considered, as outlined in Equation (2.27). The depletion width is estimated using Equation (2.25), yielding $W \approx Q_{\text{t}}/2N$, which is $<$ 0.25 nm for all samples. As the term $2W/L$ is smaller than 0.05, the impact of depletion width can be neglected in the resistivity contribution. However, the influence of single crystallite resistivity ρ_{Si} will be accounted for.
Since resistivity depends on the carrier concentration n_{avg}, ρ_{Si} is parameterized following [233, 234] for the respective measured values of n_{avg}. Finally, since the experimentally determined quantity is the sheet resistance R_{exp}, both the single crystallite resistivity ρ_{Si} and the mobility-related resistivity ρ_{μ} are divided by the poly-Si layer thickness to obtain R_{Si} and R_{μ}, respectively. Unlike in previous studies [115, 117], no additional fit parameter n was included in the exponential expression $\exp\left(\frac{V_{\text{b}}}{nk_{\text{B}}T}\right)$, as this factor lacks any physical meaning.
In Figure 5.10(b), a decreasing measured sheet resistance R_{exp} is observed with higher thermal budgets on the left side, corresponding to increasing firing temperatures. However, as TB is further increased through longer annealing times on the right side, the resistance rises slightly.
When examining the contribution from the mobility-related resistance R_{μ}, a similar trend is observed. As TB increases, R_{μ} decreases due to the crystallite growth (see Figure 4.8). Although the crystallite size continues to increase at higher TB (see Figure 4.5), R_{μ} stagnates and even increases slightly. This behavior is attributed to the decreasing carrier density in the poly-Si layer in Figure 5.9(b), caused by dopant in-diffusion into the non-conductive FS substrate, which counteracts the effects of grain growth at higher thermal budgets. At higher firing temperatures on the left side of Figure 5.10(b), R_{Si} follows the trend of R_{μ}, as minimal dopant in-diffusion occurs after initial dopant activation during firing. However, as the thermal budget increases with extended annealing times, R_{Si} rises, corresponding to a reduction in carrier density.

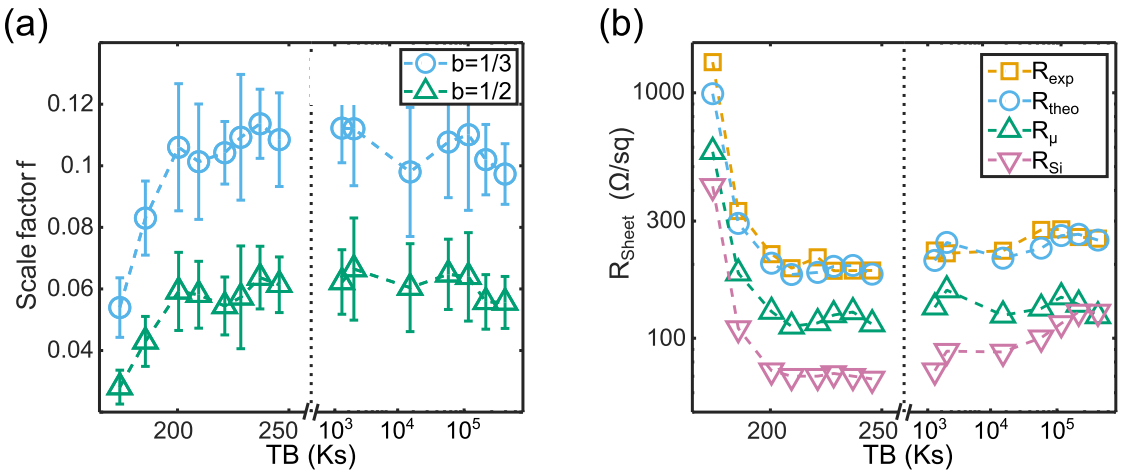

Figure 5.10.: *(a) Scale factor $f = L_{fit}/L_{XRD}$ for the evaluation with $b = 1/3$ and $b = 1/2$. (b) Different contributions to the measured sheet resistance R_{exp} for varying thermal budgets on FS substrates a comparison to the theoretical calculated resistance R_{theo}.*

Ultimately, it is evident that the grain boundary resistivity alone cannot fully explain measured resistances. Therefore, a series connection between resistance contributions within a grain (R_{Si}) and those at the grain boundaries (R_{μ}) is proposed to calculate the theoretical resistance as $R_{\mathrm{theo}} = R_{\mathrm{Si}} + R_{\mu}$ [117]. As shown in Figure 5.10(b), this expression aligns well with the experimentally determined values R_{exp}. At the lowest TB, a slight deviation is observed in the case of large sheet resistances. In this case the uncertainty in the 4PP measurements increases significantly, reaching about 20%. For values below 500 Ω/sq, the error margin is generally around 5%. Considering this measurement uncertainty, along with the limited statistics from XRD and ECV measurements, this level of agreement appears to be significant.

Cz Silicon Base

After analyzing the results obtained from FS substrates for poly-Si layers, these findings are now transferred to Cz bases, as this substrate is typically used for solar cells. A $P_{1.5}$ oxide was grown onto an (n) c-Si base, followed by the deposition of a 130 nm 1DT (p) a-Si layer. The opposite polarity of the base ensures that direct charge carrier transport during 4PP measurements occurs mostly in the poly-Si layer. However, dopant in-diffusion through the oxide into the base introduces the possibility of transport within the in-diffused region, complicating the modeling process.

As a result, T-Hall measurements reveal a significantly different behavior for samples on a Cz base, particularly for those subjected to longer annealing times. Therefore, in this analysis T-Hall data collected from FS substrates are applied to Cz samples as well.

To do so, several assumptions are made. It is assumed that the fit parameters obtained for

FS substrates can be directly applied to Cz samples. Since the barrier height shows little variability and scatter across different thermal budgets (Figure 5.9(b)), the average value is used for all samples. Furthermore, rather than determining the scale factor for each sample individually, an average value of 0.1 is taken for all samples.

Sheet resistances and XRD crystallite size were measured down to a SPFT of 725°C for Cz substrates. Crystallite sizes were slightly larger than those on FS substrates but followed the same growth trend with increasing TB. Similarly to FS substrates, ECV doping profiles were used to determine $n_{\text{avg}} \approx N_{\text{D}}$. However, instead of simply taking the average value within the poly-Si layer, the approach proposed by Kalaghichi et al. is employed to calculate $N_{\text{D}} = \frac{\int_0^x p(x)\mathrm{d}x}{d}$ by integrating over the full depth of the doping profile [289]. For samples with minimal in-diffusion, particularly those on FS substrates, this method yields the average carrier concentration within the poly-Si layer. However, for Cz samples with significant in-diffusion, the effect of the base material cannot be ignored.

The result of this analysis is shown in Figure 5.11(a). For low thermal budgets on the left side, the agreement between R_{exp} and $R_{\text{theo}} = R_{\mu} + R_{\text{Si}}$ is generally good, which can be attributed primarily to an increasing crystallite size, while n_{avg} remains largely constant. It should be noted that if the scale factor f from Seto's model with $b = 1/2$ had been applied, a significant mismatch would have occurred, supporting the approach of using $b = 1/3$. With increasing thermal budget the theoretical resistances in Figure 5.11(a) do not follow the same decreasing trend as the measured values, since the increase in crystallite size is counteracted by dopant in-diffusion into the base, which lowers n_{avg}. As the $P_{1.5}$ oxide enables charge carrier transport through the oxide by tunneling and pinhole transport, this additional conductive pathway has to be considered.

A very simplified way of incorporating transport through the in-diffused region is to model the system as a parallel circuit between the poly-Si and the resistance of the in-diffused region R_{diff} to get the total resitivity

$$R_{\text{tot}} = \left(\frac{1}{R_{\mu} + R_{\text{Si}}} + \frac{1}{R_{\text{diff}}} \right)^{-1}. \tag{5.5}$$

R_{diff} is roughly approximated through ECV measurements (Figure 4.4) by averaging the sheet resistance in the in-diffused region down to a doping concentration of 10^{18} cm^{-3}. This yields values decreasing significantly with higher thermal budgets, from $>$ 1000 Ω/sq for different firing temperatures to $<$ 200 Ω/sq for long annealing times. Figure 5.11(b) shows this correction in comparison to the measured resistance. The calculated total resistance R_{tot} aligns much more closely with the measured values (R_{exp}) for longer annealing times. For lower thermal budgets, a small offset remains. This is reflected in the residual resistance $R_{\text{res}} = R_{\text{exp}} - R_{\text{tot}}$ in Figure 5.11(b), which could point towards the influence of the interfacial

oxide. R_{res} almost vanishes for increased thermal budgets, where the oxide is significantly damaged due to pinhole formation, supporting this idea.

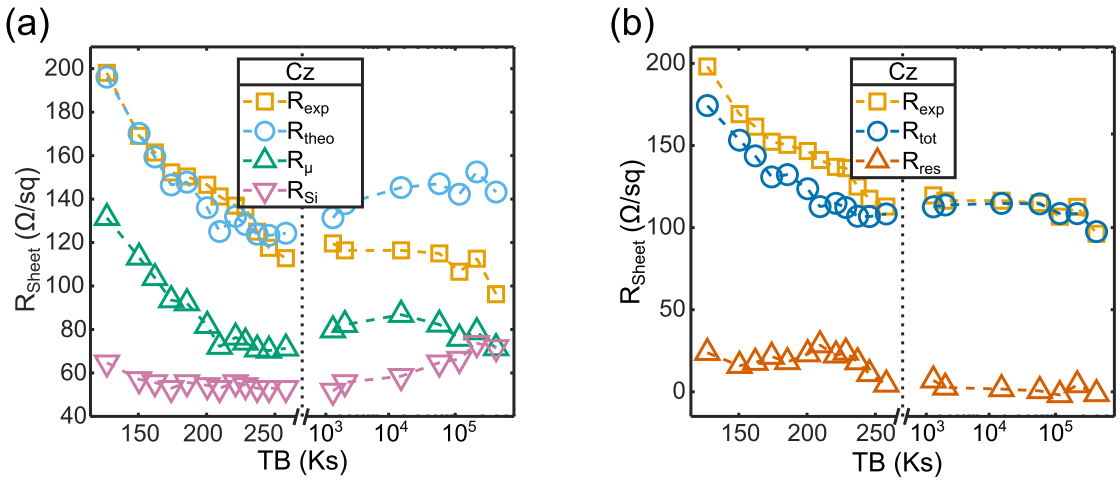

Figure 5.11.: *(a) Contributions to the measured sheet resistance R_{exp} and comparison to the theoretical calculated resistance R_{theo} in the case of (p) a-Si layers on a Cz surface. (b) Total resistance R_{tot}, calculated by considering the conduction contribution through the base, and the residual resistance $R_{res} = R_{exp} - R_{tot}$.*

It should be emphasized that these results must be interpreted with caution, as they are based on several assumptions, and the approach used to approximate base conduction involves further simplifications. To accurately describe the effects of a conductive base or multiple DT layers, simulations would be required to assess the resistivity contributions from the respective interlayer or interfacial oxides, and the c-Si base itself. However, the complexity and precision required for such simulations exceed the uncertainties involved in determining R_{theo}. Thus, this is not pursued further in this study.

5.3. Chapter Summary

This chapter investigated charge carrier transport in poly-Si based passivating contacts. The first part focused on transport through different interfacial oxides, studied via T-TLM measurements with varying low thermal budgets by adjusting both time and temperature. A transition from tunneling- to pinhole-dominated transport was observed within just a few seconds at temperatures above 800°C. In an intermediate annealing regime a combination of these mechanisms was observed and quantified through the pinhole fraction f_{P}. The timing of this transition was dependent on the oxide type, with oxide thickness being a critical factor in its stability during annealing. This shift towards pinhole transport was driven primarily by higher annealing temperatures, rather than annealing time, and was independent of the a-Si deposition technique, doping concentration, or thickness.

Pinhole formation was confirmed by removing poly-Si via TMAH and subsequent SEM imaging of the surface, where pinholes were observed with a density consistent with T-TLM evaluation, supporting the findings. Interestingly, pinholes formed already during short annealing times. This led to a comparison with the pinhole growth model proposed by Ajuria and Reif [87], which describes pinhole growth in thin oxides for long annealing times. The slow atomic diffusion process through the oxide was found to be incompatible with short high-temperature annealing, leading to the proposal of time- or temperature-dependent growth regimes, which could explain earlier oxide disruption.

Lateral transport through APCVD (p) poly-Si was also examined to relate experimental sheet resistance to microscopic parameters, such as crystallite size, grain boundary barrier height, and charge carrier concentration, for different thermal budgets. T-Hall measurements were used to determine the charge carrier mobility μ, which was evaluated using Seto's model, fitting the data to the relation $\mu = ax^b \exp(-cx)$ [115]. Instead of the expected $\mu \propto T^{1/2}$ dependence, a $\mu \propto T^{1/3}$ relationship was observed, likely due to higher doping concentrations and the broader measured temperature range. The barrier height V_B was found to be approximately 3 meV and mostly independent of the thermal budget. Consequently, the trap density at the grain boundaries Q_t was mainly influenced by the doping concentration, which decreased with higher thermal budgets, yielding values from 5.5 $\cdot 10^{12}$ cm^{-2} to 3.5 $\cdot 10^{12}$ cm^{-2}. Finally, the fit parameter a was related to the XRD crystallite size with an experimental scale factor of $f \approx 0.1$, consistent with literature reports [115, 117].
The experimental 4PP sheet resistances were correlated with theoretical values, where the resistances within the poly-Si crystallites and grain boundaries were considered in series. A good agreement was achieved for fused silica substrates, where charge transport is confined to the poly-Si layer. This process was repeated for (p) poly-Si on Cz substrates on a chemically grown oxide. Using fit parameters obtained from FS bases, good agreement was found at lower thermal budgets, though discrepancies remained at longer annealing times. These were attributed to the resistive contribution of the interfacial oxide and the in-diffused region. A simple parallel circuit equivalency between the poly-Si and the in-diffused region provided good agreement with experimental data, although a small deviation persisted.

6. Screen-Printing for Fired Passivating Contacts

Up to this point the investigation has focused on poly-Si properties, passivation, and charge carrier transport under different thermal budgets. For application in passivating contacts, the poly-Si layers must be electrically contacted. In this study, Ag screen-printing is employed after the deposition of a SiN_x layer, aligning with industrial standards. To streamline the production process, the annealing step prior to SiN_x deposition is omitted, reducing the number of processing steps. This chapter focuses on the implementation of the fired passivating contact (FPC) concept, with particular focus on variations in firing temperature after screen-printing. Section 6.1 investigates contact formation for poly-Si multilayers for different number of drive-throughs, while Section 6.2 explores modifications of the interlayer oxide.

6.1. Contact Formation for Poly-Si Multilayers

This section focuses on (p) a-Si, as there is more meaningful potential for improvement compared to (n) a-Si, which is right now mostly used in industry [17]. To evaluate the contact properties after metallization, parameters such as the contact resistivity ρ_C, saturation current density without metallization $J_{0,Pass}$, and current density after metallization $J_{0,Met}$ were measured. These parameters were then evaluated following the methodology outlined in Sections 3.1.2 and 3.3.3. The contact mechanism was further investigated via SEM imaging after sample preparation via ion-milling. Multiple DT through the APCVD system were employed to vary the thickness of poly-Si layers. While this method has already been explored for HTPC (n) a-Si [17], contact formation may differ in key aspects due to the omitted crystallization step.

Since many solar cell concepts incorporate textured surfaces, Section 6.1.1 will analyze contact formation on such surfaces. This is followed by a comparison with planar substrates in Section 6.1.2. The effect of a different interfacial oxide on contact properties is briefly examined in Section 6.1.3.

6.1.1. Textured Surface

In this section, the (n) c-Si base was treated with an alkaline texture before growth of a $T_{1.9}$ interfacial oxide. The oxide thickness was not measured on textured substrates and the reported thickness corresponds to measurements taken on a polished base using ellipsometry. Following oxide growth, APCVD (p) a-Si layers of varying thicknesses (60, 120, and 180 nm) were deposited on both sides by driving multiple times through the APCVD System (1–3DT). Additionally, a reference crystallization process at 920°C was also performed for the 2DT layers. Contacts were realized with the TLM and $J_{0,\text{Met}}$ screen (Section 2.5.2) and TLM measurements were evaluated with the 1D model due to the relatively thick oxide and opposite base polarity. Furthermore, lifetime samples were fabricated and fired at the same temperatures to obtain $J_{0,\text{Pass}}$. The following results have been largely published in [104], where all major aspects of the work were carried out by the author, including experimental design, data collection, analysis, and manuscript writing.

Surface Passivation and Contact Resistivity

To assess the quality of $J_{0,\text{Met}}$ values, passivation in the non-metallized region ($J_{0,\text{Pass}}$) is presented in Figure 6.1(a) after firing. A trend of decreasing $J_{0,\text{Pass}}$ values with increasing firing temperatures is observed across all thicknesses, with thinner layers showing lower current densities, particularly at lower firing temperatures. A lowest $J_{0,\text{Pass}}$ of 18 fA/cm^2 is reached at 890°C for 1DT. This temperature dependence is comparable to the one observed on planar substrates. Hydrogen diffusion was speculated to be critical to explain the temperature and thickness dependence on planar samples, which likely also applies for textured base substrates. However, an exact comparison can not be conducted due to possible differences in processing parameters, such as SiO_x and a-Si thickness or doping. In literature, passivation on textured surfaces has been reported to typically be worse than on planar ones [62, 290]. This is often attributed to a higher density of interface states on (111) surfaces compared to (100) surfaces [291, 292], as well as an expected reduction in interfacial oxide growth on textured surfaces [293]. During extended annealing, increased pinhole formation and boron diffusion may occur [258], particularly since pinholes tend to form at the vertices of inverted pyramids [294]. As boron diffusion is often a limiting factor for passivation in (p) a-Si contacts, increased pinhole formation on textured surfaces can further degrade passivation. However, due to the limited thermal budget of the FPC approach, passivation is not significantly impacted by boron in-diffusion, although pinhole formation may still occur during firing. Achieving high passivation levels relies heavily on an effective hydrogenation step to passivate defects at the c-Si/SiO_x/poly-Si interface.

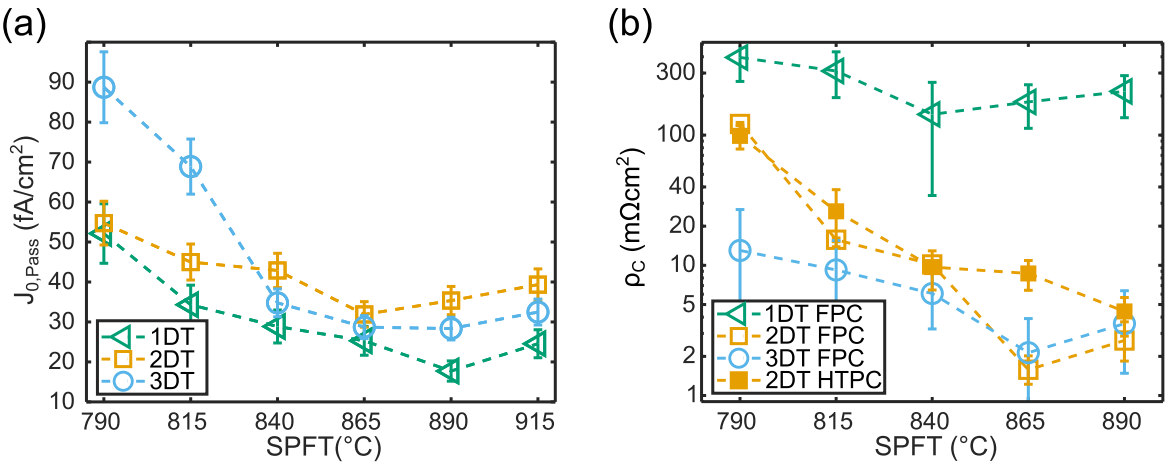

Figure 6.1.: *(a) $J_{0,Pass}$ values after firing for different thicknesses on textured surfaces. (b) ρ_C for different thicknesses and firing temperatures [104].*

Contact resistivities after screen-printing with the TLM screen are shown in Figure 6.1(b). A single drive-through results in very high contact resistivities at all firing temperatures, which can only be measured imprecisely. Increasing the number of drive-throughs leads to lower contact resistivities, especially at higher firing temperatures. For the 2DT layers, ρ_C decreases from approximately 100 mΩcm^2 at 790°C to around 2 mΩcm^2 at 865°C and 890°C. For 3DT, the contact resistivity is reduced even further at lower firing temperatures compared to 1DT and 2DT. This reflects trends observed for sheet resistances on planar substrates (Figure 4.11). Additionally, comparing FPC to HTPC samples for 2DT layers reveals a higher contact resistivity at elevated firing temperatures. An even higher ρ_C was observed in the case of an increased doping concentration for crystallized APCVD (p) a-Si layers in [17], possibly due to formation of a boron-rich layer, which negatively impacts contact formation [169]. Next, these results are analyzed on a microscopic scale using SEM cross-section images after ion-milling.

SEM Images

A high contact resistivity at lower firing temperatures for multiple DT layers can be explained by observations in Figure 6.2(a), where a cross-section of a 2DT a-Si layer is shown after firing at 815°C. In this image, very few Ag crystallites are visible within the poly-Si, reducing the available contact area between the Ag crystallites and the highly doped poly-Si. In contrast, at a higher SPFT of 890°C, large portions of the poly-Si layer are occupied by Ag crystallites, as exemplified in Figure 6.2(b) and at a larger magnification in Figure 6.2(c). Particularly in the pyramid valleys, the Ag crystallites are primarily located within the poly-Si layer and generally appear to stop at the interfacial oxide.

The cuboidal shape of the Ag crystallites corresponds with the poly-Si crystallites observed in HF-SEM images (Figure 3.6) and TEM studies for crystallized APCVD (n) a-Si layers [103]. This suggests that the contact formation mechanism is similar for both (n) and (p) a-Si, as well as between the HTPC and FPC approaches. However, a key difference for FPC (p) a-Si samples is that the Ag crystallites do not always stop at the interlayer oxide, located in-between poly-Si layers. While some Ag crystallites stop at the oxide, numerous instances of Ag crystallite penetration through the interlayer oxide into the lower poly-Si layer are visible, as evidenced in Figure 6.2(c). The corresponding larger contact area between Ag crystallites and poly-Si could further reduce ρ_C and explain the observed trends in contact resistivity. At the pyramid tips, etching behavior may vary, as seen through the formation of smaller Ag crystallites in Figure 6.2(c). In some cases, these crystallites partially extend into the c-Si base, further reducing ρ_C. Another factor contributing to the lower contact resistivity for FPC samples compared to HTPC samples is the generally higher doping concentration in poly-Si for FPC. This is due to the lack of dopant in-diffusion into the base through the omitted annealing step.

This effect can be explained using the Schottky contact model between metal and semiconductor, where the theoretical contact resistivity strongly depends on the doping concentration [163]. In the highly doped poly-Si layer ($> 1 \cdot 10^{20}$ cm^{-3}), conduction occurs primarily through field emission, resulting in very low contact resistivity between the Ag crystallites and poly-Si. However, when the doping concentration is lower, such as in the in-diffused region, ρ_C increases by multiple orders of magnitude [158]. For HTPC APCVD (n) a-Si samples, poly-Si at the pyramid tips has been observed to be etched away, leading to contact between the Ag crystallites and the lower doped c-Si base, which can increase ρ_C [17].

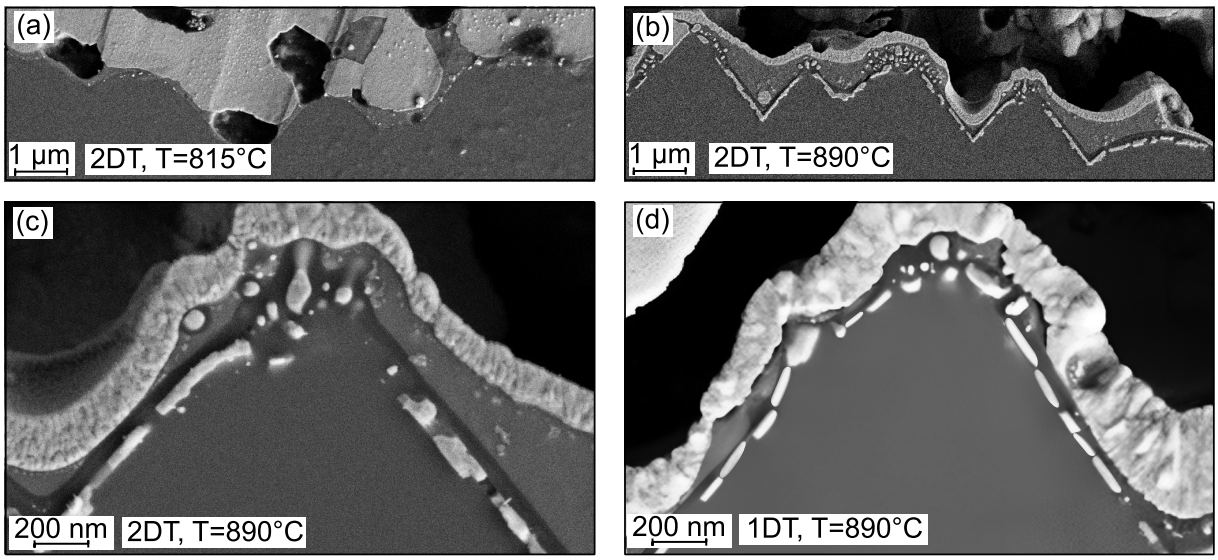

Figure 6.2.: *SEM cross-section images after ion-milling for 2DT layers at (a) 815°C and (b)-(c) 890°C, as well as (d) 1DT for an SPFT of 890°C [104].*

Similar explanations may apply for the high contact resistivities observed for the 1DT layer. The contact area between poly-Si and Ag crystallites is expected to be reduced due to the limited a-Si thickness. However, a very high density of Ag crystallites is observed for the 1DT layer at 890°C, as shown in Figure 6.2(d), suggesting a comparably larger contact area. Similar observations of increased Ag crystallite formation have been found in [17, 161, 163] for crystallized (p) and (n) a-Si layers. It has been speculated that in very thin poly-Si layers, the Ag paste etching may be modified. This could lead to the removal of most of the poly-Si during the etching process, significantly reducing the contact area between highly doped poly-Si and Ag crystallites, leaving the contact primarily with the lowly doped base. In cases where direct contact is made with the c-Si base, contact resistivity is expected to be higher for FPC compared to HTPC samples due to the lack of significant in-diffusion for FPC samples.

Passivation after Metallization

Next, the passivation quality under the metal contacts was assessed via TRPL imaging and corresponding $J_{0,\text{Met}}$ determination. The passivation quality significantly degraded across all thicknesses and firing temperatures. Particularly at larger metal fractions of 7% and 21%, the high uncertainty in the TRPL fit prevented accurate determination of $\tau(\Delta n_{\text{avg}})$ using the fit approach introduced in Section 3.1.2. However, $J_{0,\text{Met}}$ could be roughly estimated by calculating Δn_{avg} from the TRPL lifetime τ, and applying Equation (3.4) to obtain the iV_{OC} in the metallized areas [17]. These values were then used to estimate J_0 via the one-diode model in Equation (2.1). Repeating this procedure for different metal fractions, a linear fit was applied to determine $J_{0,\text{Met}}$.

Using this method, $J_{0,\text{Met}} > 5000$ fA/cm^2 was estimated for all samples, which is several orders of magnitude higher than $J_{0,\text{Pass}}$. These elevated current densities can be attributed to the high density of Ag crystallites within the poly-Si layer, many of which are in contact with the SiO_x and potentially the c-Si base. This is particularly detrimental to passivation due to the lack of dopant in-diffusion in the FPC concept. As a result, the relative impact of deep-level defects or trap states within the band gap caused by metal contamination becomes more pronounced.

Consequently, employing the FPC approach on textured surfaces proves challenging due to significant passivation losses in metallized areas. Although some solar cell concepts utilize poly-Si based contacts on textured surfaces, the full area passivating contact is more commonly integrated on planar surfaces as back contacts to minimize parasitic absorption (Figure 2.3). Contact formation on planar surfaces will be explored in the next section.

6.1.2. Planar Surface

Similar to the previous section, (p) a-Si was deposited through a varying number of drive-throughs (2-5DT) onto a 10 Ωcm (n) c-Si base with a $T_{1.9}$ oxide. The deposition parameters remained unchanged, resulting in 80 nm thick layers for every single DT. The same processing steps as outlined in the previous section were followed, where ρ_C and $J_{0,Met}$ were measured, and SEM imaging was conducted to support the analysis.

Contact Resistivity and SEM Images

Contact resistivities are shown in Figure 6.3(a), where a decreasing ρ_C is observed at higher firing temperatures for all layer thicknesses. Additionally, increasing the number of DT further reduces ρ_C, particulary at lower SPFTs. A minimum contact resistivity of approximately 2 mΩcm^2 is found for 5DT at 915°C, similar to those observed on textured surfaces.

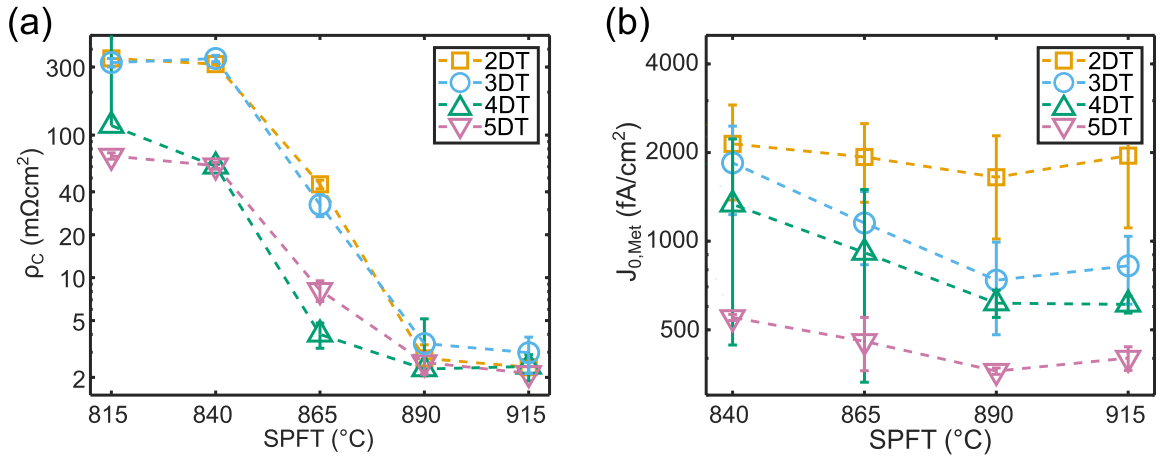

Figure 6.3.: *(a) Contact resistivities ρ_C and (b) saturation current density $J_{0,Met}$ values for different numbers of drive-throughs at various SPFT on (n) c-Si planar surfaces.*

SEM images in Figure 6.4 reveal that increasing the firing temperature, for example from 840°C in Figure 6.4(a) to 890°C in Figure 6.4(b) for 4DT, results in a higher density of Ag crystallites within the poly-Si layer. At lower temperatures, fewer Ag crystallites are observed, which are also primarily confined to the top layer. This crystallite distribution helps to explain the higher contact resistivities for lower temperatures. The larger density of Ag crystallites at higher temperature is partly due to an increased temperature-dependent etching reaction. Additionally, the etching process is of electrochemical nature and depends on the number of charge carriers available during firing. This effect is particularly evident when screen-printing is done on intrinsic (i) a-Si, where a significantly reduced carrier density in

the a-Si is present due to missing dopants. An exemplary SEM image is shown in Figure 6.4(d) for a 4DT (i) a-Si stack. Instead of large crystallites, smaller Ag crystallites are scattered throughout the entire layer. This demonstrates a significantly different behavior compared to doped a-Si layers, where larger Ag crystallites tend to form.
The decreasing contact resistivity for thicker layers at lower SPFTs may be partially related to a lower sheet resistance in thicker layers (Figure 4.11). When sheet resistance is very high, it becomes more difficult for the current to spread laterally within the poly-Si layer, causing an increased voltage drop at the contact interface, effectively raising ρ_C. Furthermore, by increasing the number of DT, the available contact area is enhanced, as long as the Ag crystallites do not stop at the interlayer oxide. In some cases, Ag crystallites are found to stop at the $SiO_{x,inter}$ layer, as shown in Figures 6.4(b) and (c). However, at higher temperatures this occurs less frequently. Furthermore, it is important to consider that these 2D cross-sections represent a 3D structure. For instance, in Figure 6.4(b), seemingly separated Ag crystallites are visible in the third layer from the top. It is likely that these crystallites are connected to the top Ag crystallites through the dimension not visible in this image.
While stopping of Ag crystallites at the interlayer oxide $SiO_{x,inter}$ is observed only occasionally, the interfacial oxide SiO_x remains a stable barrier, even at high temperatures. This is evident in Figure 6.4(c) for 2DT, where Ag crystallites do not penetrate through the interfacial oxide into the base.

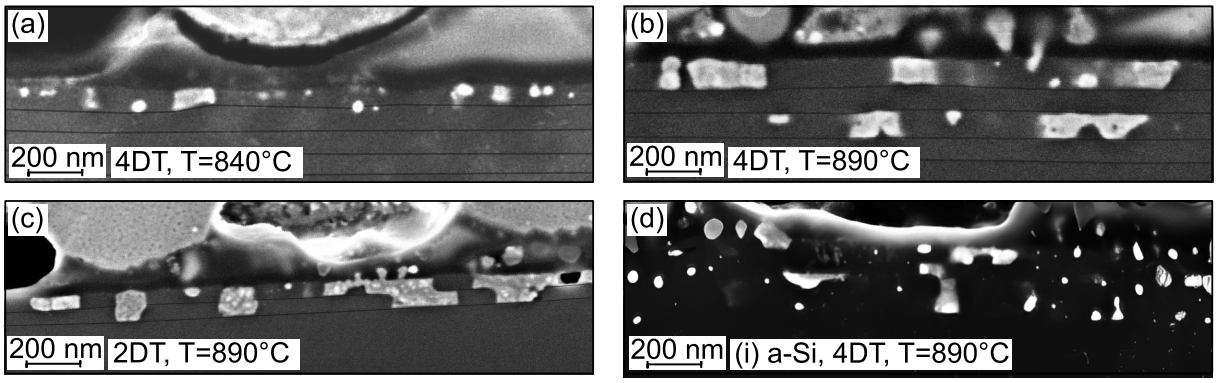

Figure 6.4.: *SEM cross-sections after ion milling for (a) 4DT layers at an SPFT of 840°C and (b) 890°C, as well as (c) a 2DT layer at 890°C on planar surfaces. (d) A 4DT intrinsic a-Si layer after contact formation is shown following firing at 890°C SPFT.*

Similar thickness-dependent contact resistivities ρ_C have been reported for crystallized LPCVD (p) a-Si using Ag/Al pastes, with a slightly higher minimum ρ_C of approximately 3 $m\Omega cm^2$ [163]. Padhamnath et al. noted that the theoretically calculated minimum contact resistivity $\rho_{C,theo} < 0.001$ $m\Omega cm^2$ is much smaller than typical experimentally measured values [163]. If Ag or Al crystallites were to penetrate into the c-Si base, variations in doping concentration can even lead to increased ρ_C, as discussed in Section 6.1.1. On the other hand, in this study the Ag crystallites remain confined within the poly-Si layer. Thus, other

factors contributing to an increase in the experimental contact resistivity compared to the theoretical value can be identified. These arise mostly from the transport of charge carriers from Ag crystallites to the Ag finger bulk, already discussed in Section 2.5.3.
One key mechanism is direct transport between the Ag finger and the crystallites, which depends strongly on the Ag crystallite size and distribution. A more homogeneous distribution generally improves contact properties. Similarly, larger crystallites, like the ones observed in SEM images in Figure 6.4, enhance charge carrier transport through the poly-Si [163]. However, overly large crystallites that extend beyond the poly-Si layer can degrade passivation. Another potential resistive contribution comes from the non-conductive glass frit [147], although optimizing the paste can reduce this effect. Some studies have even suggested that the glass frit plays an insignificant role in Ag-Al pastes on boron-diffused emitters [295, 296]. Whether these findings apply to (p) a-Si layers in poly-Si passivating contacts remains unclear, as the specific composition of the paste plays a key role in its resistivity contribution.
Given the similar etching behavior between FPC and HTPC samples, the lower contact resistivity for FPC samples is likely due to the increased contact area between Ag crystallites and the highly doped poly-Si. This could be due to an increased etch reaction of the paste with the FPC a-Si layers compared to the well-crystallized poly-Si layers produced via the HTPC route. Additionally, interlayer oxides in APCVD a-Si layers may contribute to a higher contact resistivity, especially if Ag crystallites stop at these oxides. This can potentially also contribute to the higher contact resistivity observed in HTPC samples compared to FPC samples due to the missing reliable etch stop for the FPC approach.
When comparing ρ_C values on planar surfaces to textured surfaces in Figure 6.1, contact resistivities are noticeably higher at lower temperatures on planar substrates, requiring a higher SPFT to achieve low ρ_C. This difference may be partly attributed to the lower measured peak temperatures on planar surfaces compared to textured ones (Figure 2.10), with discrepancies of up to 20°C. Additionally, the slower heat-up rate affects the overall firing profile, potentially promoting increased Ag crystallite formation during firing. Differing wetting properties of the paste on textured surfaces may also contribute to this deviation.

Passivation after Metallization

In addition to minimizing contact resistivity, maintaining low surface passivation is crucial for integrating poly-Si layers into solar cell devices. To assess the impact of metallization on passivation, $J_{0,\text{Met}}$ values are presented in Figure 6.3(b), revealing several key observations. Firstly, these values are notably lower than those observed for textured surfaces. However, despite being reduced, the current densities remain at least an order of magnitude higher

than their non-metallized counterparts. Secondly, $J_{0,\text{Met}}$ decreases with increasing SPFT, mirroring the trend seen in non-metallized samples. For lifetime samples, this improvement at higher firing temperatures has primarily been attributed to hydrogenation, which is likely the same mechanism at play here. Thirdly, Figure 6.3(b) highlights a clear dependence on the number of drive-throughs. Generally, thicker poly-Si layers enhance passivation by reducing the likelihood of Ag crystallites contacting the c-Si base, consistent with previous studies [17, 163]. The lowest $J_{0,\text{Met}} \approx 350$ fA/cm^2 is achieved for the 5DT sample at 890°C, a value significantly lower than those reported previously for the FPC concept [178, 179].
In contrast, for 2DT layers the passivation shows less improvement with higher firing temperatures compared to the results for more drive-throughs. This is likely due to a larger number of Ag crystallites making contact with the base, visible in Figure 6.4(c), introducing defects that offset the passivation benefits of hydrogenation at higher firing temperatures. For thicker layers, Ag crystallites are more likely to remain confined within the poly-Si layer, thereby preserving passivation. A decline in passivation is only observed at very high firing temperatures, possibly due to excessive Ag crystallite formation or even hydrogen-induced damage [255, 256].
In addition to Ag crystallites contacting the base, another factor potentially limiting passivation could be the diffusion of silver atoms through the poly-Si and SiO_x layers into the c-Si base. This will be discussed in detail in Section 6.2.2.

6.1.3. Effect of Interfacial Oxide

This section aims to briefly examine the influence of varying the interfacial oxide for screen-printing. Firstly, the surface passivation after metallization and the contact resistivity is compared between a chemical ($P_{1.5}$) and thermal ($T_{1.9}$) oxide. This is done because the $T_{1.9}$ oxide does not allow for significant charge carrier transport through the oxide (Section 5.1), which is important for implementation in solar cells. To accurately assess the influence of transport through the base on contact resistivity, this experiment was conducted on a Ga-doped (p) c-Si base. Secondly, the charge carrier transport through the base is investigated for the $P_{1.5}$ oxide by removing the poly-Si in-between the fingers. All investigations in this section used an APCVD (p) a-Si layer with a 5DT stack (each with a thickness of approximately 80 nm). This was chosen to reduce the likelihood of direct contact between Ag crystallites and the c-Si base, which could degrade passivation.

Surface Passivation and Contact Resistivity

Figure 6.5(a) shows $J_{0,Pass}$ and $J_{0,Met}$ values for (p) a-Si at different firing temperatures. Instead of a p-type base, for TRPL measurements an n-type base (10 Ωcm) was used to achieve a high injection state. $J_{0,Pass}$ values decrease from about 100 fA/cm^2 at low temperatures to below 30 fA/cm^2 at the highest firing temperatures. Lower $J_{0,Pass}$ values may be possible by selecting a base material with a higher doping concentration.
After metallization, $J_{0,Met}$ is higher when using the $P_{1.5}$ oxide compared to the $T_{1.9}$ oxide. This may be due to possible contact of Ag crystallites with the interfacial oxide. Although direct contact of Ag crystallites with the interfacial oxide is rarely observed in SEM images, it cannot be ruled out. Such a contact could be more detrimental to passivation when using a thinner oxide, as its thermal instability during firing can lead to Ag crystallites contacting the underlying base. Another possible factor could be Ag diffusion into the base, which will be discussed in more detail in Section 6.2.2. Nonetheless, it is evident that varying the oxide does not significantly improve the passivation behavior after metallization, and a different approach will be explored in Section 6.2.

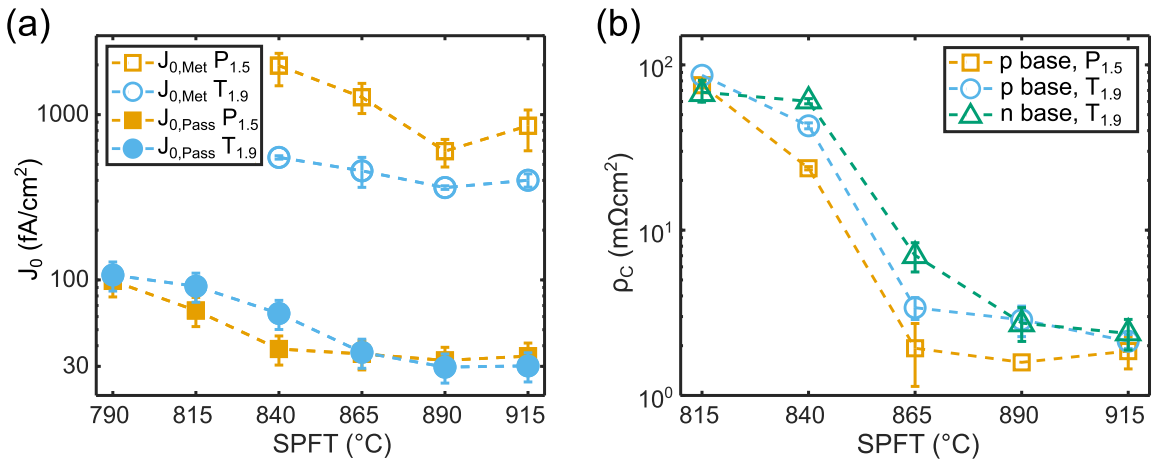

Figure 6.5.: *(a) Surface passivation without metallization ($J_{0,Pass}$) and after metallization ($J_{0,Met}$) for $P_{1.5}$ and $T_{1.9}$ interfacial oxides for 5DT (p) a-Si layers. (b) Contact resistivity ρ_C for 5DT (p) a-Si on two different oxides on Ga (p) c-Si base, compared to values on (n) c-Si base with a $T_{1.9}$ oxide.*

In addition to J_0, Figure 6.5(b) shows the contact resistivity on a (p) c-Si base for the $P_{1.5}$ and $T_{1.9}$ oxides. These are compared to results on (n) c-Si base from the previous section. It can be observed that the different bases generally exhibit similar behavior for the $T_{1.9}$ oxide across all temperatures, with only slight deviations. In contrast, the $P_{1.5}$ oxide results in a reduced ρ_C, particularly at higher firing temperatures, with a minimum of 1.6 mΩcm^2. Two factors contribute to this observation. Firstly, as discussed in Section 2.4.3, firing temperatures on Ga-doped bases tend to be slightly higher than on P-doped bases, leading

to minor deviations in ρ_C. However, this effect alone cannot explain the difference between the $P_{1.5}$ and $T_{1.9}$ oxides. Secondly, for the $P_{1.5}$ oxide on a (p) c-Si base, charge carrier transport through the base may occur through tunneling or pinhole transport, as shown in Section 5.1, further reducing ρ_C.

Transport through the Oxide

To verify whether the same mechanism is at play in these samples as in Chapter 5, T-TLM measurements were conducted on a 5DT screen-printed (p) a-Si with a $P_{1.5}$ oxide after removing poly-Si between the 60 µm thick fingers via saw dicing to allow charge carrier transport through the base. Examples of two measurements with corresponding fits are shown in Figure 6.6(a) after firing at 840°C and 915°C.

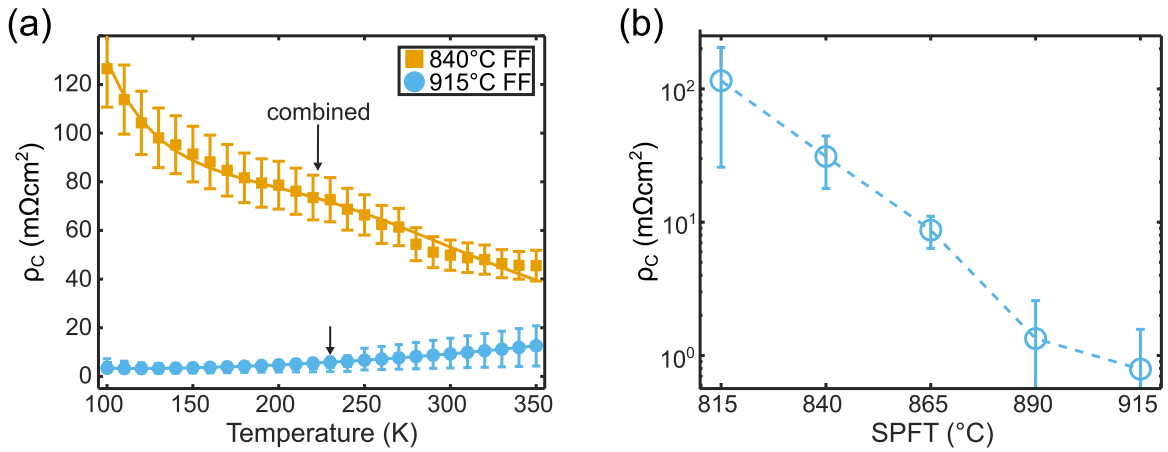

Figure 6.6.: *(a) Examples of T-TLM measurements for Ag screen-printed contacts after firing at SPFT of 840°C and 915°C and removal of the poly-Si in-between the fingers via saw dicing. (b) Oxide contact resistivity for different firing temperatures after poly-Si removal.*

A decreasing ρ_C is visible with higher measurement temperatures for firing at 840°C, which is best described using the combined model. A relatively low pinhole density of $N_P \approx 1 \cdot 10^5$ cm^{-2} and pinhole fraction $f_P = 0.23$ was found, indicating that transport is predominantly dominated by tunneling. A tunneling mass of 0.3 m_e and $\Delta E_S \approx 14$ meV was found. These values differ slightly to those found for evaporated contacts on (n) a-Si in Section 5.1. A key difference to (n) a-Si is the higher reported barrier height of 4.8 eV for tunneling through SiO_x, compared to 3.1 eV for (n) a-Si [77]. This higher barrier can result in a larger effective tunneling mass and correspondingly an increased resistance contribution. Therefore, creating pinholes in the oxide is even more important to promote charge carrier transport to the base for (p) a-Si compared to (n) a-Si.

For the sample fired at 915°C, the temperature dependence is best described by pinhole

transport, with a higher pinhole density of about $3 \cdot 10^7$ cm^{-2}. This suggests that the a-Si doping type and the contacting mechanism (evaporation compared to screen-printing) does not significantly alter the charge carrier transport characteristics through the oxide. A similar transition from tunneling- to pinhole-dominated transport is found in both cases.
The influence of firing temperature on oxide contact resistivity is also illustrated in Figure 6.6(b), where oxide contact resistivities after poly-Si removal between metal fingers are shown. Notably, a higher SPFT significantly reduces the oxide contact resistivity. This is related to the shift in the transport mechanism from tunneling- toward pinhole-dominated transport, where the oxide contact resistivity typically is lower.

6.2. Different Interlayer Oxides

In Section 6.1, low contact resistivities were achieved using the multiple drive-through approach. While surface passivation was able to be improved down to approximately 350 fA/cm^2, further improvements are necessary for implementation in solar cells to compete with the HTPC approach. One possible strategy could be to increase the number of DT further. However, this would significantly extend the total deposition time, which is not ideal for industrial applications. Furthermore, a thicker layer leads to enhanced parasitic absorption, degrading cell performance. This section aims to investigate whether a stopping effect of Ag crystallites can be achieved for the FPC approach by introducing an artificially grown interlayer oxide between just two poly-Si layers.
To this end, the process flow was modified by growing two different oxides (thermal $T_{1.9}$ and chemical $P_{1.5}$) onto an (n) c-Si base for $J_{0,\mathrm{Met}}$ determination and a (p) c-Si base for ρ_C determination. A 130 nm thick APCVD (p) a-Si layer was then deposited. Subsequently, two different oxides (thermal and chemical) were grown on top of the poly-Si layer, using the same parameters as those used for the c-Si base. However, the thickness of a-Si layers may vary when growing oxides on amorphous or polycrystalline materials, as oxide growth is often less homogeneous and thinner in the grain boundary regions [297]. Furthermore, the properties of the oxide depend strongly on doping, which can result in thinner oxides [298]. As precise thickness determination for these thin layers on top of poly-Si is challenging, these interlayer oxides are simply referred to as thermal T or chemical P to distinguish them from the interfacial oxides $T_{1.9}$ and $P_{1.5}$.
After the second oxide has been grown, an additional APCVD (p) a-Si layer was deposited on top. In addition to all oxide combinations for FPC samples, HTPC samples using the $T_{1.9}$ oxide were prepared by crystallizing at 920°C for 30 min. SiN_x was deposited, followed by Ag screen-printing and firing at SPFT temperatures between 840°C and 915°C, as lower

temperatures have been shown to result in insufficient contact formation.
Section 6.2.1 analyzes contact resistivities, while Section 6.2.2 investigates the barrier effect through SEM images and passivation values, along with a discussion of passivation-limiting factors. Finally, Section 6.2.3 briefly explores the potential for integrating the FPC concept into solar cells using a simulation tool.

6.2.1. Contact Resistivity

Contact resistivities are shown in Figure 6.7(a) for FPC and HTPC samples utilizing the $T_{1.9}$ oxide. It is observed that higher firing temperatures lead to a decrease in ρ_C for all oxide combinations, reaching down to 3 mΩcm^2 at 915°C for the $T_{1.9}$-T oxides in the case of the FPC approach. While this is slightly higher than with the native interlayer oxide (Figure 6.3), it is still relatively low for (p) a-Si screen-printed contacts. HTPC samples generally exhibit higher contact resistivities than FPC ones, in accordance with the results for native interlayer oxides (e.g., Figure 6.1). Furthermore, the $T_{1.9}$-T oxides result in lower contact resistivities compared to the $T_{1.9}$-P oxides for HTPC and FPC samples. This may be attributed to the additional thermal budget introduced during thermal oxidation, which could affect the properties of the lower a-Si layer similarly to low temperature annealing by increasing crystallinity without promoting heavy dopant in-diffusion [299]. Consequently, this also may influence the interlayer oxide growth and impact contact formation.

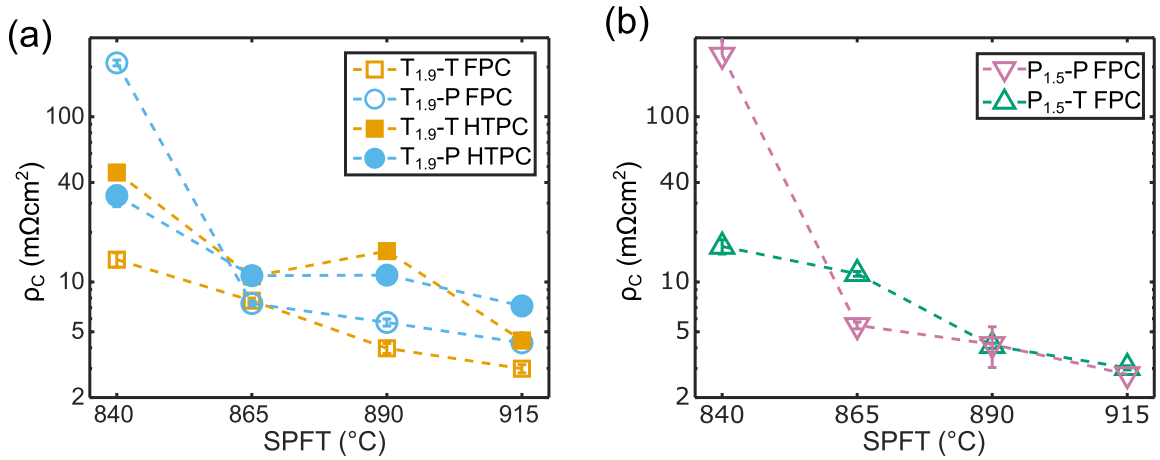

Figure 6.7.: *Contact resistivities as a function of firing temperature for the (a) $T_{1.9}$ oxide in the case of FPC and HTPC samples and the (b) $P_{1.5}$ oxide for FPC samples.*

These values are compared with those on the $P_{1.5}$ interfacial oxide in Figure 6.7(b). At lower temperatures, the contact resistivity is lower for the thermal interlayer oxide compared to the chemical interlayer oxide. While extended annealing typically leads to worse contact properties for boron-doped a-Si, these results support the hypothesis that oxidation

at 625°C acts as a form of annealing. Contact resistivities decrease continuously for both interlayer oxides, reaching values as low as ≈ 2.5 mΩcm^2 at 915°C. These values are slightly lower than those for the $T_{1.9}$ oxide, suggesting additional charge carrier transport through the base, similar to Section 6.1.3.

To investigate charge carrier transport through the base, contact resistivities were analyzed after removal of poly-Si between the fingers. However, it was not possible to evaluate the TLM data using a linear fit for these samples due to high R_{Total} values, as shown in Figure 6.8(a), where exemplary TLM measurements are shown. Instead, an evaluation following Galleni et al. [78] was performed. To obtain R_{C}, the mean value of R_{Total} was used, and ρ_{C} was calculated by solving the implicit expression found in Equation (3.24). To solve this equation, the sheet resistance R_{Sheet} is required. This was estimated by assuming no in-diffusion and using the sheet resistance of the 1.3 Ωcm Ga wafer, which corresponds to roughly 80 Ω/sq. Such an approximation is sufficient, as shown in [78], because ρ_{C} only weakly depends on the sheet resistance in the case of large contact resistances. Error bars were determined using the standard deviation of R_{Total} when solving Equation (3.24).

It should be noted that the values shown in Figure 6.8(b) only present an approximation due to the evaluation process. However, key observations can still be made.

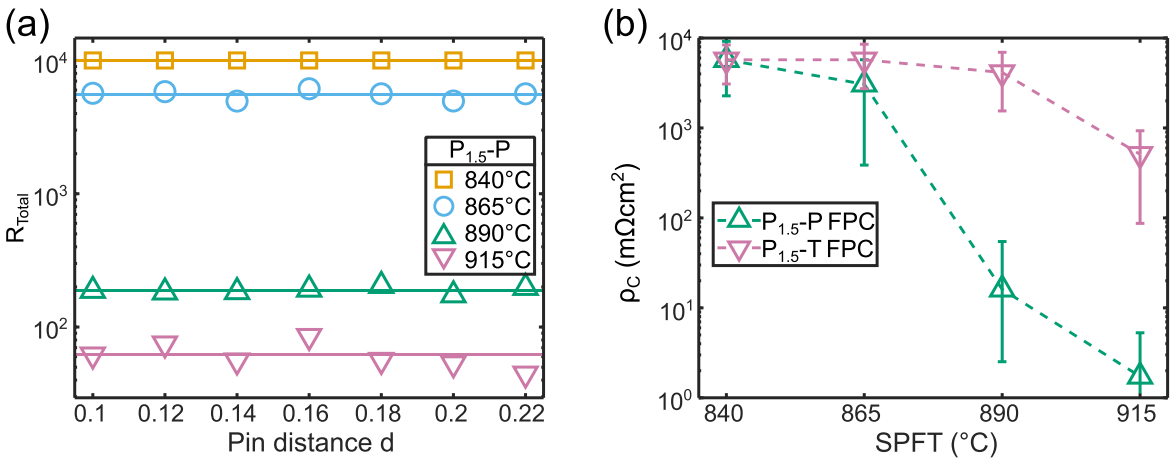

Figure 6.8.: *(a) Examples of TLM measurements for the $P_{1.5}$-P oxide combination after selective poly-Si removal via saw dicing for different firing temperatures with the corresponding mean values. (b) Oxide contact resistivity for different firing temperatures using the evaluation via averaging of R_{Total} and solving Equation* (3.24)*.*

Clearly, the oxide contact resistivity decreases with higher SPFT for both the thermal and chemical interlayer oxides. The chemical $SiO_{x,\text{inter}}$ exhibits lower resistivities particularly at higher firing temperatures. This indicates that the thickness and type of interlayer oxide influences charge carrier transport through the base similar to the interfacial oxide investigated in Section 5.1. However, in the T-TLM studies in Section 5.1, no charge carrier transport through the $T_{1.9}$ oxide was observed. In the case of the thermal interlayer oxide

in combination with the $P_{1.5}$ interfacial oxide, charge carrier transport through the base is enabled, as visible in Figure 6.8(b). Possible reasons may be differences in oxide growth on an already existing poly-Si layer or the presence of Ag crystallites in contact to the interlayer oxide. Furthermore, in comparison to Figure 6.6(b), resistivities are significantly higher, suggesting that the interlayer oxides still introduce a considerable additional resistivity contribution.

6.2.2. Investigation of Barrier Effect

In this section, the barrier effect of these artificially grown interlayer oxides is investigated, beginning with SEM imaging of the cross-section after ion-milling.

SEM Images

Figure 6.9 shows SEM images of contacts for the $T_{1.9}$ interfacial oxide after firing at 890°C. Figures 6.9(a) and (b) show FPC samples with chemical and thermal $SiO_{x,inter}$. In both cases, a clear stopping of Ag crystallites at the interlayer oxide is observed. Although SEM imaging suffers from limited sample size, no Ag crystallites were found within the bottom poly-Si layer at three separate metal fingers. Identical behavior is found for the $P_{1.5}$ interfacial oxide, which is reflected in the very similar ρ_C values.
This points to an etch stop during contact formation, as was already reported for APCVD (n) a-Si [103]. The exact mechanism behind this stop is still not fully understood, though two possible explanations have been proposed. Firstly, the influence of crystal orientation at the Ag/poly-Si interface may contribute to different Ag etching behavior. However, in [103] no clear correlation between Ag crystallite orientation and poly-Si orientation was found in TEM studies. While neighboring Si crystallites can influence Ag etching, a different poly-Si crystallite orientation would more likely lead to a reduced etch speed rather than a complete etch stop. Secondly, a more plausible explanation is the presence of the $SiO_{x,inter}$ itself, which may act as a barrier to the etching reaction (2.31). This theory is supported by the fact that artificially grown interlayer oxides produce an etch stop in FPC samples, whereas natively grown oxides do not.
These findings raise the question of how interlayer and native oxides differ from one another. Firstly, artificially grown oxides are likely thicker, which is supported by the larger oxide contact resistivities in Figure 6.7(a). Another factor may be the number of dopants within or near the oxide layer when the oxide is grown thermally or chemically instead of growth during the deposition. One can speculate that less dopants are incorporated for the samples with artificial interlayer oxides through the short chemical cleaning step and HF dip

performed before oxidation to prevent contamination. Since the etching process depends heavily on the number of charge carriers, a stronger and thicker barrier could explain the etch stop for FPC samples. Conversely, the natively grown oxide may be too thin and contain more dopants to effectively stop the etching reaction at the $SiO_{x,inter}$ in the case of the FPC approach, where no extended crystallization is applied to redistribute dopants.
Interestingly, when comparing these findings to HTPC samples with a chemical interlayer oxide in Figure 6.9(c), a different behavior is observed. Multiple instances of Ag crystallite penetration into the bottom poly-Si layer are visible, which is not the case for the thermal $SiO_{x,inter}$ in Figure 6.9(d). This difference suggests that thermal stability plays a role in the etch stop. One possibility is the formation of pinholes during annealing, which is more prevalent for the chemical interlayer oxide compared to the thermal one. In (p) a-Si, B in-diffusion has been shown to increase pinhole formation compared to phosphorus due to faster diffusion and more aggressive segregation into the oxide [98]. This presents a clear difference to APCVD (n) a-Si, where P accumulation at the interfacial oxide does not tend to damage the oxide as much. Such a mechanism could explain why stopping is observed for HTPC (n) a-Si and not for (p) a-Si. However, further investigation into the exact stopping mechanism is necessary to fully understand the microstructural interactions, which is not pursued further in the present work.

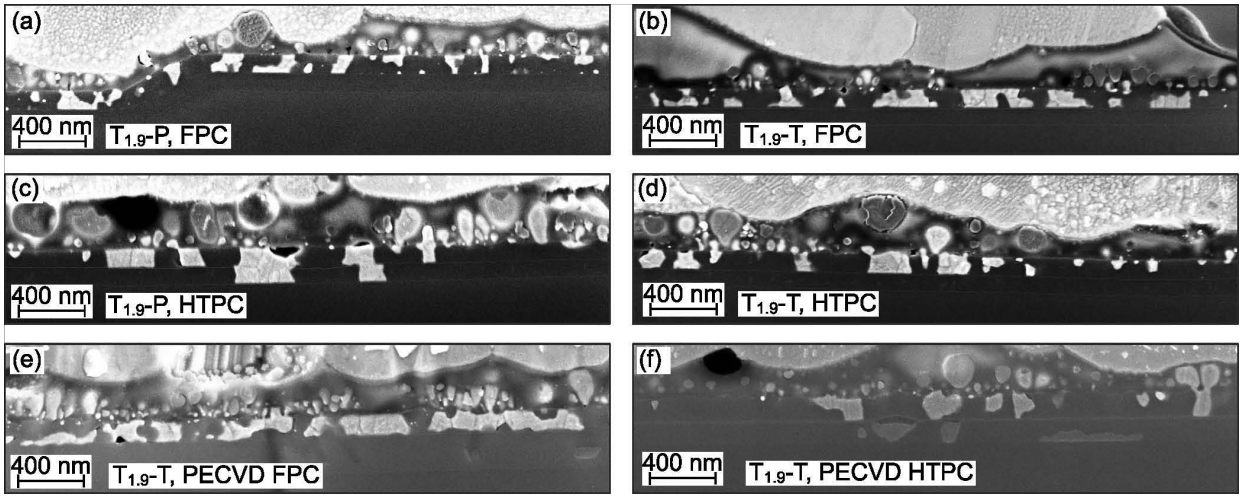

Figure 6.9.: *SEM images after ion-milling of the cross-section for the $T_{1.9}$ interfacial oxide. FPC and HTPC approaches are shown with the (a)/(c) chemical interlayer oxide and (b)/(d) thermal interlayer oxide. PECVD (n) a-Si is shown as a comparison for the thermal $SiO_{x,inter}$ in the case of (e) FPC and (f) HTPC samples.*

Another observation in Figures 6.9(c) and (d) is the larger size of Ag crystallites in HTPC compared to FPC samples. This correlation is also reflected in the poly-Si crystallite size observed in XRD measurements (see Figures 4.10 and 4.5). Generally, larger Ag crystallites are beneficial for lowering ρ_C due to an enhanced contact area, provided the Ag

crystallite formation is not excessive. Thus, the relatively large poly-Si crystallites inherent to APCVD a-Si may contribute to lower contact resistivities compared to other deposition techniques, particularly for the FPC approach with its limited thermal budget.
To compare the influence of the deposition process, a 130 nm thick PECVD (n) a-Si layer was deposited and processed similarly for the $T_{1.9}$-T oxide combination for FPC and HTPC samples. The FPC process included a short hydrogen out-diffusion step for 1 min at 700°C to prevent excessive blistering [8, 68]. Corresponding contact resistivities can be found in the Appendix A.2. For FPC layers in Figure 6.9(e), no penetration of the interlayer oxide is visible. In contrast, Figure 6.9(f) shows Ag crystallites in the bottom poly-Si layer for the HTPC approach. Similar to APCVD (p) a-Si, larger Ag crystallites are found for HTPC samples, where the shape is not cuboidal as it is for APCVD a-Si. Although the poly-Si properties vary in crystallite size, distribution, shape, and doping type, Ag crystallites stop at the interlayer oxide for FPC samples in both APCVD and PECVD a-Si cases. In contrast, HTPC samples show penetration into the bottom layer. This suggests that the stopping effect may be independent of poly-Si properties and more closely related to the crystallization step and dopant diffusion during annealing. A more detailed investigation, for instance by using high-resolution TEM imaging, would be necessary to draw firm conclusions into the importance of poly-Si crystallite structure and deposition technique onto contact formation. Finally, it should be noted that at lower temperatures, smaller and fewer Ag crystallites form, which remain confined to the upper poly-Si layer, as was already observed in Section 6.1.2. The stopping of Ag crystallites at the interlayer oxide at higher temperatures presents a key difference from the multiple drive-through approach and can significantly impact surface passivation, which will be investigated next.

Surface Passivation

In Figure 6.10(a), $J_{0,\text{Pass}}$ is shown for different SPFTs and oxide combinations in non-metallized areas on 15 Ωcm (n) c-Si base material, used to achieve high-injection state during TRPL measurements. A higher firing temperature generally leads to a lower saturation current density, consistent with previous observations for multiple drive-throughs (Figure 6.5). Some data points for HTPC are missing due to smaller sample sizes and issues during processing. The lowest $J_{0,\text{Pass}}$ of $\approx$ 20 fA/cm^2 is found for the $T_{1.9}$-T oxides, with only small deviations compared to the chemical interlayer oxide. A more significant difference is observed for the $P_{1.5}$ interfacial oxide, where a minimum of $\approx$ 45 fA/cm^2 is obtained, which is slightly higher than for the $T_{1.9}$ interfacial oxide. Due to the presumably higher defect density at the poly-Si/SiO_x/c-Si interface for chemical oxides [300], hydrogenation is typically more essential for achieving high passivation levels when chemical interfacial

oxides are used. The hydrogenation step could be impeded by the interlayer oxide, which may act as a hydrogen barrier. Consequently, this potential hydrogen barrier may have a more pronounced negative impact on passivation for the $P_{1.5}$ interfacial oxide compared to the $T_{1.9}$ interfacial oxide. It should also be noted that $J_{0,Pass}$ could be improved by using a higher-doped base with increased conductivity.

Results after metallization are shown in Figure 6.10(b). Similar to passivation without metallization, $J_{0,Met}$ decreases with higher set peak firing temperatures. The only exception is the HTPC $T_{1.9}$-T oxide, where this trend does not hold, likely because passivation is not as heavily reliant on hydrogenation for well-crystallized poly-Si layers.

Furthermore, clear trends are observed for different oxide combinations. Similar to passivation without metallization in Figure 6.10 (a), the $T_{1.9}$ interfacial oxide leads to higher passivation levels, indicated through lower $J_{0,Met}$ values. A minimum $J_{0,Met}$ of (78 ± 24) fA/cm^2 is obtained for the thermal interlayer oxide, which is even lower than values reported by Padhamnath for crystallized (p) a-Si layers. When utilizing a chemical $SiO_{x,inter}$ on a thermal $T_{1.9}$ interfacial oxide, a minimum current density of $\approx$ 180 fA/cm^2 is found.

When switching the order of oxides from $T_{1.9}$-P to $P_{1.5}$-T, the lowest $J_{0,Met}$ achieved is approximately 280 fA/cm^2. This value is still lower than those for the multiple drive-through approach, even when using 5DT (see Figure 6.3). Additionally, in comparison to the multiple DT route, this approach also allows a wider temperature range for relatively low $J_{0,Met}$ values for FPC samples. HTPC samples with a chemical interlayer oxide show worse passivation through higher surface current densities. This might be partially attributed to Ag crystallite penetration into the bottom poly-Si layer at elevated temperatures, indicated through SEM images in Figure 6.9. The reason for the low passivation level at 840°C, also observed for $J_{0,Pass}$, is unclear, but might be due to the limited sample size.

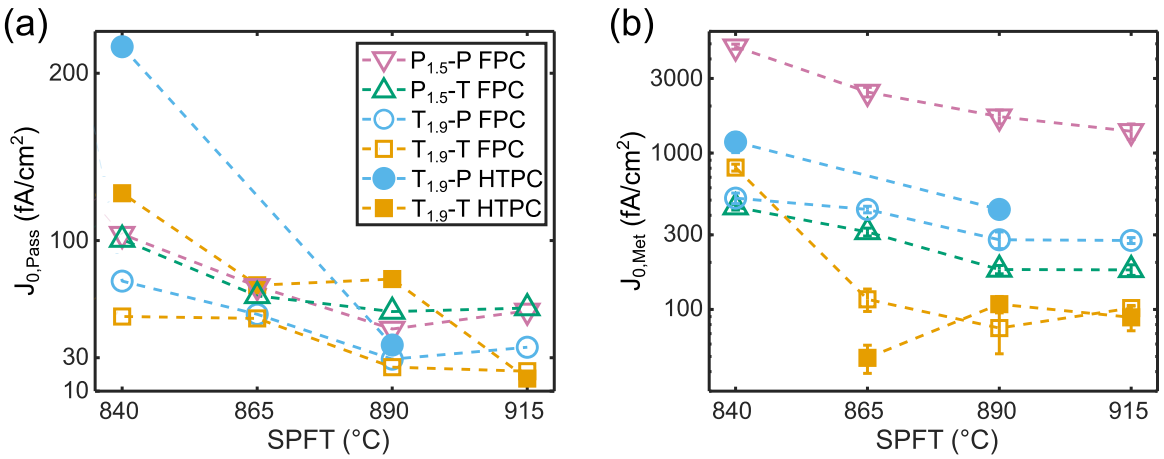

Figure 6.10.: *Saturation current density (a) $J_{0,Pass}$ and (b) $J_{0,Met}$ for different oxide combinations and firing temperatures.*

Finally, for the $P_{1.5}$-P oxide combination, a significantly higher $J_{0,Met}$ is measured, comparable to the 2DT samples in Figure 6.5. This may partially be due to the hydrogen barrier effect of the interlayer oxide being more pronounced for the $P_{1.5}$ interfacial oxide and leading to worse hydrogenation properties, even without metallization. However, compared to the $P_{1.5}$-T oxide combination, this configuration performs significantly worse after metallization. As no Ag penetration into the lower poly-Si layer is observed, other passivation-limiting factors will be discussed next.

Passivation-Limiting Factors

It becomes clear that Ag crystallites in contact with the interfacial oxide or their penetration into the base alone cannot adequately explain the observed passivation results after metallization. Two key factors likely to contribute to passivation degradation have been identified. The first one is the impact of screen-printing metallization onto the hydrogenation process. As seen in the $J_{0,Pass}$ values in Figure 6.10(a), poorer passivation is observed for the $P_{1.5}$ oxide compared to the $T_{1.9}$ oxide. This may be attributed to the presence of the interlayer oxide, as samples without it achieved comparable passivation levels in the case of a $P_{1.5}$ interfacial oxide with a native interlayer oxide (see Figure 6.5(a)). Additionally, covering a significant portion of the surface with metal paste affects the actual temperature of the sample. A higher metal fraction is suspected to lower the wafer temperature, thereby reducing the amount of hydrogen diffusing into the poly-Si. The exact temperature offset is not easily determined experimentally and may account for a slight discrepancy between the $J_{0,Pass}$ and $J_{0,Met}$ values. However, it cannot explain very high $J_{0,Met}$ results after metallization, such as in the case of the $P_{1.5}$-P oxide combination.
The second explanation involves Ag diffusion during firing. As mentioned in Section 6.1.1, defects near the SiO_x/c-Si interface can severely degrade passivation when there is limited dopant in-diffusion [301]. Even a small amount of Ag diffusion into the base can have serious consequences for passivation of FPC samples. Two diffusion pathways are typically considered. These are diffusion through the poly-Si and diffusion through various oxides, including interlayer, native, or interfacial ones. Detecting low concentrations of Ag within the c-Si base ($< 1 \cdot 10^{16}$ cm^{-3}) is below the resolution limit of GD-OES or secondary ion mass spectrometry measurements [302] and makes experimental approaches difficult to realize. However, when relying on literature, most studies focus on crystalline silicon with low doping levels and thicker oxide layers within specific temperature regimes [303–306]. Consequently, these findings may not be directly applicable to passivating contacts, where thin oxides and poly-Si layers are the critical regions to consider. Nonetheless, qualitative observations can still be relevant. To account for temperature dependence of diffusivity,

these processes are often described using Arrhenius-type relationships (Equation (2.12)), which include an activation energy and pre-exponential factor.

When considering silver diffusion in c-Si instead of poly-Si, it has been found that Ag diffuses via a combination of interstitial and substitutional diffusion, with interstitial diffusion typically dominating [303]. This explains the lower diffusivity of Ag compared to interstitially diffusing metals such as Cu, which has been mostly attributed to the mass difference between these elements [306]. Comparing these mechanisms to poly-Si, grain boundaries typically represent an additional diffusion pathway in the case of dopants such as boron or phosphorus [258, 307]. While no specific studies have been conducted on Ag diffusion in poly-Si, in cubic silicon carbide layers Ag diffusion along grain boundaries has been assumed to be the dominant mechanism [308], which may be applicable to poly-Si layers as well. If this is the case, the smaller crystallite size in FPC samples compared to HTPC samples could in fact lead to increased Ag diffusivity. A higher doping level in the poly-Si layer could also contribute to enhanced diffusivity within the crystallites due to a larger number of vacancies and interstitial defects, further increasing Ag diffusion for FPC layers.

When analyzing Ag diffusion through silicon oxides, one mostly finds studies for thick oxides ($>$ 500 nm), where a significantly lower diffusivity D than in c-Si has been found. For instance, Nason et al. reported a diffusivity of $\approx 10^{-15}$ cm^2/s at temperatures between 450-500°C, while McBrayer et al. determined an activation energy of 1.24 eV [304, 306]. In comparison, for c-Si diffusivities of $\approx 10^{-8}$ cm^2/s have been reported in a similar temperature range [303]. The corresponding diffusion length $L_\mathrm{D} = \sqrt{2Dt}$ can be calculated using Brownian motion to estimate the average diffusion length. It is important to emphasize that the diffusivity, and consequently the diffusion length, is strongly temperature-dependent due to the exponential relationship with activation energy, similar to pinhole growth in Section 5.1.2.

Finally, the role of the paste itself must be considered. If silver were in direct contact with the Si base in a traditional diffused emitter, the Ag diffusion length would be several microns during the firing cycle, even at low firing temperatures [302, 303]. The timing and temperature at which Ag begins to diffuse during the firing process is strongly influenced by the glass frit, paste composition, and the specific firing temperature and profile [17]. Thus, the role of the glass frit is essential to prevent massive Ag diffusion during firing, as diffusion from the Ag/glass solution is believed to be very limited [302]. Rather, diffusion is thought to originate mainly from the Ag crystallites formed during the cool-down phase of the firing cycle at lower temperatures. Consequently, the earlier Ag recrystallizes, the higher the temperature at which diffusion begins. Due to the strong temperature dependence for diffusion, this significantly impacts the diffusion length of Ag in poly-Si and especially in SiO_x.

Using values from [303, 304, 306] and assuming similar diffusivity between poly-Si and c-Si,

the diffusion length for a typical firing profile (e.g., Figure 2.10) can be estimated based on the temperature at which diffusion begins. For instance, with a diffusion start temperature of 500°C during the cool-down phase, the diffusion lengths are $L_{\text{poly-Si}}(500°\text{C}) \approx 10$ µm and $L_{\text{SiOx}}(500°\text{C}) \approx 23$ nm. At a lower start temperature of 400°C, these lengths are reduced to $L_{\text{poly-Si}}(400°\text{C}) \approx 3$ µm and $L_{\text{SiOx}}(400°\text{C}) \approx 6$ nm, highlighting the importance of the diffusion start temperature for Ag diffusion. Although the diffusivities used in these calculations may differ significantly from those applicable to the thin oxides studied here, this demonstrates the interlayer oxide's potential to act as an effective barrier against Ag diffusion, in addition to its role as an etch stop for metallization.

To gain further insight into the effect of different interlayer oxides, boron doping profiles are shown in Figure 6.11 through ECV measurements across various oxide combinations. For 2DT layers, no significant dip is visible between drive-throughs. In contrast, a pronounced decrease in the doping profile is observed for the chemical interlayer oxide, and even more so for the thermal oxide. This difference may account for the enhanced surface passivation achieved with the interlayer oxide approach and the generally lower $J_{0,\text{Met}}$ for thermal compared to chemical interlayer oxides. Furthermore, Chapter 5.1 shows that oxide disruption occurs even during short high-temperature annealing for chemical oxides, potentially accelerating Ag diffusion into the c-Si base and reducing passivation, particularly for the $P_{1.5}$-P oxide combination.

Thus, differences in thickness, doping, and thermal stability between chemical and thermal interlayer oxides can largely explain the observed variations in passivation across different layer combinations. Although many indicators support these conclusions, further research, such as high-resolution TEM imaging or Rutherford backscattering spectrometry, is required to confirm them with certainty [305].

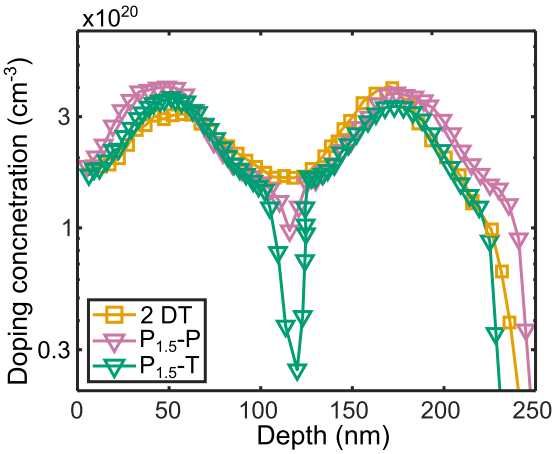

Figure 6.11.: *ECV boron doping profiles after firing at 900°C for different oxide-interlayer combinations and comparison to 2DT with a native interlayer oxide.*

6.2.3. Integration of the FPC Concept into Solar Cells

In this chapter, the influence of R_{Sheet}, ρ_{C}, and $J_{0,\text{Met}}$ on solar cell efficiency is discussed. During solar cell fabrication, many processing steps must be optimized in relation to one another to achieve high efficiencies. Instead of optimizing each step, a simulation approach using ISFH's SEGA-GUI tool based on Quokka 2 is employed [309, 310].

A TOPCon solar cell structure, similar to Figure 2.3(d), is used, where (p) poly-Si is integrated on the rear side of an (n) c-Si base with an n-type emitter emitter. All simulation parameters can be found in Table A.2 in the Appendix. Other cell designs, such as those where doped a-Si is deposited on a textured front side, are also possible. However, this can lead to parasitic absorption, and additional effort is needed to reduce this via bandgap tuning or very thin a-Si layers [27]. Figure 6.12(a) shows the relationship between sheet resistance and contact resistivity, while Figure 6.12(b) shows the influence of saturation current density on contact resistivity. To assess the performance of the interlayer oxide variation, evaluated values for ρ_{C}, $J_{0,\text{Met}}$, and R_{Sheet} are plotted as well.

In Figure 6.12(a), the dependency of contact resistivity on the sheet resistance of the poly-Si rear contact is shown. In this case, a relatively high $J_{0,\text{Met}} = 500$ fA/cm^2 was chosen. By decreasing $J_{0,\text{Met}}$, the effect of R_{Sheet} on efficiency becomes less significant. R_{Sheet} is determined alongside ρ_{C} through TLM measurements. A clear trend is visible across all sample configurations using this interlayer oxide approach, where a decreasing sheet resistance coincides with a lower contact resistivity. This correlation is largely due to formation of large Ag crystallites at higher firing temperatures, which correspond to a lower sheet resistance.

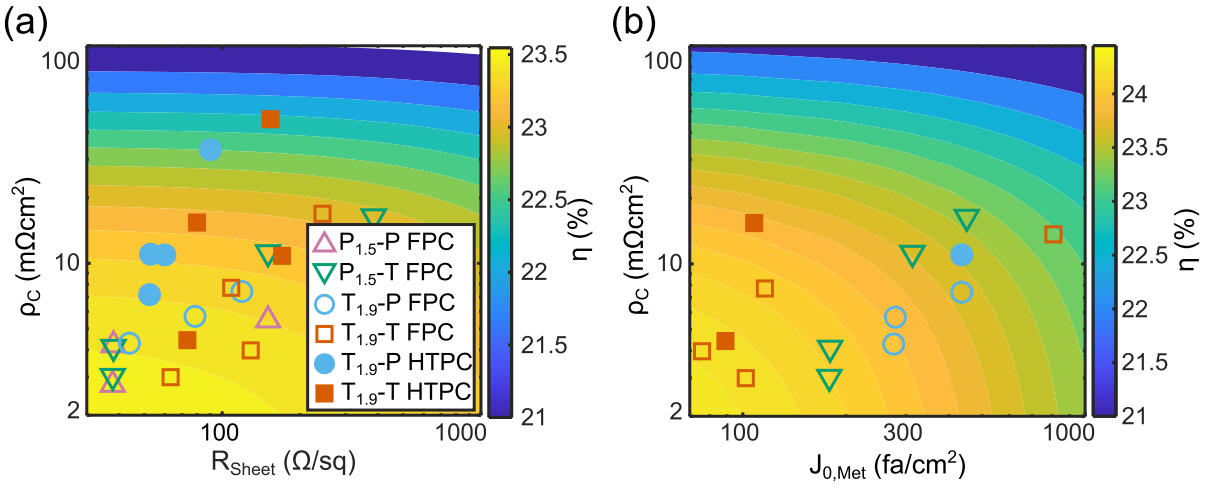

Figure 6.12.: *Influence of different solar cell parameters determined by efficiency simulation via Quokka 2. (a) Contact resistivity in dependence of the sheet resistance and (b) contact resistivity in dependence of $J_{0,\text{Met}}$. Parameters for the simulations can be found in Appendix A.2. Measured values for ρ_{C}, R_{Sheet}, and $J_{0,\text{Met}}$ are inserted for different interlayer oxide combinations.*

Furthermore, higher sheet resistances decrease cell efficiency. This effect is marginal for typical poly-Si resistances obtained in this work. A low contact resistivity is much more critical for achieving high η, as supported by the results in Figure 6.12(b). In this case, efficiencies $\eta > 24\%$ are only achievable with $\rho_C < 10$ mΩcm^2 and $J_{0,Met} < 200$ fA/cm^2. Similar to sheet resistance, an increasing $J_{0,Met}$ mostly correlates with larger ρ_C values. The best FPC efficiency for the respective ρ_C and $J_{0,Met}$ values is approximately 24.3% for the $T_{1.9}$-T oxide combination. However, even $P_{1.5}$-T oxides can lead to efficiencies around 24%. On the other hand, the $P_{1.5}$-P and multiple drive-through approaches are not compatible with high-efficiency solar cell devices due to high $J_{0,Met}$ values.
Thus, the interlayer oxide approach for FPC samples shows great promise for implementation into solar cells. To improve the results even further, the consistency of the a-Si deposition should be refined by minimizing inhomogeneities, a-Si dust, and wrap-around. Furthermore, the separate interlayer oxide growth is not ideal for industrial implementation, as it requires an additional processing step. However, this could be improved upon by in-situ oxide growth in the APCVD system, potentially using multiple injectors. The corresponding longer processing time in the APCVD machine may even enhance crystallization and passivation while reducing sheet resistance further [311].

6.3. Chapter Summary

In this chapter, metallization using Ag paste screen-printing was investigated at various firing temperatures, employing the multilayer approach through multiple drive-throughs. Studies on textured surfaces showed a reduction in contact resistivity at higher firing temperatures with 2DT and 3DT, down to approximately 2 mΩcm^2. SEM cross-sections revealed a larger density of Ag crystallites within the poly-Si layer at higher firing temperatures, which helped reduce contact resistivities for thicker layers. In some cases, Ag crystallites were stopped at the interlayer oxide, though not as reliably as in well-crystallized layers reported in the literature. The lack of a reliable etch stop at the interlayer oxide led to very high surface passivation under the metal contacts ($J_{0,Met}$), particularly due to Ag crystallite penetration into the base at pyramid tips, coupled with insufficient dopant in-diffusion.
Planar surfaces exhibited similar contact resistivity behavior, with slightly higher values than on textured surfaces, especially at lower firing temperatures. However, increasing the number of drive-throughs and the firing temperature improved $J_{0,Met}$ values, reaching as low as 350 fA/cm^2 for 5DT. Thicker layers increased the likelihood of Ag crystallites being confined to the poly-Si. Without direct contact of Ag to the interfacial oxide or the c-Si base, the passivation quality is preserved.

The use of chemical interfacial oxides reduced contact resistivity slightly due to charge transport through the base, but $J_{0,\text{Met}}$ increased slightly. Investigations of the transport mechanism through the oxide revealed a similar transition from tunneling- to pinhole-dominated transport toward firing temperatures, consistent with results for (n) a-Si in the case of evaporated contacts.

To further enhance passivation after metallization, a thermal and chemical interlayer oxide was employed instead of the native interlayer oxide grown during deposition. This resulted in slightly higher contact resistivity with minimum of around 3 mΩcm^2 at the highest firing temperatures, depending on the combination of interfacial and interlayer oxide. These oxides still enabled charge carrier transport, where oxide contact resistivity decreased heavily at higher firing temperatures.
A significant difference between the native interlayer oxide and the artificially grown ones was visible in SEM cross-sections, where the Ag crystallites reliably stopped at the thermal and chemical interlayer oxides in the case of no extended crystallization. Interestingly, this was not necessarily true for HTPC samples in the case of a chemical interlayer oxide, which might be due to disruption of the oxide during crystallization. This stopping effect was also reflected in $J_{0,\text{met}}$ values, which decreased down to approximately 80 fA/cm^2 in the case of a thermal interfacial and interlayer oxide, presenting a massive improvement in surface passivation compared to multiple DT with native interlayer oxides.
The passivation after metallization was heavily impacted by the combination of interlayer and interfacial oxides, where thinner oxides led to worse passivation properties. Thus, a discussion of passivation-limiting factors was conducted in which Ag in-diffusion during firing was identified as a potential issue, especially in the case of little boron in-diffusion into the wafer. Consequently, a thicker interlayer and interfacial oxide may serve as an Ag diffusion barrier and may help to maintain a high passivation level.

Lastly, a brief classification of the results was provided in the context of a solar cell. Simulations with a poly-Si based passivating contact on the rear side explored the influence of sheet resistance, passivation after metallization, and contact resistivity onto cell efficiency. The simulation showed that a solar cell efficiency exceeding 24% is possible using the FPC concept with grown interlayer oxides. This is comparable to samples fabricated along the conventional HTPC route.

7. Summary

This work focused on poly-Si/SiO_x passivating contacts with a reduced thermal budget, aiming to simplify processing steps and reduce costs in comparison to conventional long annealing processes. Various characterization techniques were employed, with a focus on crystallite size analysis, investigation of charge carrier transport through the poly-Si and oxide into the silicon base, as well as characterization of solar cell parameters following metallization via Ag screen-printing.

In Chapter 4, the impact of varying the thermal budget was examined for samples without metallization. This revealed increased dopant in-diffusion, crystallite size growth, and sheet resistance reduction for both APCVD (p) a-Si and PECVD (n) a-Si layers with extended annealing times. The extent of in-diffusion was heavily influenced by the interfacial oxide's thickness and type. Achieving high passivation quality required optimization of the annealing process based on the specific properties of the SiO_x layer. While thicker interfacial oxides benefited from longer annealing times, chemically grown thin oxides achieved higher iV_{OC} values with a reduced thermal budget. Shifting the entire thermal budget to a single fast firing step proved unfeasible for PECVD a-Si due to severe blistering. In contrast, APCVD a-Si, deposited at higher temperatures with significantly less hydrogen content, did not exhibit blistering. Section 4.2.1 explored the influence of different a-Si doping for varying firing temperatures, identifying (p) a-Si as the most promising option due to its compatibility with higher firing temperatures. Crucially, crystallite growth was already observed during the fast firing step. In the case of APCVD layers, larger crystallites emerged in comparison to other deposition techniques, likely due to the high 700°C deposition temperature functioning as an in-situ annealing process. The use of multiple drive-throughs (DT) for FPC layers resulted in lower sheet resistance and high passivation, particularly at increased firing temperatures. Passivation was further enhanced by selecting thinner chemical oxides, which most likely allowed slight in-diffusion, potentially improving passivation further.

In Chapter 5, the transport of charge carriers was analyzed, with a focus on short, high-temperature annealing processes. TLM measurements revealed a transition of transport mechanisms through the oxide. A shift from tunneling to pinhole-dominated transport occurred without significantly degrading passivation. This transition was primarily dependent on annealing temperature rather than duration, happening within a few seconds. Pinhole

creation in very short time frames was confirmed by pinhole magnification studies, using TMAH etching and SEM imaging. These findings deviate from pinhole growth models in literature, which do not appear to apply to early stage growth in thin, thermally unstable oxides. Section 5.2 examined transport within the poly-Si layer, building on an existing mobility model via temperature-dependent Hall (T-Hall) measurements. A modification to the mobility's temperature dependence was proposed to account for additional scattering mechanisms, higher doping level, larger measured temperature range, and the effects of amorphous phases in the poly-Si. This enabled the determination of grain boundary barrier height and trap density for APCVD (p) a-Si layers. Additionally, crystallite sizes and sheet resistances were correlated using experimental doping concentrations and grain boundary barrier heights for (p) a-Si on fused silica substrates. Repeating this process on Cz bases, while factoring in the base resistivity contribution, resulted in overall good agreement.

Metallization was accomplished via screen-printing with Ag paste and was addressed in Chapter 6. Low contact resistivities were achieved for both planar and textured surfaces. However, for textured surfaces, high recombination currents were observed under the metal contacts. This was the case due to excessive Ag crystallite formation visible in SEM images, where many crystallites made contact with the interfacial oxide. Additionally, increasing the number of drive-throughs significantly reduced recombination beneath the metal contacts for planar substrates. The type of oxide and silicon base had only a marginal effect on contacting properties. Pinhole-dominated transport was identified via T-TLM measurements at higher firing temperatures for screen-printed contacts on a chemical oxide. The multiple drive-through concept was further refined by artificially growing different interlayer oxides between two poly-Si layers, achieving contact resistivities below 3 mΩcm^2 at high firing temperatures. Notably, unlike for the multiple drive-through method, these interlayer oxides prevented Ag crystallites to penetrate into the lower poly-Si layer. This stopping mechanism is crucial to enable high passivation and has so far not been reported for (p) a-Si layers. Passivation beneath the metal contacts was significantly improved, with a minimum $J_{0,\text{Met}} \approx 80$ fA/cm^2. This is much lower than the value for 5DT with native interlayers oxides, which was approximately $J_{0,\text{Met}} \approx 350$ fA/cm^2. Ag diffusion into the c-Si base was speculated to be a limiting factor for passivation, as the SiO_x may serve as a barrier to Ag diffusion. Simulations of the efficiency potential for FPC layers, utilizing this interlayer oxide approach, indicated an efficiency exceeding 24% for a standard TOPCon solar cell with a poly-Si/SiO_x contact on the rear side.

In conclusion, the FPC concept, featuring a lean manufacturing process, shows significant potential for integrating APCVD (p) a-Si layers into solar cell devices, especially using the interlayer oxide approach. Further optimization of the APCVD deposition process can help to fully realize its potential.

List of Publications

Peer-Reviewed Journal Publications

- T. Okker, R. Glatthaar, S. Seren, G. Hahn, & B. Terheiden. "Charge Carrier Transport Mechanism through Different Oxides for (n) Poly-Si/SiO_x Fired Passivating Contacts". In: *Phys. Status Solidi RRL* 18.9 (2024), pp. 1-7.
- R. Glatthaar, F. Huster, T. Okker, B. C. Greven, S. Seren, G. Hahn, & B. Terheiden. "Contact Formation of Silver Paste and Atmospheric Pressure Chemical Vapor Deposition (n) Poly-Silicon Passivating Contacts on Planar and Textured Surfaces". In: *Phys. Status Solidi A* 219.24 (2022), pp. 1-8.
- J. Linke, R. Glatthaar, F. Huster, T. Okker, S. Möller, G. Hahn, & B. Terheiden. "Poly-Si Thickness and Temperature Dependent Oxide Disruption Induced by Penetration of the Interfacial Oxide in (p) Poly-Si/SiO_x Passivating Contacts". In: *Sol. Energy Mater. Sol. Cells* 246 (2022), pp. 1-8.
- R. Glatthaar, B. C. Greven, T. Okker, F. Huster, G. Hahn, & B. Terheiden. "Fundamental Microscopic Studies on the Etching Behavior of Silver Pastes on Poly-Si/SiO_x Passivating Contacts". In: *Sol. Energy Mater. Sol. Cells* 261 (2023), pp. 1-7.
- R. Glatthaar, F. P. Schmidt, A. Hammud, T. Lunkenbein, T. Okker, F. Huster, G. Hahn & B. Terheiden. "Silver Metallization with Controlled Etch Stop Using SiO_x Layers in Passivating Contacts for Improved Silicon Solar Cell Performance". In: *Sol. RRL* 7.21 (2023), pp. 1-9.

Conference Proceedings

- T. Okker, R. Glatthaar, S. Seren, G. Hahn, & B. Terheiden. "Influence of Firing Temperature on APCVD Poly-Si Properties for Fired Passivating Contacts". In: *AIP Conf. Proc.* Vol. 2826, 2023, pp. 1-5 - Poster Award Winner.

- T. Okker, R. Glatthaar, F. Huster, G. Hahn, B. C. Greven, S. Seren, & B. Terheiden. "Investigation of Contact Resistivities on APCVD (p) Poly-Si for Fired Passivating Contacts". In: *Proc. 13th Int. Conf. Cryst. Silicon Photovolt.* 1 (2024), pp. 1-6 - Poster Award Winner.
- T. Okker, R. Glatthaar, F. Huster, G. Hahn, S. Seren, T. Pernau, & B. Terheiden. "Accurate Crystallite Size Determination in Poly-Si/SiO_x Passivating Contacts". In: *Proc. 2023 Eur. Photovolt. Sol Energy Conf.* (2023), pp. 1-4.
- R. Glatthaar, T. Okker, F. Huster, B. C. Greven, S. Seren, G. Hahn, & B. Terheiden. "APCVD (n) Poly-Si Passivating Contacts on Textured and Planar Surfaces". In: *Proc. 2022 Eur. Photovolt. Sol Energy Conf.* (2022), pp. 1-8.

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A. Appendix

The following Chapter displays supplementary information, referred to in the course of this work. In Section A.1, additional measurements are provided, while in Section A.2 details to simulations and fit parameters are supplied.

A.1. Additional Measurements

This section provides additional measurements, giving additional context to presented results. These are GDOES measurements of different doping concentrations, results of strain analysis for XRD measurements, additional T-TLM measurmeents, and contact resistivities for PECVD (n) a-Si.

Doping Concentration

GDOES measurements for highly and lowly doped (p) a-Si are shown in Figure A.1 to illustrate the doping difference for different a-Si thicknesses. A significant deviation in signal strength between lowly and highly doped (p) a-Si is visible.

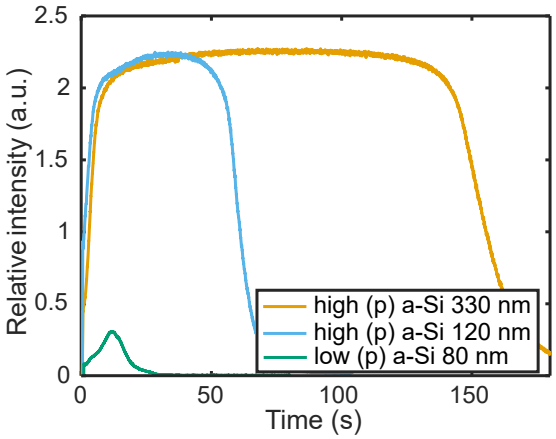

Figure A.1.: *GDOES measurements for highly and lowly doped (p) a-Si for various thicknesses.*

Poly-Si Strain

Strain values after Rietveld refinement of XRD measurements for different types of a-Si are shown in Figure A.2. It is noticable, that PECVD (n) a-Si leads to lower strain compared to APCVD (n) a-Si. Even higher strain values are obtained for (p) a-Si layers, especially for a higher doping concentration.

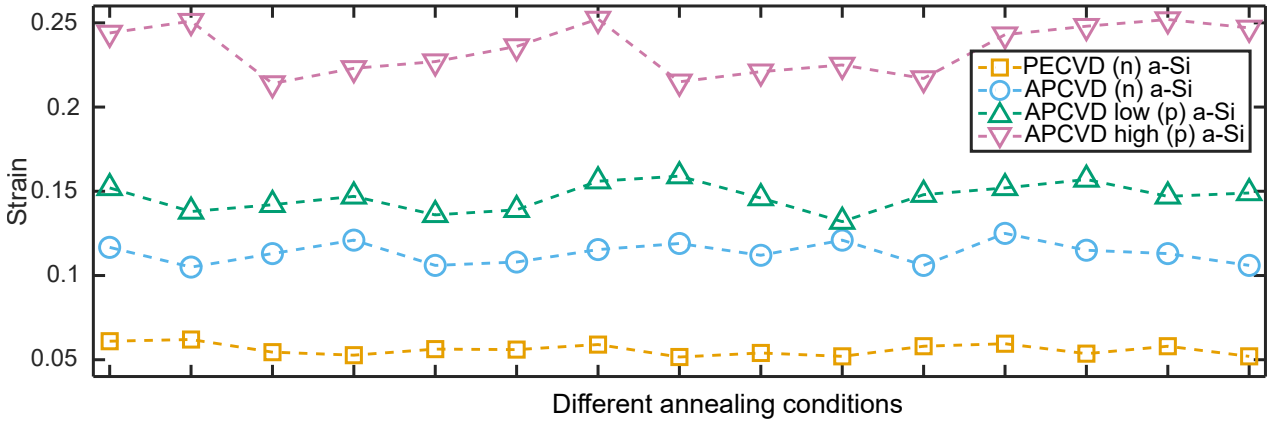

Figure A.2.: *Strain values determined from XRD measurements for PECVD (n) a-Si, APCVD (n) a-Si, APCVD (p) a-Si with low doping, and APCVD (p) a-si with high doping.*

T-TLM measurements

Additional T-TLM measurements with corresponding fits, which have been used to illustrate the pinhole fractions in Figure 5.4, are shown in Figure A.3.

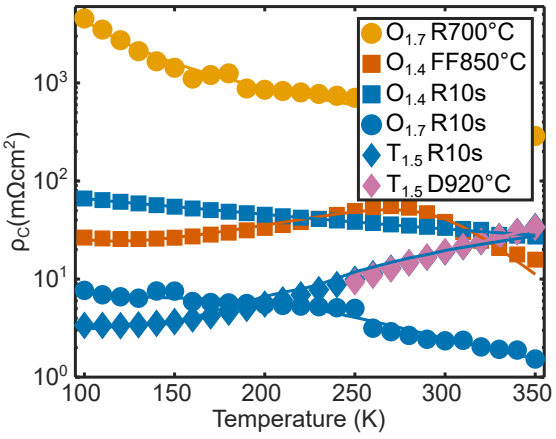

Figure A.3.: *T-TLM measurements for different oxides and annealing times with corresponding fits.*

PECVD Contact Resistivity

Contact resistivities for FPC and HTPC approach for PECVD (n) a-Si with a thermal interlayer oxide are shown in Figure A.4. The FPC approach leads to higher contact resistivities compared to HPTC samples.

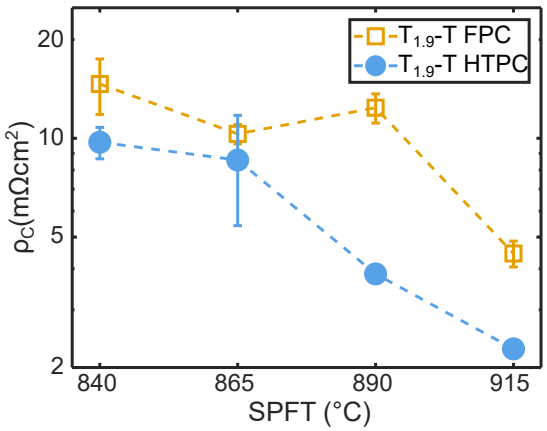

Figure A.4.: *Contact resistivity for PECVD (n) a-Si at different firing temperatures for the $T_{1.9}$-T oxide in the case of FPC and HTPC.*

A.2. Simulation and Fit Parameters

In this section, additional information regarding simulations and fit parameters is provided. This includes details for T-TLM fit parameters and simulation parameters to obtain the cell efficiency using Quokka2.

T-TLM Fit Parameter

All fit parameters of T-TLM measurements used within this work are listed in Table A.1.

Table A.1.: *T-TLM fit parameters for various types of a-Si, annealing, and oxides.*

a-Si	Oxide	Annealing	f_{P}	$m_{\mathrm{T}}[m_0]$	ΔE_{S}[meV]	d_{ox}[nm]	$N_{\mathrm{P}}[\mathrm{cm}^{-2}]$	r_{P}[nm]	$N_{\mathrm{D}}[\mathrm{cm}^{-3}]$
APCVD (n)	$P_{1.5}$	R700℃	0	0.23	66	1.5	-	-	-
APCVD (n)	$P_{1.5}$	R5s	1	-	-	-	$1 \cdot 10^{8}$	4.4	$7.5 \cdot 10^{14}$
APCVD (n)	$P_{1.5}$	R30s	1	-	-	-	$3 \cdot 10^{7}$	5.3	$7.5 \cdot 10^{14}$
APCVD (n)	$P_{1.5}$	D920℃	1	-	-	-	$1 \cdot 10^{8}$	5.6	$3 \cdot 10^{15}$
APCVD (n)	$O_{1.4}$	R700℃	0	0.36	10	1.42	-	-	-
APCVD (n)	$O_{1.4}$	FF850℃	0.64	0.13	243	1.40	$5 \cdot 10^{7}$	4.8	$7.5 \cdot 10^{14}$
APCVD (n)	$O_{1.4}$	R5s	0.43	0.23	54	1.46	$5 \cdot 10^{6}$	3.6	$1.5 \cdot 10^{16}$
APCVD (n)	$O_{1.4}$	R10s	0.523	0.23	74	1.45	$1 \cdot 10^{6}$	3.1	$6.5 \cdot 10^{16}$
APCVD (n)	$O_{1.4}$	R30s	0.71	0.23	142	1.40	$1 \cdot 10^{7}$	6.1	$7.5 \cdot 10^{14}$
APCVD (n)	$O_{1.4}$	D920℃	1	-	-	-	$1 \cdot 10^{8}$	7.4	$7.5 \cdot 10^{14}$
APCVD (n)	$O_{1.7}$	R700℃	0	0.32	15	1.70	-	-	-
APCVD (n)	$O_{1.7}$	FF850℃	0.59	0.12	345	1.71	$7 \cdot 10^{6}$	3.9	$6.5 \cdot 10^{15}$
APCVD (n)	$O_{1.7}$	R5s	0	0.23	0.12	1.67	-	-	-
APCVD (n)	$O_{1.7}$	R10s	0.055	0.14	142	1.68	$9 \cdot 10^{6}$	4.3	$1.5 \cdot 10^{15}$
APCVD (n)	$O_{1.7}$	R30s	0.66	0.23	24	1.65	$9 \cdot 10^{6}$	4.1	$2 \cdot 10^{16}$
APCVD (n)	$T_{1.5}$	FF850℃	0.31	0.23	34	1.68	$9 \cdot 10^{5}$	3.1	$3 \cdot 10^{16}$
APCVD (n)	$T_{1.5}$	R5s	0.059	0.23	72	1.53	$9 \cdot 10^{4}$	3.3	$3.5 \cdot 10^{15}$
APCVD (n)	$T_{1.5}$	R10s	1	-	-	-	$1 \cdot 10^{8}$	5.9	$7.5 \cdot 10^{14}$
APCVD (n)	$T_{1.5}$	R30s	1	-	-	-	$5 \cdot 10^{7}$	5.8	$7.5 \cdot 10^{14}$
APCVD (n)	$T_{1.5}$	D920℃	1	-	-	-	$3 \cdot 10^{7}$	5.3	$7.5 \cdot 10^{14}$
PECVD (n)	$P_{1.5}$	R700℃	0	0.23	118	1.49	-	-	-
PECVD (n)	$T_{1.5}$	R5s	1	-	-	-	$3 \cdot 10^{7}$	4.5	$8.5 \cdot 10^{15}$
PECVD (n)	$O_{1.7}$	R5s	0	0.23	58	1.50	-	-	-
PECVD (n)	$O_{1.7}$	R30s	1	-	-	-	$3 \cdot 10^{8}$	5.2	$1 \cdot 10^{15}$
APCVD (p)	$P_{1.5}$	FF840℃	0.30	0.36	14	1.53	$1 \cdot 10^{5}$	3.3	$3.5 \cdot 10^{15}$
APCVD (p)	$P_{1.5}$	FF915℃	1	-	-	-	$2 \cdot 10^{6}$	3.5	$1 \cdot 10^{16}$

Quokka 2

For solar cell efficiency simulations, the contribution of the metal grid is assumed to contribute 0.3 $\Omega\mathrm{cm}^2$ to the series resistance, and the generation current is 42 $\mathrm{mA/cm}^2$. Key cell

parameters used to determine cell efficiency are listed in Table A.2.

Table A.2.: *Parameters used for Quokka 2 simulations to determine the efficiency of a solar cell with a poly-Si layer on the rear side.*

Rec. Properties	**Value**	**Contact Properties**	**Value**
Bulk lifetime	2 ms	Front finger width	25 μm
Bulk resistivity	5 Ωcm	Front finger pitch	1000 μm
Front passivated rec.	5 fA/cm^2	Front contact resistivity	1 mΩcm^2
Front contact rec.	500 fA/cm^2	Rear finger width	80 μm
Emitter	150 Ω/sq	Rear finger pitch	1000 μm
Rear passivated rec.	5 fA/cm^2	Rear contact resistivity	[1-100] mΩcm^2
Rear contact rec.	[1-1000] fA/cm^2	Rear Sheet resistivity	10-1000 Ω/sq

Zusammenfassung

Diese Arbeit untersuchte poly-Si/SiO_x passivierende Kontakte mit geringem thermischen Budget (FPC). Ein wesentliches Ziel war es den Prozessfluss zu vereinfachen und die Kosten im Vergleich zu herkömmlichen, längeren Kristallisationsprozessen zu senken. Dabei lag der Schwerpunkt auf der Analyse von Kristallitgrößen durch XRD-Messungen, der Untersuchung des Ladungsträgertransports durch das poly-Si und Grenzflächenoxid, sowie der Charakterisierung von Metallkontakten nach Siebdruck.

In Kapitel 4 wurde der Einfluss verschiedener thermischer Budgets auf unmetallisierte Proben untersucht. Mit längeren Kristallisationszeiten wurde eine Zunahme der Eindiffusion von Dotanden beobachtet, wobei das Ausmaß der Eindiffusion stark von der Dicke und Art des Grenzflächenoxids abhing. Sowohl für APCVD (p) a-Si als auch für PECVD (n) a-Si wurden mit größerem thermischen Budget größere Kristallite und kleinere Schichtwiderstände beobachtet. Um eine hohe Passivierung zu erreichen, muss der Kristallisationsprozess an die spezifischen Eigenschaften der SiO_x-Schicht angepasst werden. Während dickere Oxide von längeren Kristallisationszeiten profitierten, erreichten chemisch gewachsene dünnere Oxide höhere iV_{OC}-Werte bei geringerem thermischen Budget. Die Verlagerung des gesamten thermischen Budgets auf einen einzigen schnellen Feuerschritt erwies sich für PECVD a-Si als nicht umsetzbar aufgrund starker Blisterbildung. Im Gegensatz dazu zeigte APCVD a-Si keine Blister, da die Abscheidung bei höheren Temperaturen mit signifikant weniger Wasserstoffgehalt stattfand. In Abschnitt 4.2.1 wurde der Einfluss unterschiedlicher a-Si-Dotierungen für verschiedene Feuertemperaturen untersucht, wobei (p) a-Si aufgrund seiner Kompatibilität mit höheren Feuertemperaturen als vielversprechendste Option identifiziert wurde. Zu betonen ist, dass bereits während des kurzen Feuerschritts Kristallitwachstum beobachtet wurde, wobei für APCVD-Schichten größere Kristallite im Vergleich zu PECVD gemessen wurden. Die Verwendung mehrerer Durchfahrten für FPC-Schichten führte zu einem niedrigeren Schichtwiderstand, wobei ein gutes Passivierungslevel erreicht werden konnte. Dies konnte durch die Verwendung chemischer Grenzflächenoxide weiter verbessert werden, vermutlich aufgrund einer geringfügigen Eindiffusion von Dotanden während des Feuerprozesses.

In Kapitel 5 wurde der Ladungsträgertransport mit Fokus auf kurze Hochtemperaturprozesse analysiert. TLM-Messungen zeigten einen Übergang des Transportmechanismus durch das Oxid von tunneldominiertem zu pinholedominiertem Transport. Dieser Übergang war

hauptsächlich von der Temperatur und nicht von der Dauer des Prozesses abhängig und trat innerhalb weniger Sekunden auf. Die Pinhole-Bildung in sehr kurzen Zeitspannen wurde durch Pinhole-Untersuchungen mit TMAH-Ätzen und Elektronenmikroskopbildern bestätigt. Diese Ergebnisse weichten von bestehenden Modellen des Pinholewachstums ab. In Abschnitt 5.2 wurde der Transport innerhalb der poly-Si-Schicht durch temperaturabhängige Hall-Messungen untersucht, wobei ein bereits bestehendes Mobilitätsmodell weiterentwickelt wurde. Eine Modifikation der Temperaturabhängigkeit wurde vorgeschlagen, um zusätzliche Streumechanismen, höhere Dotierungen, oder die Auswirkungen amorpher Phasen zu berücksichtigen. Dadurch konnten die Barrierehöhen und Defektdichten an den Korngrenzen für APCVD (p) a-Si-Schichten bestimmt werden. Zusätzlich wurden Kristallitgrößen und Schichtwiderstände unter Verwendung experimenteller Dotierkonzentrationen und Barrierenhöhen für (p) a-Si auf Quarzglas-Substraten korreliert. Mit Berücksichtigung des Basiswiderstands wurde dieser Prozess für (p) a-Si auf Cz-Basis wiederholt, was insgesamt eine gute Übereinstimmung zeigte.
Kapitel 6 beschrieb Metallisierung durch Siebdruck mit Ag-Paste für den FPC Ansatz bei verschiedenen Feuertemperaturen. Sowohl für planare als auch für texturierte Oberflächen wurden niedrige Kontaktwiderstände erreicht. Für texturierte Oberflächen wurden jedoch hohe Rekombinationsströme unter den Metallkontakten beobachtet. Dies korrelierte mit einer in REM Aufnahmen beobachteten großen Anzahl von Ag-Kristalliten, die Kontakt mit dem Grenzflächenoxid und möglicherweise der Siliziumbasis haben. Mehrere Durchfahrten durch die APCVD Anlage reduzierten die Rekombination unter den Metallkontakten signifikant. Dabei zeigten Oxidtyp und Dotierungstyp der Siliziumbasis nur einen geringen Einfluss auf den Kontakt. Wie auch bei aufgedampften Silberkontakten wurde bei hohen Feuertemperaturen Pinholetransport über T-TLM-Messungen identifiziert. Anstatt mehrere Durchfahrten zu verwenden, wurden unterschiedliche Zwischenoxide zwischen zwei poly-Si Schichten gezielt aufgewachsen. Dies ermöglichte Kontaktwiderstände unter 3 mΩcm^2 bei hohen Feuertemperaturen. Bemerkenswert ist, dass diese künstlich aufgewachsenen Zwischenoxide das Eindringen von Ag-Kristalliten in die untere poly-Si-Schicht verhinderten. Dieser Stoppmechanismus ist entscheidend, um eine deutliche Verbesserung der Passivierung zu ermöglichen, mit einem minimalen $J_{0,\text{Met}} \approx 80$ fA/cm^2. Dies ist deutlich niedriger als der Wert für 5 Durchfahrten mit nativen Zwischenoxiden, der $J_{0,\text{Met}} \approx 350$ fA/cm^2 betrug. Ag-Diffusion in die c-Si-Basis wurde als limitierender Faktor für die Passivierung vermutet, da SiO_x als Barriere für Ag-Diffusion dienen könnte. Effizienzpotenzial-Simulationen für FPC-Schichten, die diesen Zwischenoxid-Ansatz nutzen, zeigten eine Effizienz von über 24% für eine Rückkontakt TOPCon-Solarzelle.
Zusammenfassend zeigt das FPC-Konzept mit seinem reduzierten Prozessfluss erhebliches Potenzial für die Integration von APCVD (p) a-Si-Schichten in Solarzellen. Eine weitere Optimierung des APCVD-Abscheideprozesses kann helfen das volle Potenzial der Technologie auszuschöpfen.

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