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COMPARISON OF UMG MATERIALS: ARE INGOT HEIGHT INDEPENDENT SOLAR CELL EFFICIENCIES POSSIBLE?

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ABSTRACT: Upgraded metallurgical-grade silicon (UMG-Si) offers benefits in costs and energy consumption, although the actual low silicon price enhances the need to reach the same level of solar cell efficiency and long-term behaviour as electronic-grade silicon. Especially boron and phosphorus are hardly removable from the UMG silicon feedstock. Therefore, also the purity of the feedstock is relevant. This work shows the progress on this route for two ingot suppliers. The usage of UMG material from different suppliers allows a direct comparison of material quality and solar cell performance. Additionally, a selection of solar cells from different height positions was cut up into small stripe-like cells with the intention of receiving an improved spatial resolution in electroluminescence, dLIT, bulk resistivity and IV measurements.
Keywords: Upgraded Metallurgical Grade, Silicon Solar Cell, Electroluminescence

1 INTRODUCTION

The use of upgraded metallurgical-grade silicon (UMG-Si) as a material for solar cells involves several difficulties concerning the higher concentrations of impurities compared to standard block cast material. Especially the control of boron and phosphorus is crucial for the ingot yield and is pursued by different techniques [1]. Due to its segregation coefficient, boron cannot be removed totally only by means of solidification [2]. Therefore, it is important either to use a feedstock with low impurity concentrations or to influence the crystallization in a way that shifts most of the impurities to the top part of the ingot which is cut off in the end. Boron and phosphorus differ in the segregation coefficients. The high concentrations lead to a compensation zone in the upper part of the ingot implying a p/n junction according to the Scheil equation. For the cost-effective production of solar cells from UMG material, it is necessary to place the p/n junction as high as possible in the ingot to allow a high yield. Additionally, the IV parameters of the processed solar cells as well as carrier lifetimes and resistivities of the wafers should be homogeneous over the vertical positions in the ingot, but especially UMG-Si often shows strong spatial and vertical inhomogeneities [3].

All processed solar cells were characterized by IV measurements, electroluminescence under forward and reverse bias, dark lock-in thermography (dLIT) and bulk resistivity measurements. Then, a group of cells from varying height positions was cut up into smaller cells to account the averaging effects of the large cells, and the measurements were repeated.

2 MATERIAL CHARACTERISTICS

For this work, wafers from several bricks of two ingot suppliers A and B were used to process screen-printed multi-crystalline 12.5x12.5 cm^2 p-type solar cells. All wafers were fabricated from 100% UMG-Si ingots. Although this alternative to electronic grade silicon (EG-Si) is more effective concerning material costs, energy and chemical consumption, it is important to keep in mind the different material properties. Today's UMG-Si materials show a large variation in the concentration of impurities, depending on the feedstock suppliers and the ingot crystallization technique. Also the purification methods vary strongly [4, 5, 6]. In general, the concentrations are higher than for EG-Si, especially for boron and phosphorus. Due to the different segregation coefficients of the dopants, the resulting net doping concentration decreases with increasing ingot height position. Therefore, the bulk resistivity rises in the ingot from the bottom to the top. Most of the other impurities are segregated to the very top of the ingot. This is why they are mainly relevant for solar cells processed from this level. However, the very top part of the ingot is n-type material, due to the type inversion which is caused by the dopant concentrations. Thus, material from this fraction of the ingot normally isn't processed with the cell process for p-type solar cells as applied here.

The materials A_1 and A_2 from the first supplier were parts of bricks from the edges of two different ingots. The materials B_1 and B_2 from the second supplier were manufactured only on research purposes. Thus, material B_2 contains a higher phosphorus concentration.

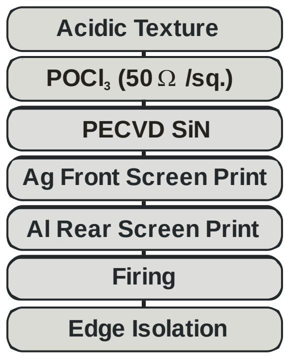

Figure 1: Process Flow Chart.

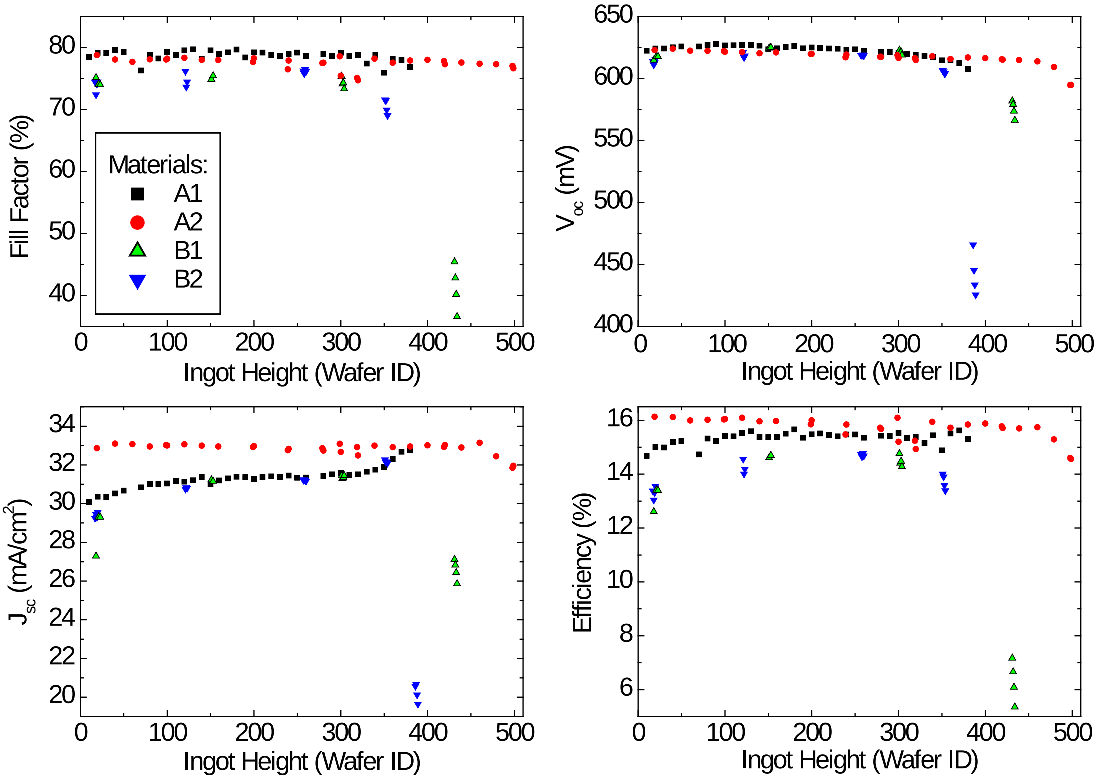

Figure 2: *IV parameters for the solar cells processed with materials from two ingot suppliers A, B in dependence of the vertical position in the ingot.*

3 CELL PROCESS AND CHARACTERIZATION

3.1 Solar cell process

100% UMG-Si wafers sawed out of several bricks by two different ingot suppliers were processed to 12.5x12.5 cm^2 multi-crystalline p-type solar cells according to the flow chart in Fig. 1.

After an acidic texturization, the emitter was formed by a 50 Ω/sq $POCl_3$ diffusion. Then, the phosphorus glass was removed and a SiN_x:H layer was deposited by plasma enhanced chemical vapour deposition (PECVD). A screen printed Ag front grid and a full Al rear contact formed the metallization which was dried and fired at an optimized temperature profile in a belt furnace. The edge isolation was performed by a wafer dicing saw.

3.2 Measurements

The bulk resistivities of the damage-etched wafers were measured with a 4-point prober. Besides IV measurements, all cells were characterized by means of electroluminescence (EL) under forward bias (20 mA/cm^2), EL under reverse bias (-10V, constant signal/noise-ratio) and dark lock-in thermography (dLIT) up to -9 V. These measurement setups have proven to offer innovative methods for spatial imaging of shunts and series resistances [7, 8]. Afterwards, five representative cells from different height positions in the ingot were each sawed into 16 (2x8) small stripe-like cells. The necessity to involve a piece of the busbar per cell to ensure reliable contacting set the limit of two columns. Then, the measurements were repeated with these small sample cells. The control measurement via dLIT allowed the extensive manual reduction of strong shunts at the newly created sawed cell edges. The bulk resistivity maps were measured on neighbouring damage-etched wafers. Additionally, the Seebeck effect was used to distinguish between p- and n-types.

4 HEIGHT INDEPENDENT CELL EFFICIENCIES

The distribution of impurities in dependence of the height within the ingot can be calculated according to the Scheil equation [9]. Variations of the concentration of boron and phosphorus within the silicon feedstock enable the shift of the type inversion level. Thus, the wafer yield of an ingot can be increased by a controlled addition of boron or phosphorus or by a more purified feedstock. However, it is important to keep in mind that for UMG-Si the concentrations cannot be varied independently because this affects directly the bulk resistivity, too. This is why completely height independent cell results cannot be realized. But it should be theoretically possible to reach similar cell properties like cells processed from wafers which were manufactured via the Siemens route and minimize the variations in the IV parameters resulting in rather height independent cell efficiencies.

5 RESULTS OF LARGE SOLAR CELLS

5.1 IV results

We studied the materials of two different ingot suppliers. All materials consist of 100% UMG-Si. The main part of each studied ingot brick is p-type, which means that the concentration of boron is higher than that of phosphorus.

From the first supplier A, the highest position of wafers is on the verge of the p/n junction of the ingot. However, from the second supplier B wafers from the higher n-type part of the ingot were also available. The delivered wafers were processed to screen-printed solar cells under the same process conditions.

Fig. 2 shows the IV parameters of the completed solar cells in dependency on the wafer ID which relates with the position in the ingot brick. The wafers of both suppliers have similar thicknesses of about 200 µm, but the same wafer-IDs of both suppliers do not correspond to exactly the same position in ingot height. The results of the material A_1 were already discussed recently. We observed an increase of the short circuit current density in the bottom and the top part, whereas the open-circuit voltage slightly increased with ingot height in the bottom part and decreased in the rest of the brick [10].

The ingot of the second material A_2 of the same supplier was produced later. Both bricks were parts of the edges of their ingots.

The comparison of A_1 and A_2 in Fig. 2 shows that the wafers from the more recent material A_2 result in more homogenous IV parameters according to ingot height position. The short circuit current density is almost stable at 33.0±0.4 mA/cm^2 until it decreases in the highest part which is much higher than for A_1. One possible explanation for this decrease is that the inversion level is at a position high enough in the brick so that the harmful effects from the high impurity concentrations in the top overcompensate the expected increase in the short circuit current density. The open-circuit voltages and fill factors for A_2 decrease much slower with ingot height than measured for A_1. Especially in the upper part, the decrease is shifted further to the highest part of the ingot, according to the higher placed p/n junction.

The decreases of the open-circuit voltages (Fig. 2), the fill factors and as a result also of the efficiencies for A_1 as well as for B_1 and B_2 compared to A_2 are observed for all cells of the recent experiment. They are not caused by the material qualities but by increased saturation current densities j_{02} of ~ 80 nA/cm^2. According to this, the solar cells show a reduced internal quantum efficiency (IQE) for short wavelengths which can be explained by increased recombination as a result of accidental contamination during texturization.

For the material B_1, the strong decrease of all IV parameters starts roughly at wafer-ID 400. This is about the same height as for A_1, but much lower than for A_2.

The material B_2 contains an addition of phosphorus to the melt. That is why the inversion of the polarity type is located about 70 wafers lower than for B_1.

The comparison of these materials shows that the ingots B_1 and B_2 were not optimized for UMG-Si. One plausible

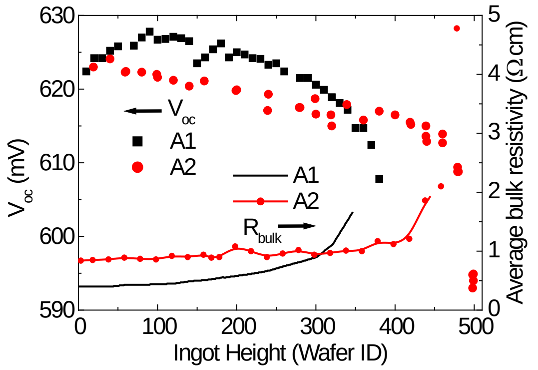

Figure 3: *Comparison of open-circuit voltage and average bulk resistivity for the materials A_1 and A_2.*

possibility is a not yet adjusted crystallization of the ingot. Another one is that there are differences concerning the purities of the silicon feedstocks which increased the height position of the p/n junction for A_1 and especially for A_2.

5.2 V_{oc} versus bulk resistivity

The average bulk resistivity increases with ingot height due to the decline of the net doping which is caused by different segregation coefficients of boron and phosphorus, according to the Scheil equation. The increase in bulk resistivity should come along with a decrease of the open-circuit voltage, because for UMG-Si, the net doping is relevant, instead of the acceptor concentration which was discussed in [11]. This is in agreement with the observed behaviour which is shown in Fig. 3. While A_1 showed a bulk resistivity profile like reported for other materials [4], A_2 starts at a higher resistivity and is stable over a larger height. Both V_{oc} curves for A_1 and A_2 show the same dependence of the bulk resistivity which is also clearly visible at the intersection point. Thus, other effects influencing V_{oc} would have to occur for both materials A_1 and A_2.

5.3 Grain boundaries

The electroluminescence images under forward bias of 20 mA/cm^2 (see left column of Fig. 4) show the entirely processed cells. The small sample cells, which are discussed below, resulted in qualitatively identical forward bias images. The grain boundaries which can be seen clearly by the lower luminous recombination activities get more and dense towards higher positions. In addition, grain boundary clusters grow and then remain stable over wide height ranges. Further details will be discussed in the following.

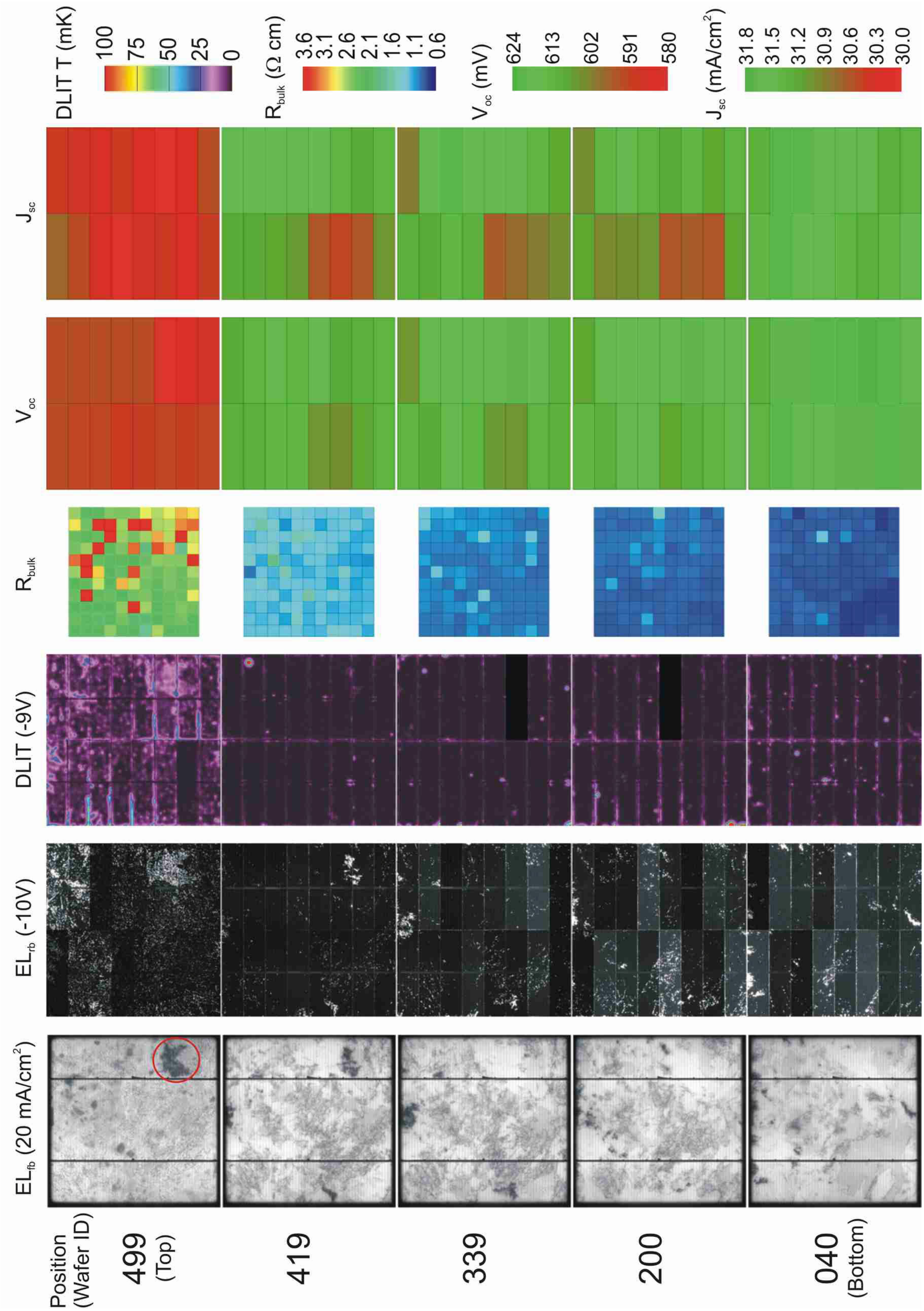

Figure 4: *Survey of the measurements on sawn sample solar cells from material A2 in dependence of the ingot height position.*

6 RESULTS OF SAWN CELLS

The IV measurements of the 12.5x12.5 cm^2 cells provide only average values. This is why strong 2-dimensional inhomogeneities within the cell can hardly be distinguished from homogeneous but low performing cells. For the electroluminescence setup, especially under reverse bias, a large amount of the limited maximum current can flow off over dominant shunts. This reduces the apparent intensity of the rest of the cell. Therefore, five cells were selected from different heights of the material A_2 and each sawed into 2x8 cm^2 small cells to achieve a better spatial resolution. Then, the measurements by IV, electroluminescence and dLIT were repeated for these small sample cells and the results assembled in the original positions. Additionally, bulk resistivity maps were recorded for neighbouring wafers.

6.1 Stability of the short circuit current density

The short circuit current densities for the small cells reveal the spatial variations but are also systematically about 2 mA/cm^2 lower than for the entire cells. This is caused by two different effects. Mainly, this is due to a lack of a suitable IV calibration cell for this size, especially considering size and reflection. The finally chosen calibration contains a too low illumination intensity. Apart from this, the cutting into pieces causes increased shunts at the sawing edges. These could mostly be reduced by manual grinding. For most of the sawn sample cells of A_2, the short circuit current density remains unvaried except for a decrease in the very top part. So the reduction in efficiency is based on the decreasing open-circuit voltage which can be partly explained by the increased bulk resistivity while the reduction in the upper part might be caused by the increased impurity concentrations.

6.2 Spatially resolved bulk resistivity maps

In addition to the average values shown in Fig. 3, 2-dimensional maps of the bulk resistivities were performed on neighbouring wafers of the sawn sample cells. The results shown in Fig. 4 are mean values of two measurements with the wafers rotated by 90° to estimate the statistical and systematic variations. The visible distance from the wafer edges was kept during the measurements to reduce systematic errors which are caused by the wafer edge. Significant differences between the two measurements were only seen for a few separate values. Distinct local correlations between the bulk resistivity and the open circuit voltage are not observed because the measuring positions are defined differently and the variations within one wafer are small. Certainly, the increase of the bulk resistivity with ingot height followed by the decrease in V_{oc} can be seen. This causes also the lower V_{oc} for A_2 compared to A_1, but there is still a possibility for other additional reasons for the decrease in V_{oc}.

Since the same values of bulk resistivity can be measured either right below or above the type inversion, further investigations were necessary to rule out the possibility that particular parts of the cells are already n-type. This is plausible because of a probably earlier crystallization at the edges of the ingot. Voltage measurements with punctual heating using the Seebeck effect, executed on vertical cuts next to the brick confirm a slightly lower type inversion in the middle of the vertical cut compared to the edges at same height. When executed on the neighbouring wafers of the sawn sample cells, even for cell 499 no local type inversion was detected. This affirms the assumption (see IV measurements) of an inversion level high enough that the accumulated impurities in the top region inhibit the expected increase of the short circuit current density.

6.3 Shifting grain boundary clusters

The shown electroluminescence images under forward bias (20 mA/cm^2) were performed on the entire large cells. Qualitatively, the same results were observed for the small sample cells. In the pictures of the bottom ingot part, several grain boundary clusters can be seen. The whole series of EL images reveals that these and most of the grain boundaries are shifted towards the upper side of the image. The inspected brick was part of the ingot edge. The comparison with measurements on former materials indicates that the grain boundaries wander towards the centre of the ingot with increasing ingot height, so the bottom of the picture corresponds to the ingot's outer face.

6.4 Shunt analysis of grain boundary clusters

The EL reverse bias images showed that the grain boundary clusters were also areas of increased shunting. This explains qualitatively the lower short circuit current densities for the corresponding small cells, although the decline on the left side is stronger than expected. The reverse bias images for the subcells reveal much more details compared to the entire large cells. This is caused by the current limitation of the measurement bias, and by scaling. For strong shunts draining most of the current, the remaining weaker shunts are shown with a much lower intensity. This effect is much lower for the small cells. Additionally, the contrast of less shunted subcells is improved by individual scaling. For each subcell, the scales were set to the local minimum/maximum values.

The shunted area of the red-marked grain boundary cluster in the upper part of the brick appears larger than the cluster visible under forward bias. The whole series of EL images showed that the bundling starts already at position 340 and grows with ingot height. In the top part, also V_{oc} was reduced, but rather slightly considering the size of the cluster. The same size was observed with dLIT under reverse bias at -9 V. It is obvious that the intensity is much higher for the top part of the brick. The similarity of the dLIT signal and the bulk resistivity maps for the highest wafer can be caused by the grain boundaries constricting the current of the 4-point-prober and therefore increasing the measured bulk resistivity.

In the left part of the wafers, a small cluster starts to grow at position 140, reaches up to the top part of the brick where it disappears at position 460. In spite of its small size, this could be the reason for the lower V_{oc} and J_{sc} values in this region. dLIT does not show significant shunts here. Especially the low J_{sc} of the small sample cell 1_7 of wafer 200 cannot be explained by that.

7 SUMMARY

Our previous results [10] pointed to the necessity to shift the compensation level of p- and n-type silicon to a higher position within the ingot of UMG material to increase the fraction of p-type wafers. This work shows that this aim was achieved by at least one of the ingot producers under investigation. The efficiencies of solar cells processed from this material are homogeneous over the observed ingot height from bottom to the very top of the ingot. Though, due to a problem with the texturization, the fill factors were limited. The previously observed unbalanced increase in the short circuit current density and the decrease in the open-circuit voltage due to the changing doping level impeded the fabrication of solar cells with height-independent electrical properties. In the recent experiments we observed a constant short circuit current density and open-circuit voltage according to ingot height position. The p/n junction in the ingot was shifted to the very top of the ingot. Both can be explained by the increased stability of the bulk resistivity.

The materials from the second ingot manufacturer B (grown close to standard conditions) still show a decrease of all IV parameters at a lower position in the ingot compared to the first supplier's material A.

Solar Cells cut up into small sample cells from the first supplier's material provided a more detailed view, especially considering the influence of grain boundaries which are stable over a large range in ingot height.

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