The Influence of High Temperature Steps on Defect Etching and Dislocations: Etch Pit Density Reduction in Multicrystalline Silicon

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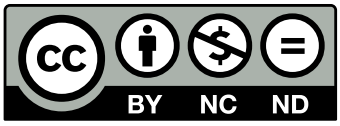


Abstract

This work is concerned with the study and explanation of a peculiar phenomenon that can be observed in dislocation-etched multicrystalline silicon after high temperature phosphorous diffusion steps. Dislocation etching forms visible etch pits at sites where the line-like disturbances of a crystal's symmetry, called dislocations, intersect with the crystal surface. High temperature phosphorous diffusion gettering steps can cause the density of etch pits to reduce drastically. Yet, it is not known whether this etch pit density (EPD) reduction can be identified with a reduction in the density of dislocations or whether other effects are at play that modify the formation of etch pits.

An algorithmic solution for automatic counting of etch pits has been developed that solves the distinct challenges appearing in the analysis of defect etched multicrystalline silicon (mc-Si) material. This procedure has been released to the community under a free and open source software license and is used to study the cause of etch pit density reduction directly, i.e. via the observation of the etch pit density in variation of the preparation state of the studied system. Using direct measurements of the EPD alone, hypotheses about the movement of dislocations in the observed temperature regime have been falsified and the mechanism of EPD reduction has been discerned. A complete picture of the mechanism of EPD reduction is formed by verifying a prediction of this mechanism that is outside of the scope of direct EPD measurements. Presumably, the discoveries about dislocation etching presented here apply to all types of crystalline silicon material and their implications should be considered.

Contents

1. Introduction and motivation

The study of multicrystalline silicon (mc-Si) material is directly linked with photovoltaics. In this field, the primary source of limits in the efficiency of solar cells has shifted away from the cell architecture to the semiconductor material quality. Since the beginning of the digital revolution, there is an increasing demand for the creation of high purity silicon material, that is integral to most of the technology surrounding us.
The refinement of silicon material quality has come a long way since: silicon crystals can be grown with higher purities than for any of the other elements [1] and impurities have been reduced to levels that are hardly detectable by direct measurements. The photovoltaics (PV) industry has profited and does profit a lot from goals that are shared with the much larger industry for silicon semiconductors, that are found in virtually every electronic device made on our planet today.

Large parts of this work focus on properties of and techniques for the analysis of crystal defects, especially those disturbances in the crystal symmetry that can be traced along a single line through the crystal, so-called dislocations. This thesis contributes some pieces of novel knowledge that affect the material characterization technique of dislocation etching, which is applied in photovoltaics and semiconductor device research alike. Dislocation etching forms visible etch pits at sites where the line-like dislocations intersect with the crystal surface. The etch pit density (EPD) is therefore often equated with the surface density of dislocations.
The contribution of this thesis is twofold: first, a software solution for determining large scale etch pit density maps with single dislocation precision has been developed and released to the community under a free and open source software licence [2]. A lack of such a tool might explain the fact that in the literature high precision etch pit data is regularly used in the form of example images of tiny sample regions, but only rarely quantitatively on a large scale. Second, this tool has been used for EPD analysis on multicrystalline silicon (mc-Si), aiding in the study and explanation of the phenomenon of reduced EPD after phosphorous gettering.
In this thesis, results from various experiments that study this phenomenon are combined to a new model that explains all observations and findings available in the literature by the same simple principle.
After the fundamental aspects of mc-Si material quality and essential properties of dislocations are discussed (chapter 2), the experimental methods for studying the material quality that are used throughout this thesis are presented (chapter 3). This includes a description of the algorithm for automatic etch pit counting and grain boundary identification (section 3.3.4). The effects on material quality of high temperature and gettering processes is documented from the perspective of charge

carrier lifetime and interstitial iron concentration measurements (sections 4.2.1, 4.4.1), as well as measurements of the surface-close charge carrier recombination activity (section 4.3). The passivating influence of hydrogen as well as the interplay of hydrogen passivation with the firing step is discussed and the effect of a hydrogen-free gettering step on the surface-close recombination activity is resolved (chapter 4.3). This experiment provides the necessary background for the interpretation of comparable measurement results (chapter 5.13), which offers evidence for the proposed mechanism of EPD reduction without relying on EPD measurements. The various windows into the interplay of impurity concentration and gettering steps presented in chapter 4 are a central contribution to the understanding of EPD reduction. Finally, a combination of experiments is described that use direct measurements of changes in the EPD to infer the mechanism that is underlying EPD reduction (chapter 5) and predictions of this mechanism are tested in ways that are independent of the EPD analysis (sections 5.13 and 5.14).

While the findings that concern EPD reduction have been achieved in the context of PV applications, a fact underlined most clearly by the choice of mc-Si material (a material solely used in PV), the insight into the behavior of defect etch solutions and their interplay with dislocations contribute to the understanding of defect etching on materials other than mc-Si and might therefore benefit silicon technology as a whole.

2. Fundamentals and their link to the local defect structure

This section contains an introduction to material quality aspects that are relevant in silicon photovoltaics as well as a description of a basic solar cell production process, from which the relevance of the processing steps applied in this thesis in solar cell production and their influence on material quality becomes clear. Links between these topics and the main achievements of this thesis are highlighted and the relation to the contents of the following chapters is pointed out. This chapter repeatedly uses [3].

2.1. Material quality

Central to the generation of electrical current by photovoltaic devices is the separation of charge carriers, photo-generated electron-hole pairs. This separation process can be regarded as complete, once the charge carriers have transitioned from the semiconductor material into external metallic terminals. As long as the separation process is incomplete, electron hole pairs can undergo pairwise recombination and thereby erase their contribution to the solar cell's current production. The electrical quality of materials used in photovoltaic applications is therefore mainly determined by the mean time difference between charge carrier creation and recombination, the effective charge carrier lifetime τ_{eff}.
In an infinitely large silicon crystal, i.e. a crystal without a surface but only bulk material, the charge carrier lifetime τ_{bulk} can be expressed as a function of a recombination rate R_{bulk} and the excess charge carrier density Δn, defining the bulk carrier lifetime as

$$\tau_{\text{bulk}} = \frac{\Delta n}{R_{bulk}}. \tag{2.1}$$

In the silicon bulk material there are three independent processes for recombination (figure 2.1) that add up to the combined bulk recombination rate

$$R_{\text{bulk}} = R_{\text{radiative}} + R_{\text{Auger}} + R_{\text{SRH}}. \tag{2.2}$$

The dominant recombination channel in mc-Si material is the Shockley-Read-Hall (SRH) recombination channel [4] [5]. Radiative and Auger recombination are effects intrinsic to the material and therefore not directly linked to material quality. Radiative recombination is the inverse process to charge carrier generation by photon

absorption: the direct recombination of an electron in the conduction band with a hole in the valence band. For indirect semiconductors like silicon, this direct band to band recombination is probabilistically disfavored, since the difference in crystal momentum between charge carriers of the valence and the conduction band has to be transferred for this process to happen. Conservation of momentum can be fulfilled e.g. in presence of a phonon of suitable momentum. Naturally, three body decay processes are probabilistically disfavored in comparison to two body processes, therefore in typical silicon materials, recombination losses due to radiative recombination can be neglected compared to SRH recombination activity. In the Auger recombination process, the energy from the electron-hole-recombination is transferred to a third particle, either to another electron in the conduction band or to a hole in the valence band. The particles receiving the energy will quickly relax thermally by transferring their energy to the lattice. As the presence of three particles is required, Auger recombination is a limiting effect only for high carrier concentrations.

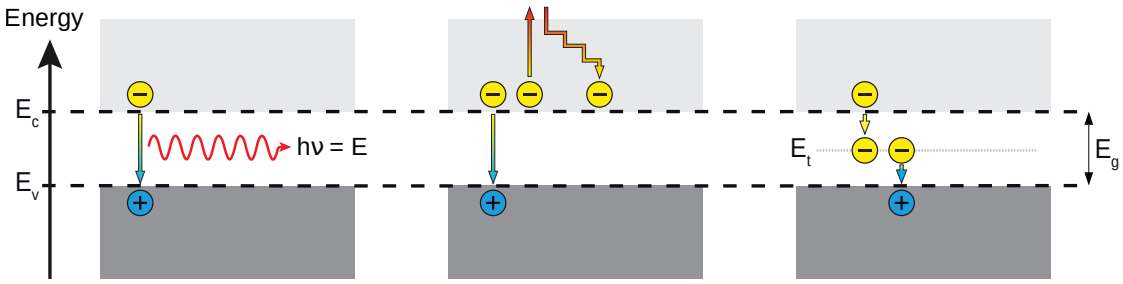


Figure 2.1.: Schematic representations of the recombination method via the radiative (left), Auger (middle) and Shockley-Read-Hall (right) process. Image by Sebastian Joos.

While Auger and radiative recombination are intrinsic crystal effects, unrelated to material quality, the Shockley–Read–Hall formalism describes recombination activity due to the presence of impurities and imperfections in the crystal. With any such disturbances of the crystal's periodicity, energy states within the silicon band gap are associated that can trap electrons from the conduction band, leading to a two-step recombination of excited states. Defects that produce energy states in the middle of the band gap ('deep' trap levels) exhibit significantly higher recombination rates than shallow states close to the conduction or valence bands [6]. For SRH recombination, the differences in crystal momentum between electrons in the conduction and valence band can be mediated via the defect that causes the intra band-gap energy state. Therefore, at typical solar cell operation conditions, SRH recombination is the dominant recombination channel in indirect semiconductors.

SRH recombination active energy states inside the band-gap originate from any disturbance to the crystal symmetry. These can be sorted according their dimensionality:

- **0-D, point defects:** Vacancies (missing silicon atoms at a lattice point, resulting in open or dangling bonds) and impurities (any non-silicon atoms in the silicon lattice or at interstitial sites)
- **1-D, line defects:** Dislocations, an extended line-like disturbance in the crystal's symmetry
- **2-D, plane defects:** Grain boundaries and the wafer surface
- **3-D, spatial defects:** Precipitates, i.e. crystallized impurities within the surrounding silicon crystal

The dominant lifetime-limiting effect is due to the untreated wafer surface. The sudden discontinuation of the crystal leads to continuous energy states inside the band gap [7] [8] that can be described as SRH recombination centers. Bulk and surface recombination effects can be combined to an effective lifetime

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{1}{\tau_{\text{surface}}}, \tag{2.3}$$

when considering typical silicon wafer material of the present time, for which the diffusion length $L(\tau_{\text{eff}}) = \sqrt{D\tau_{\text{eff}}}$ is large compared to the wafer thickness. The effective charge carrier lifetime is, in principle, by far the most sensitive tool for detecting the presence of impurity elements in silicon material [9] and accessible with various measurement methods. Therefore τ_{eff} is widely used as observable for quantification of material quality. A practical detection limit is reached, when measured lifetimes approach the intrinsic band-to-band recombination lifetime, which, for $10\,\Omega\,\text{cm}$ p-type silicon is equivalent to a detection limit of $10 \times 10^7\,\text{cm}^{-3}$ for an impurity like iron [9].

2.2. Dislocations and their influence on material quality

This thesis focuses on investigations of dislocations in the silicon bulk, line like locations from which a shift in the crystal symmetry originates. Dislocations are a major cause of lifetime limitations in mc-Si material. Improved lifetime results of newly developed high performance mc-Si material can often be attributed to modifications of the dislocation structure of the material [10].

The structural nature of a dislocation is best understood using the example of edge- and screw-dislocations, since they can be visualized easily (figure 2.2). Their disturbance in the crystal symmetry creates energy states within the band-gap [11],

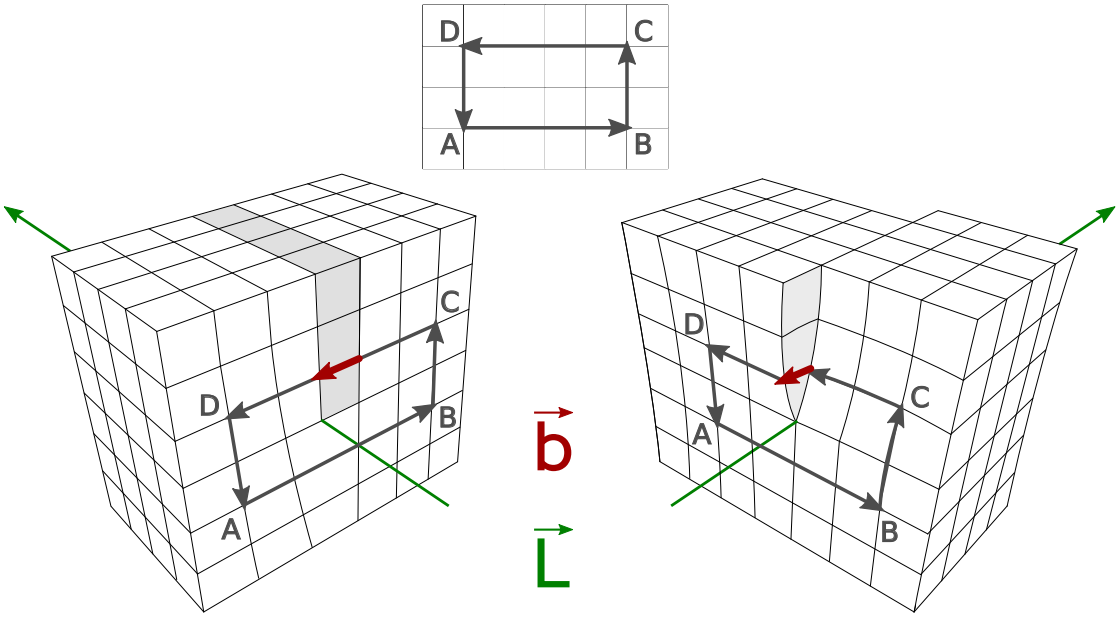


Figure 2.2.: Schematic drawing of an edge (left) and screw dislocation (right). Edge dislocations are caused by the presence of an additional half plane in the crystal (marked as gray blocks). The dislocation's line vector $\vec{L}$ is located along the end of that half plane. A screw dislocation can conceptionally be constructed by cutting the crystal along a half plane until the dislocation line is reached, followed by a shift of one of the cut halves in the direction of the dislocation line. The rectangles ABCD mark a closed loop around the dislocation centers. The same path in the undisturbed crystal differs from the path around a dislocation by the Burgers vector $\vec{b}$.

that can be thought of as a one dimensional chain of dangling bonds. Dislocations thereby facilitate carrier recombination according to the SRH model. The significance of dislocations to the recombination activity in silicon materials is well known [12] [13]. Recombination activity is enhanced further when dislocations are decorated with impurity elements [14] [15] [11].
It will be discussed how dislocations can be made visible by selective etching processes (section 3.3) resulting in visible etch pits at dislocation sites. For study of the impact of dislocations on the material quality, the density of etch pits is a central observable. Here, defect etching results are recorded with the optical microscope, having sufficient precision for the detection of single etch pits but at the same time allowing for analyses of regions with the size of several cm^2. The detection of etch pits on microscope raw images has been solved, based on a method published in [16]. This approach has been modified and extended in the context of this thesis (section 3.3.4). Some modifications deal with the characteristics of mc-Si image data, i.e. the necessary distinction between etch pit structures and grain boundaries. Other changes allow to compute results with larger file sizes or allow for computationally simpler and more versatile means of data presentation.

A Python implementation of the analysis developed during this thesis has been released to the community [2] as free and open source software under the GNU General Public License GPLv3.
Novel aspects in the understanding of the defect etch process, as well as for the interpretation of their results and the interplay of dislocations with impurities are presented here. Central results to the argumentation chain within this thesis, e.g. those presented in sections 5.8.1 or 5.8.2, would not have been possible without single etch pit precision analysis or would have likely been missed with less resolution and/or smaller analysis areas.

In mc-Si, the most problematic regions of lowest τ_{eff} are typically regions of highest dislocation density [13] [12]. By combining various spatially resolved measurements, i.e. τ_{eff}, interstitial iron concentration, etch pit density and surface-close recombination activity, the macroscopic behavior of material quality is resolved into microscopic components.

Since in the literature dislocation movement is often used to explain changes in the observed dislocation densities caused by high temperature annealing processes [17] [12] [18] as well as when caused by phosphorous gettering steps [19] [20], a brief discussion of the mathematical description of dislocation movement is given in the following section.

2.2.1. Dislocation mobility

Dislocation velocity v is typically described by an empirically motivated equation, describing a thermally activated process of the form

$$v = v_0 \left(\frac{\tau}{\tau_0}\right)^m \exp\left(-\frac{Q}{kT}\right), \tag{2.4}$$

where v_0 and τ_0 are constants of the material, k is the Boltzmann constant, the exponent m, typically in the range between 1 and 2 and the activation energy for the dislocation motion Q [21]. Large mechanical stress τ and high temperatures T lead to high dislocation velocities. Experimental findings show the exponent m to smoothly vary in the range of 0.8 to 2 with changing temperature [22], motivating the ansatz of a temperature dependent exponent [22]

$$m = m(T) = m_0 + \frac{E_i}{kT}$$

that leads to a formulation of equation (2.4) with a stress dependent activation energy:

$$v = v_0 \left(\frac{\tau}{\tau_0}\right)^{m_0} \exp\left(-\frac{Q - E_i \ln(\tau/\tau_0)}{kT}\right), \tag{2.5}$$

Experiments for studying dislocation velocities typically control τ by applying external mechanical stress on monocrystalline material [23] [22]. Dislocation velocities

can be estimated by repeated measurements of the location of dislocations using either defect etching or x-ray diffraction topography before and after mechanical stress is applied [24].

2.2.2. Dislocation creation and annihilation

Dislocations in silicon are created during crystal growth, so controlling dislocation densities is mostly possible at this stage. For monocrystalline silicon grown with the Czochralski process, dislocation growth can be significantly reduced by an initial reduction of the crystal diameter in the beginning of the crystal growth process, the so-called Dash necking process crystals [25]. Dash necking is especially useful to remove dislocations that are created by the thermal shock when the seeding crystal is brought in contact with liquid silicon [1].
Mc-Si is grown by cooling liquid silicon in a crucible. Thermal stress, e.g. due to faster cooling of the material close to the crucible wall as well as stress due to different crystal orientations are the main causes for dislocation creation [12]. Favored dislocation creation at the solid-liquid interface close to grain boundaries during crystal growth [26] as well as increasing dislocation density during the cooling phase [27] are reported.
Once created, the density of dislocations can be reduced by high temperature annealing steps. Using temperatures in the range of 1100 °C to 1350 °C and annealing times up to 6 h, reductions in dislocation density in the range of 20 % to 90 % are possible [12]. Longer annealing times and higher annealing temperatures generally favor dislocation density reduction. Yet, in mc-Si solar cell production, such high temperature annealing steps are typically not used, since in addition to costs due to energy and processing time, high temperature annealing can be detrimental to material quality due to dissolution of metal precipitates.
Controlling dislocation densities in mc-Si in practice is therefore chiefly a task of skillfully adjusting the block casting process.

2.3. Solar cell processing steps and their relation to material quality

Here an overview of the basic steps required for the production of a solar cell is given and the context and relevance of the processing steps that are used for this work are pointed out. Most of the processing steps, here discussed exemplarily for boron doped substrate material, fulfill multiple purposes at once, as shall be briefly highlighted.
Assuming a cleaned silicon wafer of suitable base doping as starting condition, necessary process steps for the creation of a reasonably well working solar cell must include the following (or functionally equivalent) steps:

- **A means for charge carrier separation. Here, creation of a pn-junction and gettering:** Any working solar cell has to achieve charge carrier separation in some way. The cause of charge carrier separation is best explained as a difference in conductivity of electrons and holes in the vicinity of two opposing contacts [28]. The often used model of charge carrier separation in the electric field of the pn-junction's space charge region is, surprisingly, no essential requirement for this process [28]. Here, the n doped side of a pn-junction provides a large conductivity for electrons and a small conductivity for holes, thereby causing a high electron concentration. The process for creating pn-junctions studied in this thesis is the diffusion of phosphorous from phosphosilicate glasses (PSG) into the boron doped silicon material. The diffusion process is facilitated by ambient temperatures of the order of 800 °C to 900 °C, resulting in an highly n-doped region of less than 1 µm depth, the so-called emitter. On the one hand, diffusion from high to low concentration is happening for phosphorous that diffuses from the PSG into the wafer. On the other hand, there is a gradient in the concentration of metallic impurities from the PSG layer (low impurity concentration) towards the silicon material (high impurity concentration). In this way, high temperature diffusion processes facilitate a reduction of the impurity concentration in the silicon material. This so-called (external) gettering, can drastically enhance the material quality. In this thesis, material quality changes due to gettering are characterized, and novel insights into the behavior of dislocation defects and defect etching could be gained.
- **Surface passivation, anti-reflex coating and hydrogen passivation:** Opposing to the time that is required to complete the process of charge carrier separation is the lifetime of minority charge carriers, i.e. their recombination activity. The dominant contribution to the recombination activity, here originating from the untreated wafer surface, can be reduced by surface passivation: The presence of dielectric layers on the wafer surface can strongly reduce the recombination activity, either by repelling charge carriers from the silicon surface through electrical fields (field effect passivation) or by saturating dangling and open silicon bonds on the wafer surface (chemical passivation). While a minimum thickness of the passivation layer is required for it to be effective, the layer thickness beyond that is a free parameter that can be optimized to second as an anti reflex coating (ARC). As a third beneficial aspect, substances that are used for ARC and passivation, such as silicon nitride or aluminium oxide, can be made to contain large amounts of hydrogen, that in turn can passivate dangling bonds in the silicon bulk and thereby greatly improve electron-hole-lifetimes.
- **Metallization for front and rear contacts:** For electrical contact between a solar cell and external circuits, a metal-silicon interface is required. Typically, special metal pastes are screen-printed onto the wafer surface that electrically contact the silicon material after a fast firing step.
- **Contact formation and hydrogen redistribution:** During fast firing, a

brief heat-up to temperatures between 800 °C to 950 °C or more, the contact between the silicon material and the metal terminals are formed. Besides this, the passivation quality of substances like silicon nitride and aluminium oxide drastically improves with firing. Lastly the firing step redistributes hydrogen in the silicon material and releases hydrogen from the passivation layers into the silicon bulk, facilitating chemical passivation of internal states.

In practice, some more steps may be beneficial or necessary: Typically, edge isolation is needed to make sure that the only electrical contact between front and back side of the solar cell is via the space charge region. Texturing the wafer surface can increase the amount of light entering the wafer as well as reduce the amount of light that exits the wafer. Various advanced architectures for solar cells have been developed, that improve upon many aspects of such basic cell designs: Several ways for passivating metal contacts are used in practice that have a strong impact on cell efficiencies. Bi-facial solar cells allow for light entering from the front- as well as from the back side. Other designs manage to totally avoid metal contacts on one wafer side, such that no light is blocked by metallization.

Chapter summary

In this chapter, the fundamental observable for the state of material quality, τ_{eff}, has been introduced and the various ways for charge carrier recombination have been discussed. Dislocations and their interplay with material quality as well as their capability to become mobile have been summarized. In addition, the steps to create a simple solar cell and the interplay of each step with the material quality have been highlighted.
The following chapter describes the experimental methods for studying the material quality that are used throughout this thesis, thereby giving an impression of the untreated state of the material.

3. Material characterization and methods for analysing the defect structure

In this chapter, the measurement techniques that are used here to analyse the mc-Si material quality are presented. For the characterization techniques that are central to this thesis, measurement results of the so-called 'as-grown' state, the material after basic cleaning steps only, are discussed.

3.1. Material properties

The material studied here is industry standard boron-doped mc-Si with a nominal resistivity of $1\,\Omega\,\mathrm{cm}$. The wafer material is sorted according to the column position in the block, i.e. it is known whether wafers are from the border, edge or center of the mc-Si block (figure 3.1) and wafers are numbered according to their position in the column, starting with wafer number 1 at the bottom of the useable part of the block. Therefore, it is possible to select wafers that originate from the same location of the silicon block: Sets of wafers from the same column that are neighbors in the direction of crystal growth, so-called sister wafers, naturally exhibit a highly similar grain structure, material quality and a high correlation of the density and location of defect structures. Throughout this work, comparisons between differently processed sister wafers are used to identify the influence that certain processing steps have on the material.

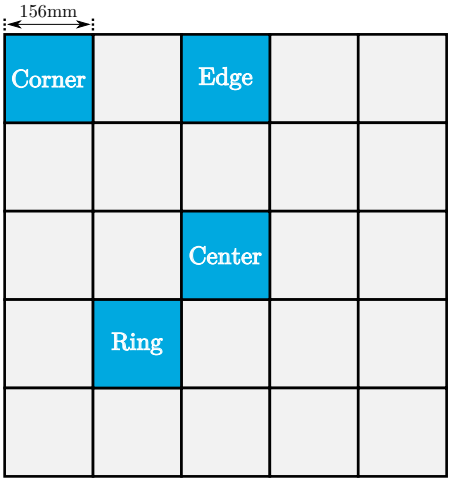


Figure 3.1.: A schematic drawing of the mc-Si block and the ingot positions from which wafer material could be accessed for this thesis (labeled and marked in blue). Results from the edge and ring are presented here.

3.2. τ_{eff}-based measurements

Due to the high sensitivity of τ_{eff} to impurity concentrations and the well established correlation with solar cell efficiency, τ_{eff} is a key observable for silicon material quality [29]. In addition, measurements of τ_{eff} can be used to infer the interstitial iron concentration $[Fe_i]$ [30] [31]. Measurements of τ_{eff} and $[Fe_i]$ as well as other measurements will be used to characterize the gettering steps (sections 4.2.1, 4.4.1) that cause the effect of EPD reduction.
For the measurement of τ_{eff}, so-called lifetime samples are prepared, i.e. wafer samples that, in contrast to solar cells, do not feature metallic terminals and for which the emitter region is removed. Thereby, material quality improvements due to gettering can be seen free from negative influences due to enhanced recombination in the emitter region and free from shading and enhanced recombination at metallic terminals. In the following, it is shown how lifetime samples are prepared and measurement results of the as-grown material state are discussed.

3.2.1. Sample preparation for τ_{eff}-based measurements

Wafers are obtained from mc-Si blocks by a sawing process, for which typically either a diamond-plated wire or, as it is the case for the material used in this thesis, an un-plated wire and sawing slurry is used [32]. The sawing process damages the wafer surface mechanically and introduces impurity elements, e.g. due to auto-abrasion of the sawing wire [32]. Therefore, 10 µm of material per wafer side are removed from the as-cut wafer material. This material removal is performed chemically in two steps. The first 5 µm are removed in hot KOH, the remaining material is removed in a chemical polish (CP) solution consisting of 5 parts HF (50 %), 12 parts acidic acid (99.8 %) and 75 parts nitric acid (65 %).

The wafer surface is then cleaned by reaction with piranha solution, a mixture of three parts H_2SO_4 (30 %) and one part H_2O_2 (95 % to 97 %), followed by a dip in diluted HF. Piranha solution is a strong oxidizing agent, capable of dissolving organic material and oxidizing the silicon surface. The oxidation reaction comes to a natural end when the whole wafer surface has reacted. The subsequent HF dip removes the surface oxide, thereby creating a fresh silicon surface and loosening particles and metallic contaminations that are attached to the surface.
Cleaning the wafer in this way is essential to avoid redistribution of contaminants in subsequent high temperature steps, that would otherwise severely degrade material quality.

Even after these cleaning steps, the largest contribution to charge carrier recombination for the wafer material that is used in this thesis, arises due to the wafer surface - the abrupt end of the crystal lattice [33]. Material quality in the wafer bulk becomes relevant only when the influence of the surface can be reduced. This can be achieved by depositing dielectric materials on the wafer surface [33] [34]. This passivation of the surface reduces recombination activity on the surface by two means:

- Dangling bonds at the crystal end can be chemically terminated and thus their negative influence as SRH recombination centers can be reduced. (Chemical passivation)
- SRH recombination of electron and holes at recombination active energy states originating from the wafer surface can be reduced by passivation layers that introduce localized electric charges to the wafer surface. Depending on the charge sign, the electric field reduces the density of either electrons or holes at the wafer surface, thereby suppressing SRH recombination. (Field effect passivation).

Passivation of lifetime samples throughout this work is achieved by hydrogen enriched silicon nitride layers ($SiN:H_x$) of at least 75 nm thickness and a refractive index at a wavelength of 633 nm of $n_{633} = 2.01$. The deposition of these layers is conducted at 450 °C with a Centrotherm plasma enhanced chemical vapor deposition (PECVD) machine, a direct-plasma device operating at a plasma frequency of 40 kHz. For $SiN:H_x$, the passivation mechanism is a mixture of chemical and hole-repelling field effect passivation [35] [33].

As a last step, samples undergo a fast firing procedure, a brief heating of the samples with a peak temperature set value of 850 °C. In solar cell processing, this step facilitates contact formation between external metal contacts and the silicon material [3]. This fast firing step greatly improves the passivation quality of the $SiN:H_x$ surface layer [34]. Additionally, chemical passivation in the bulk is influenced, since the high temperature step modifies the distribution of hydrogen throughout the material [3] [33] [34].

3.2.2. Measurement of τ_{eff}

3.2.3. τ_{eff} from photoconductance decay measurements

It is possible to infer τ_{eff} from simultaneous measurements of the illumination of a silicon sample and its photoconductance, the latter of which is modified by the creation of free charge carriers [36] [37]. The excess charge carrier density Δn can be written in terms of charge carrier generation rate G, recombination rate $\frac{d\Delta n}{dt}$ and effective carrier lifetime τ_{eff} as [8]

$$\Delta n = \tau_{\text{eff}} \left(G - \frac{d\Delta n}{dt} \right). \tag{3.1}$$

Measurements of τ_{eff} via photoconductance decay (PCD), as used for this thesis, are carried out in quasi steady state conditions, i.e. illumination times are much longer than τ_{eff}, resulting in a constant charge carrier density $\frac{d\Delta n}{dt} = 0$. This simplifies equation (3.1), such that only G and Δn are required for determining τ_{eff}. In these conditions, equation (3.1) can be rewritten, using the measured conductance σ_L, the well-known charge carrier mobilities μ in silicon and the measured photogeneration current density J_{ph} as [37] [36]

$$\tau_{\text{eff}} = \frac{\Delta n}{G} = \frac{\sigma_L}{J_{\text{ph}}(\mu_{\text{n}} + \mu_{\text{p}})}. \tag{3.2}$$

In practice, a flash lamp is used for illumination that provides a slowly (relative to τ_{eff}) decaying light pulse during which the photoconductance as well as the photogeneration current density are recorded as a function of time. Steady state conditions are satisfied in each moment of the light pulse decay, when the decay constant τ_{flash} of the flash is a factor of 10 larger than τ_{eff} [38], ensuring that for each moment in time, equation (3.2) is applicable. In this way, a single measurement is sufficient to determine the lifetime at various injection levels, i.e. throughout the decay process of the flash light.
Conversely, measurements of material with large τ_{eff} are measured with a short and quickly decaying light pulse [37]. In this case the decay of photoconductance is continuing while the illumination has already come to an end, corresponding to a generation rate $G = 0$ in equation (3.1), the condition for the so-called transient measurement mode. In this thesis, PCD measurements are used for calibration of photoluminescence (PL) imaging measurements, that in turn provide spatially resolved lifetime maps. The PL setup used in this thesis requires quasi steady state conditions for calibration [39], therefore the transient measurement mode can not be used.
A Sinton WTC-120 PCD tool was used for quasi steady state photoconductance (QSSPC) decay measurements [38]. The flash lamp that is used for illumination in this setup is operated at its maximum decay constant of approximately 2000 µs, allowing material with lifetimes of up to 200 µs to be at quasi steady state conditions throughout the decay of the flash [38]. However, the mc-Si material that was studied

here can contain grains with peak effective lifetimes up to 400 µs next to regions with lifetimes an order of magnitude lower. Quasi steady state conditions are then fulfilled only in some regions of a given wafer, resulting in a systematic overestimation (corresponding to a term $\frac{d\Delta n}{dt} < 0$ in equation (3.1), implying that equation (3.2) is not applicable) of lifetime results of QSSPC calibrated photoluminescence images when such high lifetime grains are contained. While a generalized measurement method is available that can take into account all terms of equation (3.1) [40], ultimately the calibration of PL data and the technique for measuring the interstitial iron concentration that is used throughout this work requires calibrated photoluminescence images on the basis of quasi steady state measured lifetimes.

3.2.4. Spatially resolved τ_{eff} with calibrated photoluminescence imaging

While QSSPC measurements result in a single average value for the area in which the photoconductance is measured, photoluminescence (PL) imaging [39] offers spatially resolved τ_{eff} measurements. In the context of mc-Si material quality analysis, the possibility to spatially resolve τ_{eff} within individual grains and at grain boundaries is very valuable. This section follows explanations found in [39].
With PL imaging, photons from the radiative recombination channel are measured. In regions of high SRH defect density, the SRH recombination channel dominates and radiative recombination is low. Auger recombination strength can be estimated from carrier injection and is a sub permille effect at the injection levels used here. Therefore regions with a strong PL signal correspond to wafer regions of low SRH recombination, i.e. regions of high material quality. In practice, the sample is illuminated at low wavelengths ($\lambda_{\text{LED}} = 630\,\text{nm}$) and recorded by an image sensor that is located behind a GaAs wafer acting as step filter. The band gap of GaAs corresponds to a wavelength of $\lambda_{\text{GaAs}} = 875\,\text{nm}$. With a wafer thickness of 350 µm and GaAs being a direct semiconductor, near perfect blocking of wavelengths $\lambda < \lambda_{\text{GaAs}}$ is ensured while PL photons from radiative recombination through the silicon band gap with a wavelength of about 1100 nm can pass the filter wafer. The recorded PL intensity can be calibrated with τ_{eff} information from QSSPC measurements such that the PL intensity image is transformed to a map of τ_{eff} [39]. Two sources of uncertainty arise due to PCD calibrations of PL data: As discussed, quasi steady state conditions can, due to the limited illumination times of the flash setup, not be fulfilled in high-lifetime grains. This biases the lifetime values measured via the QSSPC method and the QSSPC-calibrated PL results towards large lifetime values. The PL measurement takes place at true steady state conditions, i.e. the PL signal is measured during continuous illumination, so no further bias is expected at this stage. Secondly, unlike the PCD's flash setup, a thermal radiator, the light source that is used in the PL setup excites charge carriers close to the surface. Therefore differences are expected if surface passivation is not perfect, i.e. when $\tau_{\text{eff}} \approx \tau_{\text{bulk}}$ is not fulfilled [39]. PL measurements of the as-grown material recorded

in this fashion (figure 3.2) show the typical inhomogeneous distribution of lifetimes that is expected for mc-Si material. Naturally, the spatial resolution is limited by the diffusion length $L(\tau_{\text{eff}}) = \sqrt{D\tau_{\text{eff}}}$, which is on the order of 0.5 mm at lifetimes of 100 µs.

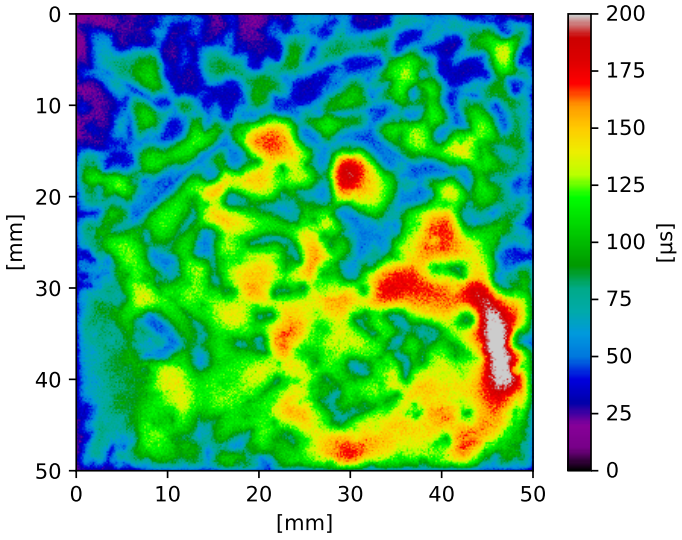


Figure 3.2.: QSSPC calibrated PL image of a square mc-Si wafer with 50 mm side length in the as-grown state, i.e. after saw damage removal, cleaning and SiN:H_x passivation and fast firing.

3.2.5. Interstitial iron concentration

With deep-level transient spectroscopy (DLTS) measurements in boron doped silicon, it can be shown that recombination-active iron atoms occur in two states in the silicon bulk, that can be identified as iron in an interstitial lattice site (Fe_i) and iron-boron pairs (FeB) [30]. Iron in the form of FeB pairs can be dissociated into interstitial iron by elevated temperature or by illumination [30]. During extended dark storage at room temperature, iron relaxes into bound FeB pairs [30]. The method for determination of [Fe_i] that is used here makes use of the fact that for most excess charge carrier concentrations, the recombination activity of iron in interstitial form differs strongly from iron in form of FeB pairs [31]. For the above shown measurement of τ_{eff} (figure 3.2) the wafer has been illuminated for 45 s with a photon flux of approximately 1 sun equivalent, thereby preparing a state where FeB pairs have been dissociated into separate boron and (mobile) interstitial iron atoms. Longer illumination times do not show further increases in lifetime, hence repeatable dissociation conditions are assumed. Lifetime maps that are recorded after dark storage at room temperature for more than 24 h (figure 3.3) exhibit a clear difference in recombination activity compared to samples that have been previously illuminated (figure 3.2). For recording these images, a photon flux of

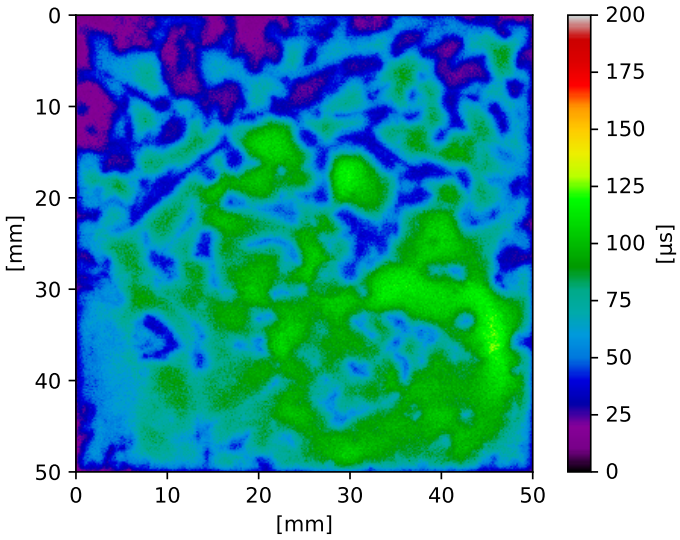


Figure 3.3.: QSSPC calibrated PL image of the very same wafer depicted in figure 3.2, here recorded after dark storage, i.e. in a state where iron is present in the form of FeB pairs.

$2.6 \times 10^{17}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ for the duration of 0.1 s is used: a low total illumination, so that breaking of FeB pairs is kept at a minimum, yet strong enough to still result in a reasonably strong PL signal. Illumination time is exceeding the expected τ_{eff} values by several orders of magnitude, so that steady state conditions of the charge carrier density, as required for PL calibration, is ensured.

From these measurements of effective carrier lifetimes before (τ_0, figure 3.3) and after breaking of FeB pairs (τ_1, figure 3.2), the interstitial iron concentration [$\mathrm{Fe_i}$] of each pixel can be obtained (figure 3.4) as [31]

$$[\mathrm{Fe_i}] = C\left(\frac{1}{\tau_1} - \frac{1}{\tau_0}\right), \tag{3.3}$$

with C containing the electron-capture coefficients of $\mathrm{Fe_i}$ and FeB [30][31].
The recombination activity of FeB and interstitial iron defects changes as function of the charge carrier concentration: At low illumination (low carrier concentrations), the recombination activity of interstitial iron exceeds the recombination activity of FeB pairs. For high carrier concentrations, this behavior is inverted. At some point in the middle regime, depending on boron dopant concentration typically in the range of $10^{13}\,\mathrm{cm}^{-3}$ to $10^{15}\,\mathrm{cm}^{-3}$ [41], the recombination activity of both FeB pairs and interstitial iron are equal. At this so-called crossover point, no difference in lifetime between the two states is measured and equation (3.3) can not be used for determining [$\mathrm{Fe_i}$]. Consequently, measurements of [$\mathrm{Fe_i}$] should be carried out at some distance to the crossover point so that adequate signal strength is ensured. Measurements of [$\mathrm{Fe_i}$] that are shown in this work have been performed at high carrier concentrations, therefore splitting of FeB pairs leads to an increase in observed lifetimes. The discussed problem that quasi steady state conditions

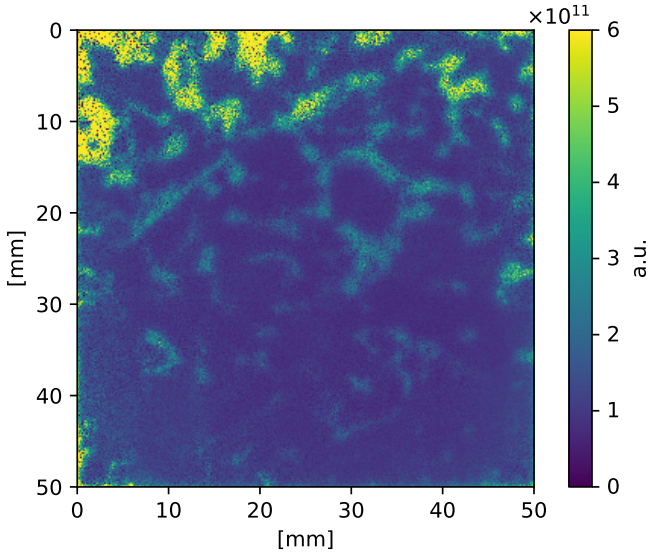


Figure 3.4.: Interstitial iron concentration [Fe_i], calculated from data of figures 3.2 and 3.3. As explained in the text, relative values between two identically prepared samples offer meaningful results, the discussed restrictions of the measurement procedure, however, lead to the conclusion to only use a scale of arbitrary units for single measurements.

can not be fulfilled for QSSPC measurements in well-performing grains, therefore has a stronger influence on measurements after FeB pair dissociation. This bias in the calibration procedure results in an overestimation of [Fe_i] values. Since charge carrier steady state conditions are fulfilled during the PL measurement, relative comparisons of the [Fe_i] signal within the same sample are unaffected by this uncertainty.

An additional systematic uncertainty in [Fe_i] results arises due to the unknown preparation state of the associated and dissociated state of FeB pairs at the time of measurement: some unknown amount of dissociation is happening due to the light needed for the measurements themselves. Conversely, an unknown amount of FeB re-pairing might happen, between the time the sample is dissociated and the measurement is executed. It has been shown that for mc-Si material with a boron doping concentration of $1.5 \times 10^{16}\,\mathrm{cm}^{-3}$, i.e. similar material to what is used here, even continuous illumination with up to 11 suns does not result in full dissociation of FeB pairs [42]. Required illumination strengths for full dissociation varies with the material properties [42]. Authors using optical activation with a 10 sun equivalent intensity for 1 min assume full dissociation [31]. No such illumination sources have been available for this work. Based on the results of [42], illumination as used here (about 1 sun for 45 s) results in about 20 % to 25 % dissociation. Partial dissociation can be dealt with a simple correction factor f for the interstitial iron

concentration [30], changing equation (3.3) to

$$[\mathrm{Fe_i}] = \frac{C}{f}\left(\frac{1}{\tau_1} - \frac{1}{\tau_0}\right). \tag{3.4}$$

The multitude of effects that contribute to the uncertainty of $[\mathrm{Fe_i}]$ measurements lead to the decision to use a scale of arbitrary units (a.u.). The ratio of two such measurements with identical means of preparation (and therefore identical f) are independent of f, so relative changes in $[\mathrm{Fe_i}]$ between two samples are a valid measure.

In the as-grown state, $[\mathrm{Fe_i}]$ (figure 3.4) is strongly correlated with low τ_{eff} regions. More refined conclusions can be drawn when comparing changes in $[\mathrm{Fe_i}]$ after gettering processes (sections 4.2.1, 4.4.1)).

3.3. Etch pit density analysis on mc-Si material

The main achievements presented in this thesis are related to measurements of the etch pit density as seen after defect etching processes. Here, the defect etching process and the subsequent computer based analysis of the resulting data as well as the data presentation will be described. This section uses [43] [44]

Defect etching is a chemical technique by which crystalline material can be etched selectively at sites of crystallographic defects. Selective etching results in small holes at defect sites, so-called etch pits, whereas ideally the surrounding crystal remains unchanged. Often the etch pit density (EPD) is seen as a synonym for the dislocation density, and indeed most etch pits are due to dislocation defects [45]. Other defects such as stacking faults or precipitates can result in localized etch structures after defect etching, too, and different defect etch solutions vary in their capability to delineate defects of a certain kind [44].
Various chemical techniques for general etching of silicon material, such as the already discussed chemical polishing and cleaning steps, are used in semiconductor technology. Acidic solutions for etching silicon consist of two components: a strong oxidizing agent that is capable of oxidation of silicon atoms bound to the crystal lattice and HF as second component, which is capable of dissolving the resulting silicon oxide. If only the oxidizing agent is present, the oxidation reaction comes to an end after a few nanometer thick SiO_2 layer has been formed. If additionally HF is present, oxidation of silicon and dissolution of SiO_2 take place simultaneously and material is removed.
For defect etching, the strength of the oxidizing agent is critical: Silicon atoms that are part of a defect are bound to the crystal less strongly than atoms that are part of the undisturbed lattice. A suitable oxidizing agent for defect etching is able to enter a reaction with the weakly bound atoms belonging to a defect but not with silicon atoms that are part of the undisturbed lattice. The additional presence of HF leads to material removal only in regions close to weakly bound

silicon atoms. The weakening of bonds between silicon atoms close to dislocations is generally accepted to be a consequence of strain fields that are associated with the dislocations [44].
Apart from this model concept, surprisingly little is known about the etching process that leads to the development of etch pits and comparable defect features [44]. It is not understood why different kinds of defects are delineated with varying results by different defect etch solutions. Many solutions, such as the Secco [46], Schimmel [47] and Wright [48] etch, use compounds that contain chromium in oxidation state +6 as oxidizing agent for which in the literature an explicit lack of understanding of the etching process is reported [45].
For applications that require a defect etch free from metallic compounds, HNO_3 can be used as oxidizing agent: Various compositions of HF, HNO_3, water and acidic acid are used for etching silicon in various applications. There are phenomenological studies about the behavior of various mixtures of these components [49] [50] [51] [52]. For mixtures with high HF content, as they are used for defect etching [53], however, it is reported that "the reaction becomes very complex" [51] and there are only speculations about the mechanism in the literature [51]. Oxidizing agents of suitable strength and their relative concentration are found by trial and error and resulting defect etch solutions sometimes exhibit surprising behavior: Some defect etch solutions do not form etch pits by preferentially removing material at the defect site, but exhibit the opposite behavior, i.e. all but the material close to a defect site is removed, resulting in in the formation of hillocks instead of etch pits. Such hillock-etching techniques have applications in transmission electron microscopy studies when it is important that the defect itself is still present for subsequent analyses [54]. For the so-called Sirtl etch, it is reported that a reduction of the processing temperature is sufficient to switch from an etch-pit to a hillock-forming behavior [55]. Again, the principles that govern such behavior are not understood. Despite the lack in detailed mechanistic understanding of the defect etch process, for more than half a century these techniques are and have been one of the most important tools for studying extended defects in crystals. A main concern of this thesis are novel discoveries regarding defect etching in combination with phosphorous diffusion gettering.

Publications concerned with EPD measurements in mc-Si material often estimate the EPD based on flatbed scanning images [20] [19] [16] or use indirect measurements of the EPD [56]. Optical microscope images with sufficient precision to directly observe etch pits and therefore directly measure the EPD, are typically only used as reference images for very small regions [19]. Here, the aim is to combine the precision of optical microscope images, sufficient for counting individual etch pits, with large analysis areas of several cm^2 size. In the following section as-grown material is used as an example to discuss the process and results of defect etching: This includes details on how wafers are prepared, defect etching is executed and how optical microscope data is reduced to EPD values. The analysis tool used to obtain EPD data from images of etched mc-Si wafers has been published in combination with [2]. Parts of the following sections are based on this publication.

3.3.1. Sample preparation for defect etching

Defect etching is negatively influenced by rough surfaces [46], therefore many defect etches are applied on polished surfaces [46] [47] [48] [53]. For EPD measurements using flatbed scanning, chemical polishing results in surfaces that are sufficiently smooth for the subsequent analysis procedure [20]. For computer aided etch pit counting that is capable of detecting individual etch pits, it is crucial that prior to defect etching, the wafer surface appears featureless when analysed with the optical microscope. Wafer surfaces after chemical polishing retain some surface roughness, resulting in structures that exhibit comparable contrast to etch pits when analysed with the optical microscope. Therefore chemically polished material has been found unsuitable for computer aided EPD analysis in our study. Instead of chemical polishing, chemo-mechanical polishing of individual samples is used, resulting in surfaces that appear perfectly smooth on magnification scales used in the optical microscope.
Proper polishing is an essential part to the results presented in this thesis. It is a time consuming process and therefore takes considerable time to master, especially when defect etching is done in bulk. Therefore, the practical experience in polishing mc-Si material that was acquired while working on this thesis has been documented in detail in the appendix (section A.2). The following is an overview of the necessary steps:
Samples are laser-cut to a size of 25 mm × 12 mm. The 12 mm side length is a restriction placed by the electron backscatter diffraction measurement technique, which has been used for some studies that are not presented in this thesis, and the side length of 25 mm corresponds to half the wafer size used for lifetime samples, therefore allowing two rows of EPD samples per lifetime sample.
In preparation for the polishing procedure, the sample is glued onto a jig (Logitech PP6). Proper glueing attaches the sample in a plane-parallel fashion to the jig's head and prevents the sample from breaking as well as the wafer edges from chipping. At certain grain boundaries, however, some damage during polishing is hardly avoidable, i.e. occasionally in all wafers of a batch of sister samples the same grains become loose.
Polishing of the glued sample is done with a Logitech PM5 Polishing System in two steps. With the first step, the sample surface is flattened and with the second step, the flat surface is polished, i.e. surface roughness is reduced below structure sizes visible in the optical microscope. Flattening is a wet abrasion process, for which sand papers with a grain size of 10 µm have been found suitable. Polishing is done using an alkaline colloid solution of SiO_2 of 0.032 µm grain size (LOGITECH Syton Typ SF1) on an aluminium-oxide foam plate. This step produces a homogeneous, mirror-like surface that is perfectly suited for contrast-based detection of etch pits in optical microscope images. A challenging problem is that the polishing results can not be judged immediately: Surfaces that seem perfectly devoid of scratches and marks under the optical microscope can still reveal scratches after the defect etching process.
The combined material removal of flattening and polishing has been estimated

to be $21.0 \pm 5.3\,\mu m$. This estimation is based on thickness measurements of seven different samples, taking thickness measurements in the wafer center. More material is removed close to the wafer edges.
After polishing and removal of the wafer from the jig, the wax used for glueing the wafer to the jig has to be removed. Two cascades of hot piranha solution (10 min each) followed by a dip in diluted HF have been used to reliably free samples of wax residue. Varying storing times in air can influence defect etch results, so a further advantage of this cleaning procedure is that it ensures repeatable initial conditions, when the second HF dip is done immediately before the defect etching step.

3.3.2. The defect etch process with the Secco etch

Various chemical solutions have been developed for the selective etching of defect sites on silicon and other semiconductors. In this work, chiefly the so-called Secco etch [46] is used, which is known to delineate defects on silicon surfaces of all crystallographic orientations. This makes the Secco etch well suited for studies on mc-Si material. Additionally, etch pits with suitable contrast for detection with optical microscopy are obtained with well controllable etching times in the range of minutes.
The Secco etch is used in a composition consisting of two volume parts HF with a concentration of 50 % and one volume part of a 0.15 molar solution of potassium di-chromate ($K_2Cr_2O_7$), providing hexavalent chromium as oxidizing agent. Right before the etching process, the polished wafers are dipped in diluted HF, removing the oxide from the previous piranha cleaning step, creating a fresh silicon surface and therefore repeatable initial conditions. During the etching process, the Secco etch is agitated in an ultrasonic bath, which suppresses the sticking of gas bubbles to the silicon surface that would otherwise result in characteristic circular regions off less pronounced etching. Besides the suppression of these artifacts, ultrasonic agitation reduces etching times.

An experiment not shown here, during which the same wafer was repeatedly etched for short time durations to slowly accumulate larger etch times, has shown that below a certain minimum etch time, only a fraction of etch pits on a wafer appear with sufficient contrast for reliable analysis. In case of the Secco etch it could be shown that etch times of 60 s or longer create etch pits of sufficient size for consistent detection with the optical microscope and that etch times between 60 s and 120 s produce similar EPD results in low, mid and high EPD regions. Comparison of scanning electron microscope (SEM) and optical microscope image data after a 60 s Secco etch (figure 3.5) confirm a one-to-one correspondence of regular sized etch pits between both microscope techniques, thereby confirming that the resolution achieved with the optical microscope is sufficient for detection of individual etch pits even for short etch times. Defect etching in this work is done with a 90 s Secco etch, unless explicitly stated otherwise.

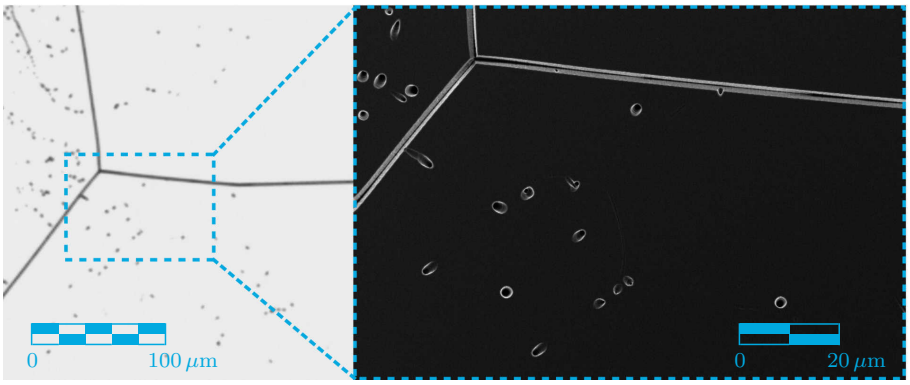


Figure 3.5.: Comparison of etch pit image data from optical (left) and scanning electron microscopy (right) after 60 s Secco etch, demonstrating that after proper mechanical preparation and defect etching, the resolution of optical microscope image data is sufficient for the detection of individual etch pits. In this thesis, mostly etching times of 90 s are used, leaving an additional safety margin.

3.3.3. Recording of optical microscope data

Images of the etched wafer surfaces are recorded using a Zeiss Axio optical microscope at 50x total magnification (5x magnification lens, 10x eyepiece/camera). Wafer sizes for EPD analysis of 25 mm × 12 mm at this magnification result in images sizes of about 6.2×10^8 pixels. Higher magnification and thereby further increased image sizes would unnecessarily complicate image modifications on typical office computers. Since with this minimum magnification, individual etch pits can be resolved easily, no attempts to increase magnification have been considered. Images are exposed as bright as possible while at the same time ensuring that etch pits retain a few perfectly black pixels. Sister wafers are exposed under identical conditions. Resulting images are stitched into a single file with Zeiss ZEN (version 2.0.0).

3.3.4. Computer aided etch pit density analysis

In this chapter the steps of the computer based etch pit analysis are described such that the analysis process as well as the resulting EPD maps are understood correctly. Technicalities are mentioned only where they are of importance to the interpretation of the results.

Distinguishing between interesting structures on the wafer and the wafer surface (background) relies on contrast between background and structures of interest. Separation is achieved by converting the gray scale microscope image to binary image data using a threshold value: A pixel with a gray scale value below the threshold value is stored as 0, all pixels above the threshold are stored as 1. Resulting regions of connected ones or zeros can be analysed with existing algorithms, such as

regionprops of the Python package *scikit-image* or the *regionprops* implementation in Matlab. Executing *regionprops* on a binary image containing connected structures generates a list-like object that for each structure contains a set of properties, such as a structure's center of mass coordinate or its size in pixels, etc. This principle of etch pit detection via thresholding and analysis has been presented by Needleman et al. [16].

Etch pits occur in one of three categories :

1. Isolated (single) etch pits
2. Groups of overlapping etch pits that are small compared to the size of a single pixel in the final EPD map. These etch pit conglomerates are typically found in mid-EPD regions
3. Regions where etch pits are so dense that they cluster together to a single structure (etch pit clusters). Etch pit clusters differ from conglomerate structures in so far that they are larger than a pixel of the final EPD map.

A distinction between these three cases (figure 3.6) has to be made. Structures belonging to case 2 consist of multiple etch pits. A good estimator for the number of etch pits that make up a conglomerate structure is obtained by dividing its size by the size of a typical etch pit. For case 3, further steps are necessary because etch pit clusters are typically much larger than a single image pixel in the resulting EPD map, therefore the shape of the etch pit cluster has to be considered. Additionally, etch pit clusters are often connected to grain boundaries, hence a distinction between grain boundaries and etch pit clusters has to be made. After separation of grain boundaries and etch pit clusters, the cluster's EPD has to be estimated. Subsequently, the location information of etch pits within the cluster is obtained by uniformly distributing etch pits onto the cluster area until the estimated EPD is reached. Finally, location information (x,y) of etch pits of all three cases are saved to disk, from which an EPD map can be inferred. The following details the procedures of these steps.

Counting algorithm

A few manual steps are required before the algorithm can be run. First, images are cropped, such that only the wafer surface is part of the image (figure 3.7). If parts of the image are not suited for analysis, e.g. due to heavily scratching or surface stains, these regions are removed from the image. Heavily scratched areas typically are found in the sample's corners.

Finally, a suitable threshold value must be determined. A typical image editor such as GIMP can be used to apply the threshold function and visually compare the structures in the resulting binary image with the etch pits seen in the original image. As many etch pits as possible should have a corresponding structure in the binary image whereas no noise from the background should appear. Typically, most parts of the wafer can be exposed such that there is clear contrast between etched

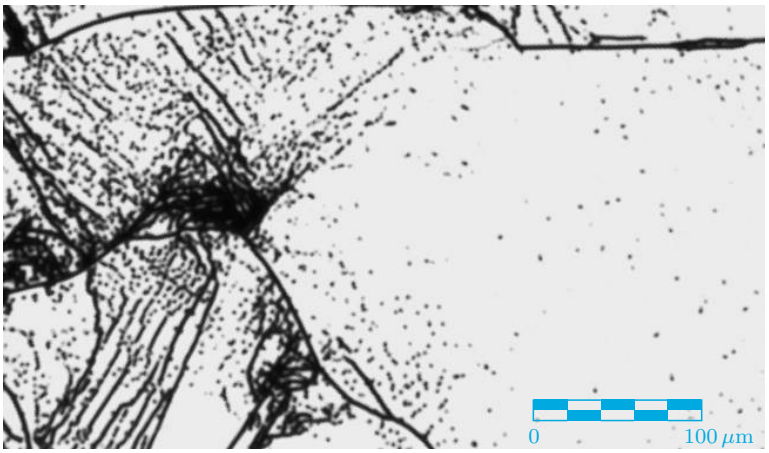


Figure 3.6.: Optical microscope image of a typical mc-Si wafer region after defect etching, showing clustered regions of high EPD, next to regions of mid and low EPD. Low EPD regions feature individual etch pits (e.g. bottom right), isolated structures in regions of medium EPD often correspond to conglomerates of multiple etch pits (e.g. top left), which are identified by size and weighted according to their relative area during etch pit counting. It is clear that for etch pit clusters, as seen in the left center, counting of individual etch pits is not possible. A lower limit for the EPD in clusters can be estimated based on the cluster area and the median area of isolated etch pits, as is described in the text.

structures and the wafer surface. In these cases there is a wide range of threshold values available that can be used with good results.
At times, certain grains develop a less reflective surface after defect etching and the wafer surface appears darker than in nearby grains. Especially in these regions, threshold values should be cross-checked for the appearance of noise. This phenomenon of dark grains and inter-grain contrast is relevant mostly for Wright etched samples and occurs in Secco and Schimmel etched samples far less frequent and in far less intensity. Investigations on the nature of inter-grain contrast are summarized in the appendix (chapter A.1).

After cropping and removing of scratches, an image can be fed to the algorithm where it is converted to a binary image using the previously determined threshold value. Next, a distinction between large and small structures is made: Two new binary images are created, one of which contains only structures below a certain size S and the other image containing all structures above the size S (figure 3.8). The resulting EPD map does not sensitively depend on S since for both, large and small structures, there is a similar check whether they consist of multiple etch pits. For etch pits of large structures, individual spatial coordinates are attributed, ensuring that etch pits from a large structure can contribute to multiple different pixels of the resulting EPD map. Therefore, S should be chosen smaller than the area of EPD image pixels.

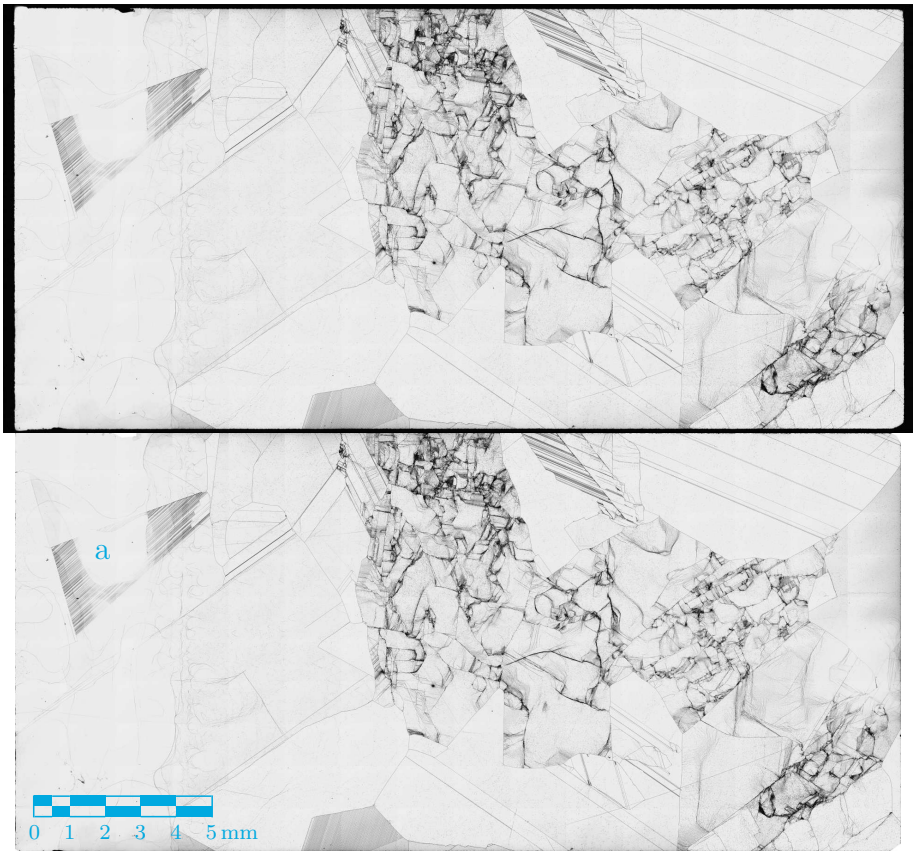
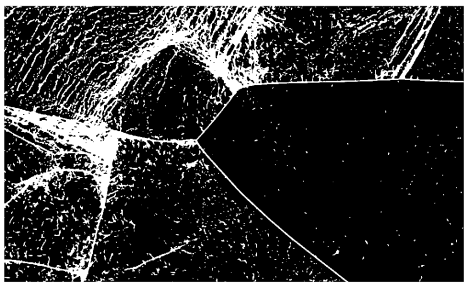


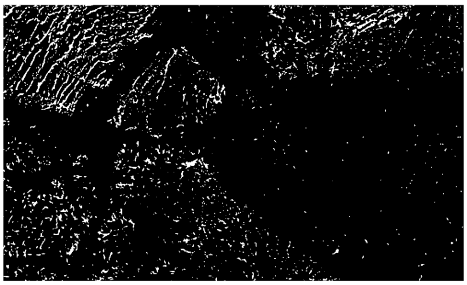
Figure 3.7.: Image of a defect-etched wafer as recorded by the optical microscope (top) and after manual cropping and masking (bottom). If necessary, scratched regions, typically found in the wafer corners, are removed. The leftmost 5 mm of the wafer are covered by the carrier during defect etching, therefore this region features highly uneven contrast (see grain with twin boundaries, marked as a). The region covered by the carrier is removed during the analysis.

Structures with sizes smaller than S are either individual etch pits, specs of noise (i.e. single pixels that exceed the threshold value) or etch pit conglomerates of a few etch pits, typically appearing in mid-EPD regions (figure 3.6). A distinction between these three cases can be made based on structure size and happens at a later stage. Structures larger than S can be surface stains or, more importantly, grain boundaries and clusters of etch pits (figure 3.6).

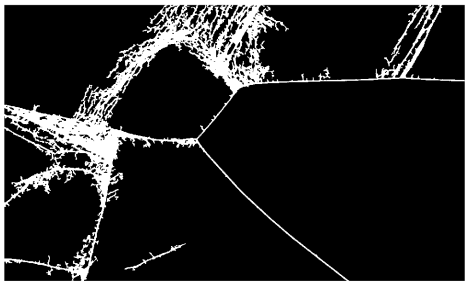
The image that contains the small structures only is analysed with *regionprops*. The center of mass location of the regions and their size in pixels are saved to disk. Separating noise from etch pit data and separating individual etch pits from etch pit conglomerates is done at a later stage.
While the analysis of small structures is straightforward, lots of the large structures are grain boundaries, a plane-like defect, that should not contribute to the density of etch pits that are due to line-like (and possibly some surface-close point-like) defects. Grain boundaries and defect clusters are often in direct vicinity and form



(a) Binary image



(b) Small structures



(c) Large structures

Figure 3.8.: The input binary image (a) is split into two images, one containing only small structures below a size S (b), the other containing the remaining large structures (c). The wafer section shown here is about 1 mm wide and only shows 0.2 % of the wafer surface that is analysed.

a single structure in the binary image. In addition, all grain boundaries of a wafer are connected with one another. Again, *regionprops* can potentially be used for distinction between grain boundaries (line structures) and etch pit clusters (cloud-like structures, often with holes), however, *regionprops* requires separate, disconnected structures. For this purpose, the image is superimposed with a square grid of white pixels, effectively subdividing large structures into smaller square tiles. The tile size should be chosen to be small compared to the grain size of the material. This assures that a typical grain boundary fragment within a tile is likely to be a straight line - a property that is used for distinction between grain boundaries and etch pit clusters. On the other hand, the tile size must be well above the thickness of etched grain boundary structures after thresholding, such that grain boundary fragments within a tile remain highly elongated structures. These criteria leave a wide range of suitable tile sizes. A tile size of 300 pixels corresponding to 210 µm, or about 30 to 50 times the thickness of a typical grain boundary, is used throughout this work. Variations of the tile size only have small effect on the grain boundary removal process as long as they remain within the discussed limits.
After splitting the image into tiles, *regionprops* is used for analysis of each tile's contents: The criteria for distinction between grain boundaries and etch pit clusters that are used here, are the eccentricity ϵ of an ellipse that has the same second central moments (measures for the regions shape) as the region in question, as

well as a region's Euler Number, a measure for the number of holes that a region contains. Regions with $\epsilon > 0.93$, i.e. structures highly elongated in one direction, are classified as grain boundaries. Secondly, regions with three or less holes are classified as grain boundaries. Another potentially promising decision variable, the ratio between the region area and the smallest convex polygon that can contain the region ('solidity'), has been studied and used in decision tree structures with the other mentioned variables. However, the above described simple separation by two parameters could not be reliably improved when using such decision trees. Regions classified as grain boundaries are discarded, the remaining regions are treated as etch pit clusters. With these simple criteria, most grain boundaries, twin grain boundaries and polishing scratches can be removed (figure 3.9).

The etch pit density in a cluster can be estimated from the pixel size of the image data, the cluster's size (the number of pixels that it contains) and the size (the number of pixels) A of a typical etch pit. The EPD in clusters, estimated in this way, constitutes a lower limit to the true EPD value and explicitly depends on A. While calculating A for each image separately is easily possible, the A dependant cluster EPD requires a constant value of A when sets of sister wafers are to be compared. Therefore, a fixed value of $A = 18$ pixels is used here, determined as the median etch pit size over a set of seven similarly etched wafers.

After splitting the large structures into tiles and after sorting grain boundaries from etch pit clusters, the algorithm fills up the area of etch pit clusters with uniformly distributed etch pits until the previously calculated EPD value is reached: For every cluster region, a list-like data object that contains the coordinates of all pixels that make the structure is obtained and reduced such that it contains only every A^{th} entry, with A the number of pixels of a typical etch pit. This reduced pixel list is saved to disk, providing the location information of etch pits in an etch pit cluster, based on the assumption that the whole cluster area is composed of etch pits of size A. Additionally, meta information about the analysis, such as the input image file's name and path, the used values for threshold, grain boundary detection (eccentricity ϵ, Euler Number and grid tile size), the assumed value for the etch pit size A in clusters and the magnification of the optical microscope setup is saved.

It is important to note that this procedure can only give a lower limit for the true etch pit density in clusters. In etch pit clusters, the distance between two etch pits can become smaller than the radius of a typical etch pit. In these conditions multiple etch pits can overlap with each other and the assumption that the area of an etch pit cluster is proportional to the number of etch pits that are contained in the cluster is systematically underestimating the true EPD in these regions. SEM images of etch pit clusters (figure 3.10) and EPD analysis of these images (figure 3.11) show that locally, clusters can exhibit EPD values that exceed the limit estimated by the described algorithm by more than an order of magnitude. It is noteworthy, that the size of the region shown in figures 3.10 and 3.11 corresponds to only 36 % of the size of a single pixel of the EPD map as used in this thesis. For many parts of a cluster, the estimated lower EPD limit is a good approximation.

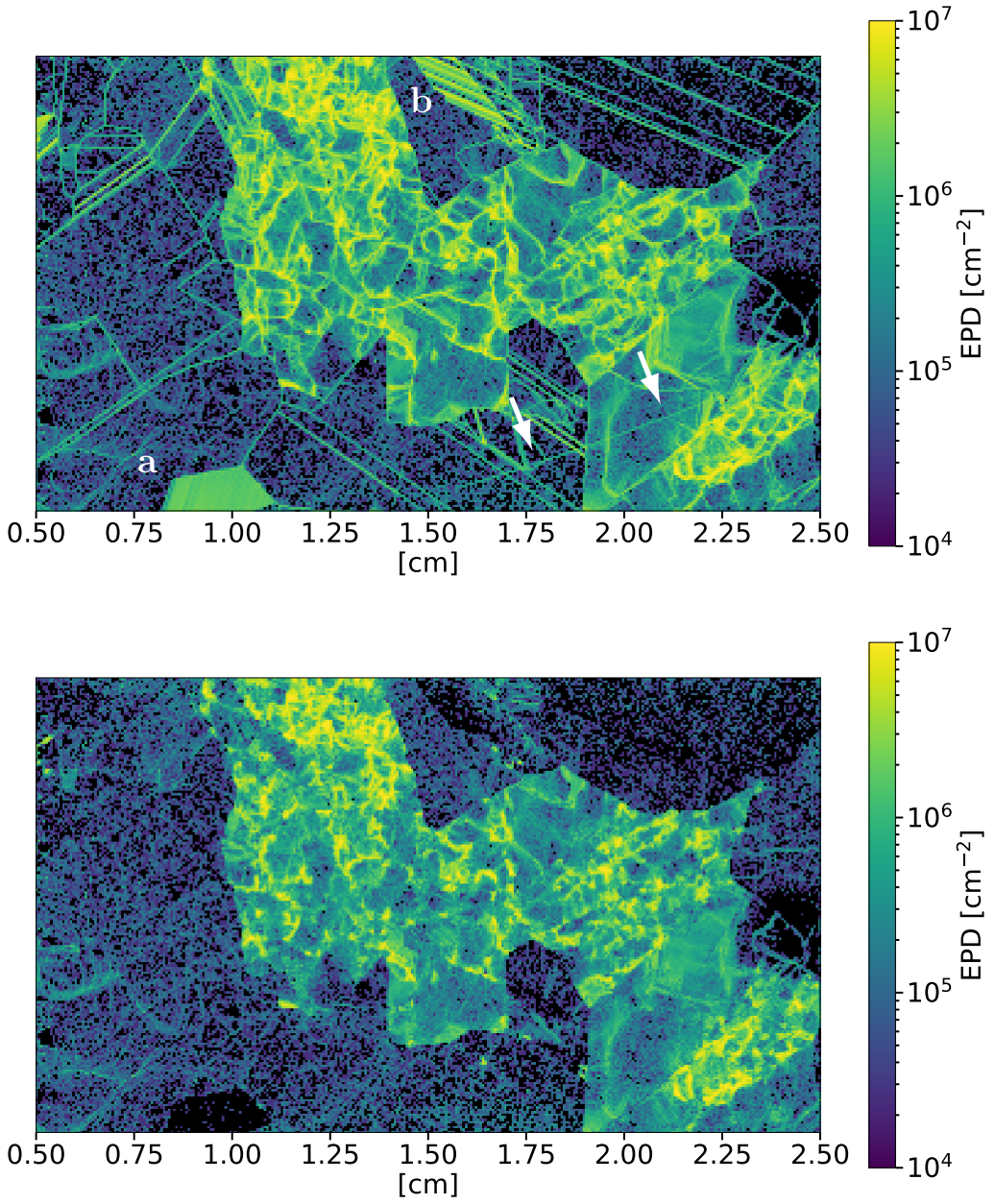


Figure 3.9.: Etch pit density analysis result before (top) and after (bottom) grain boundary removal. Regions with twin boundaries (marked "a" and "b") show meaningful values only after grain boundary removal. Polishing scratches (marked with arrows) are removed, too. The shape of etch pit clusters, however, can be influenced by the grain boundary removal process. With grain boundaries removed, only data due to etch pits is remaining, allowing for a further data reduction step (figure 3.13).

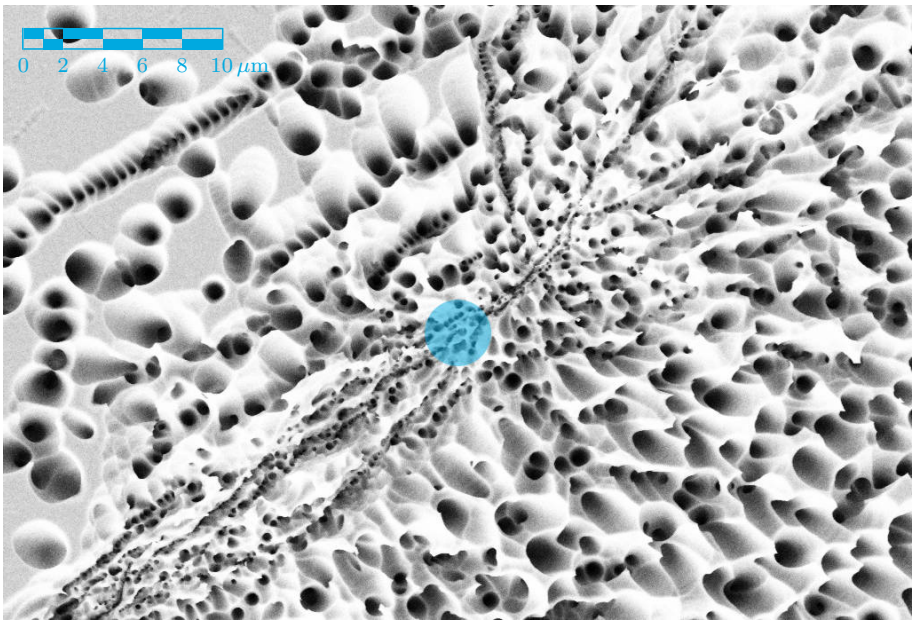


Figure 3.10.: Scanning electron microscope image of a high density region within an etch pit cluster. The blue semitransparent circle corresponds to A, the area of a typical etch pit as seen after thresholding optical microscope image data. It is clear that estimating the etch pit density in clusters based on the assumption that the whole cluster area is composed of etch pits of size A can only provide a lower limit of the true EPD in clusters.

While the SEM is a good tool to determine absolute EPD values of etch pit clusters, comparisons between sister wafers with the SEM are hardly possible, because size, shape and EPD within clusters is subject to a high degree of variation even from one wafer to the next. Analysis with the optical microscope allows for large enough areas to be recorded, such that these small length scale variations are not significant to the overall picture, while still preserving single etch pit precision counting in low and mid EPD regions.

Due to the large size of the input images (more than 6×10^8 pixels) the computation of structured etch pit data from the raw image takes about a minute of time on current processors, whereas filtering and plotting the structured etch pit data set can be accomplished within a few seconds. In day to day work, re-computations of EPD maps are done many times, so separating the time consuming step is intuitive from a practical point of view.

After reading in the results of the steps described so far, etch pit size filtering is applied, i.e. structures with a size of 1 pixel are discarded as noise. Unwanted wafer regions, such as missing wafer parts due to breakage or the part of the wafer that has been in contact with the carrier during defect etching, are cropped.
At this stage, etch pit conglomerates, defined as etch pits that have a size $a > 2A$, with A the size of a typical etch pit, are weighted with a factor $\frac{a}{A}$, effectively counting them as multiple etch pits according to their size (multiplicity counting).

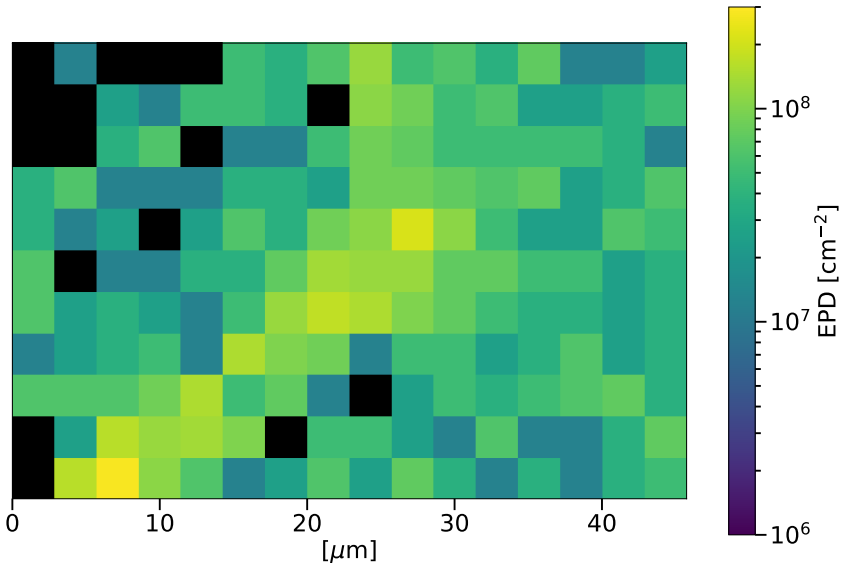


Figure 3.11.: EPD map based on the image depicted in figure 3.10. Center regions show a maximum EPD of more than one order of magnitude above the value that is accessible with optical microscope image data. The depicted region corresponds to a size of about 36 % of a single pixel in an EPD map as used in this thesis. Since the input image features etch pits of highly varying size, the feature of the algorithm for multiple counting of etch pit conglomerates, which is based on etch pit size, had to be disabled to achieve meaningful results: Here, isolated structures are counted as a single etch pit, regardless of their size. A further noteworthy consequence of the highly varying etch pit size in figure 3.10 is that the bin size, which was chosen to reflect the peak EPD in the cluster center, is smaller than single etch pits in other regions of the image.

Again, keeping A constant is required for a meaningful comparison between sister wafers.

3.3.5. EPD results

Etch pit data is visualised in the form of a two dimensional histogram, with the vertical and horizontal axes corresponding to the physical dimensions of the wafer and the bin height corresponding to the etch pit density (figure 3.9). It is noteworthy that the process of binning the data determines a lower limit of the EPD: The minimal EPD value, associated with one etch pit per bin, depends on the bin size. A physically meaningful bin size could be chosen using the minority charge carrier diffusion length as characteristic length scale for the bin width. However,

in typical mc-Si material there are regions of very high and low diffusion length in close proximity, so a compromise is necessary. Bins that are too large will hide etch pit structures. If bins are very small (about the size of an etch pit), density calculation becomes meaningless. EPD plots in this work use square bins with a width of 62.5 µm, corresponding to an area more than two orders of magnitude larger than the area of a single etch pit. This bin size is chosen such that typical structures in mid and high EPD regions are resolved with good detail. Larger bin sizes allow for easier interpretation of results in low EPD regions but at the cost of hiding structure in mid and high density regions (figure 3.12). For plots that are easier to read, empty bins are drawn in black.

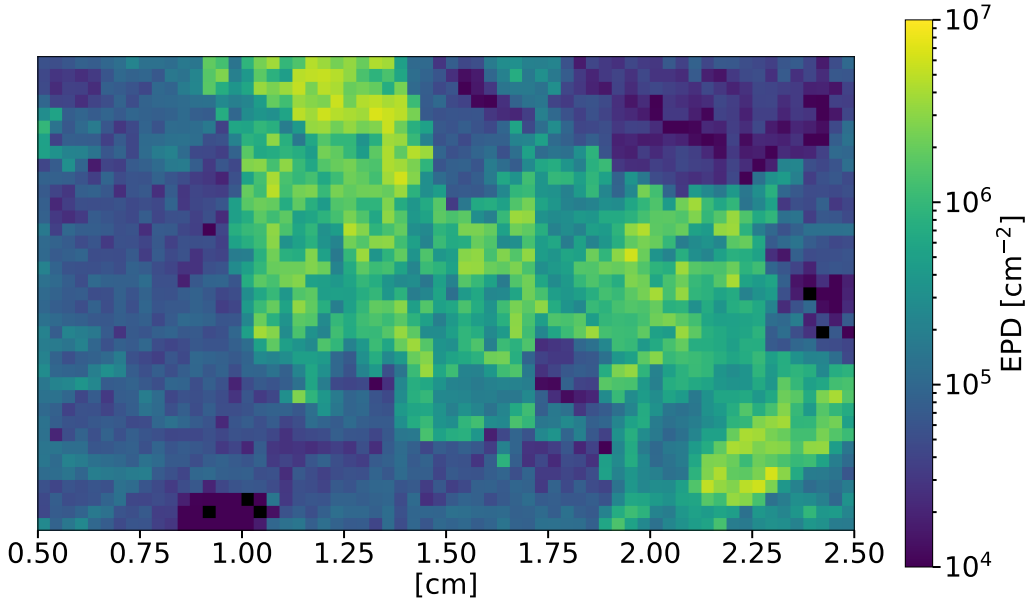


Figure 3.12.: An EPD map of the wafer shown in figure 3.9 (with grain boundaries removed), here shown with a bin width of 300 µm, about five times the bin width that is used in the other EPD maps shown in this work. While low EPD regions within grains appear more homogeneously, EPD structures in mid and high EPD regions can not be resolved with this bin size.

While these spatial maps are good for comparisons with other spatial measurements, such as τ_{eff}, [Fe_i] and EBIC measurements, changes in EPD can be better quantified if the data is reduced even further: The 2-d maps can be reduced to 1-d histograms, for which the fraction of the wafer surface affected by a certain EPD is shown (figure 3.13). Such a distribution of the area fraction as function of EPD allows for a good understanding of a wafer's EPD, while at the same time the comparison between two distributions of this type gives a good impression on possible changes in EPD. The ratio between two area fraction histograms makes quantification of EPD changes due to a certain process easier (figure 3.13).

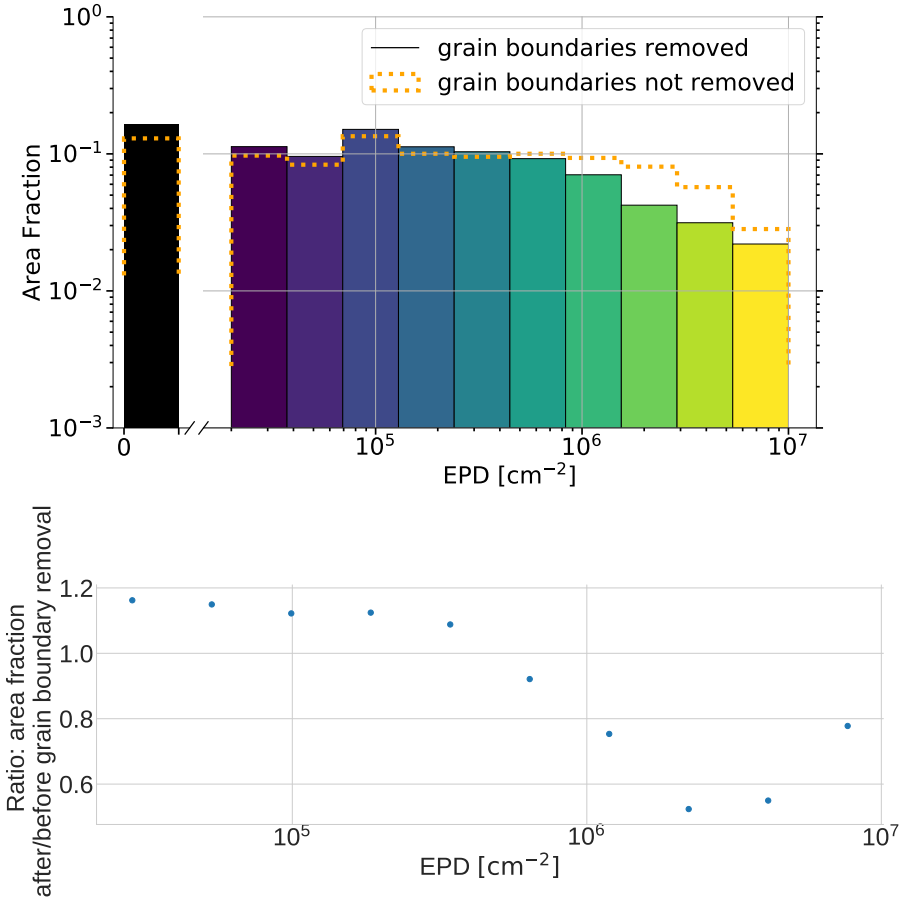


Figure 3.13.: Top: An example of 1-d EPD histograms, calculated from the EPD data of figure 3.9, showing the area fraction of the wafer surface that is covered by a certain EPD. The histogram in solid colors shows the EPD after detection and removal of grain boundaries, while for the dotted histogram no distinction between grain boundaries and etch pit clusters has been made. Therefore, the dotted histogram does not represent the true EPD of the wafer. Bottom: The ratio of the above histograms.

Spatial EPD maps presented in this thesis are sometimes cropped to a smaller area. This is done to remove regions where either parts of the wafer have been lost due to breakage or to remove regions containing a high density of polishing scratches. Identical cropping is applied to all wafers of a set of sister wafers. Removing these regions ensures that 1-d histogram plots similar to figure 3.13 contain only corresponding regions for a complete set of sister wafers.

Interpretation of EPD maps

In summary, when interpreting EPD maps, the following points should be kept in mind:

- There is an upper limit to the EPD that can be detected with the optical microscope. This limit corresponds to an EPD of about $1 \times 10^7\,\mathrm{cm}^{-2}$. Cluster regions can exhibit much larger EPD values on highly localized sub regions, where EPD values of up to $2 \times 10^8\,\mathrm{cm}^{-2}$ could be measured.
- The lowest possible, non-zero EPD value, using a bin size b, is $\frac{1}{b}$. Here, square bins with a side length of 62.5 µm are used, corresponding to a minimum EPD of $2.56 \times 10^4\,\mathrm{cm}^{-2}$.
- The number of etch pits in an etch pit conglomerate and the number of etch pits in a cluster are explicitly depending on the median etch pit size A. The value of A has been determined from a set of identically etched wafers. A fixed value of $A = 18$ pixels, with a pixel size of 698 nm, is used here, such that a meaningful comparison between sister wafers is possible.

3.3.6. Uncertainty of EPD measurements

A set of three identically processed as-grown sister wafers has been subjected to defect etching and EPD analysis, such that the uncertainty level of EPD measurements can be estimated. The relative uncertainty in the total number of isolated etch pits in these three samples is 3.2 %. The total number of etch pits that belong to clustered structures, a number directly proportional to the surface area that is covered by etch pit clusters, exhibits a relative change of 18 %. Repeating this calculation with etch pit data that has not been subjected to the algorithmic removal of grain boundary structures, results in a relative change of only 13 %, indicating that this step introduces some systematic uncertainty.

For quantification of changes in EPD on a given wafer, various sections of this thesis contain EPD data in the form of 1-d histograms. By comparing such histograms for the above described sample set (figure 3.14 without grain boundary removal, figure 3.15 including the grain boundary removal step) a feeling for the natural variance of EPD changes due to variations in the crystal and defect structure can be obtained. However, the wafer-specific defect structure that a certain set of sister samples exhibits, strongly influences the shape of this histogram, yet the significance of relative changes between such histograms depends on the histogram shape: Large changes in bins of large height (large fraction of the surface area) indicate significant changes in the defect structure whereas similarly large relative changes in bins of small height can be insignificant.

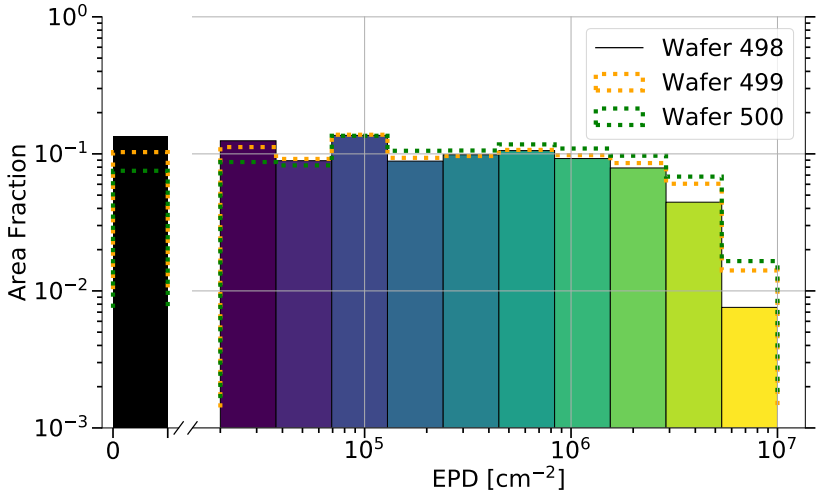


Figure 3.14.: Comparison of the EPD frequency of three identically processed sister samples in the as-grown state. This data (unlike figure 3.15) still contains grain boundary information. The EPD seems to increase with the direction of crystal growth and observed differences between immediate sister wafers are overall smaller.

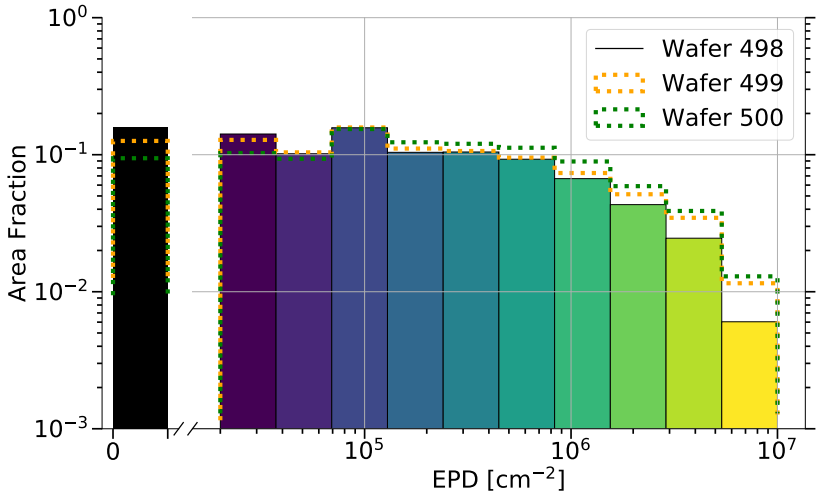


Figure 3.15.: Comparison of EPD measurements of the very same samples depicted in figure 3.14, here after removal of grain boundaries. EPD differences between these samples help to judge changes in EPD that are solely due to the crystallographic differences in sister samples. A slight increase in the observed difference between the depicted samples suggests that the process of grain boundary removal is a small contribution to the systematic uncertainty.

This experiment shows, that even identically processed sister wafers can exhibit considerable changes in EPD: For example the surface area of the sample that is covered with an EPD of 0 decreases from 16 % to 13 % to 9 % with increasing waver number (figure 3.15). This indicates a systematic change in EPD along the direction of crystal growth.

3.4. Electron beam induced current

3.4.1. EBIC measurement principle

With electron beam induced current (EBIC) measurements [57], spatially resolved surface-close recombination activity can be measured. The electron beam of a scanning electron microscope (SEM) is used to locally excite charge carriers in the material. With short circuit conditions (figure 3.16) and a means of charge carrier separation present (i.e. a pn-junction, a metal-oxide-semiconductor (MOS) structure or Schottky diode), a net current is diffusing through the wafer material. This current is reduced in the vicinity of charge carrier recombination active defect sites. By scanning the wafer surface, spatially resolved current measurements are obtained. These can be used to map regions of high recombination activity across the wafer surface. Secondary charge carriers are created close to the surface where primary electrons from the SEM beam interact with the material. Because further charge carrier movement is governed by diffusion, charge carrier concentrations are highest in surface-close regions. Recombination is proportional to the carrier concentration (equation (2.1)), therefore variations in the EBIC signal are caused dominantly by surface-close defects (figure 3.16).

3.4.2. EBIC sample preparation

Using lifetime samples as starting point, samples for EBIC measurements are prepared by removal of existing passivation layers in HF and subsequent creation of a fresh surface, using a 1 min chemical polish (CP) step, corresponding to a removal of about 1 µm per wafer side. Subsequently a 10 min reaction in piranha solution is executed. Here, the piranha solution is used for growth of a silicon oxide layer only: In contrast to piranha clean steps, after which the resulting oxide layer is removed in HF, here the oxide layer is kept for its insulating properties. Square aluminium pads with 9 mm side length and 15 nm thickness are created on the wafer top via masked thermal evaporation. Technically the structure created here constitutes a metal-oxide-semiconductor (MOS) structure. However, the oxide layer thickness after piranha treatment is only about 0.55 nm [58], so in practice this structure performs like a Schottky-diode, i.e. there is a naturally occurring space charge region facilitating charge carrier separation. The so-called MOS/EBIC technique explicitly uses very thick oxide layers (up to 45 nm in [59], i.e. more than

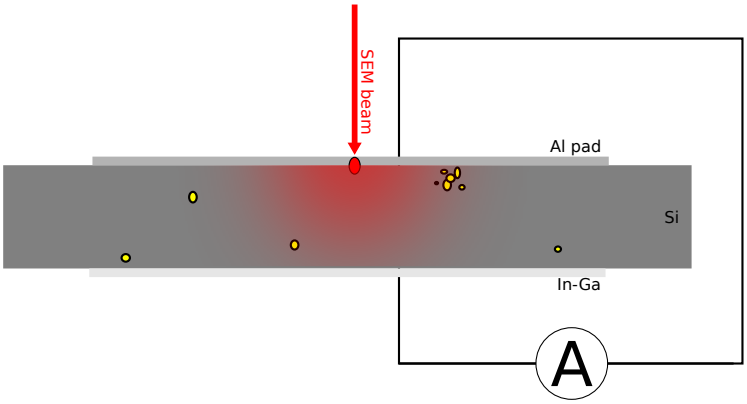


Figure 3.16.: Schematic drawing of EBIC measurement principle in a cross-sectional side-view: Primary electrons from the SEM beam are exciting secondary charge carriers close to the wafer surface (red ellipse). Charge carriers are separated in the space charge region of the aluminium-silicon transition (Schottky contact) and start to diffuse isotropically inside the wafer (red gradient). Charge carriers either recombine, e.g. at recombination active centers (yellow) or they reach the rear contact and thereby contribute to the measured current. Since recombination is proportional to the charge carrier density, modifications of the measured current are dominated by surface-close defects.

80 times the oxide layer thickness used here), in which case the space charge region must be created via a bias voltage. In MOS/EBIC applications, the thickness of the space charge region can be controlled by varying the bias voltage, allowing for thinner space charge regions when compared to a Schottky Barrier. Because defects withing the space charge region typically exhibit very low recombination activity [59], the MOS/EBIC technique allows for analysis of defects closer to the surface in comparison to conventional Schottky EBIC.
With the sub nanometer oxide layer that is used here, a mixture of both cases is achieved: The thin oxide layer weakens diffusion, resulting in a space charge region of reduced thickness while still retaining the characteristic of a Schottky barrier.
An electrical rear-side contact between the sample and the sample holder is achieved by mechanical application of a liquid indium-gallium alloy on the wafer (figure 3.16). Distributing this alloy with a metal scalpel ensures that the oxide layer on the rear side is destroyed. The aluminium pad on the front side is contacted by pressing a wire onto the aluminum pad.

A typical EBIC measurement of a low τ_{eff}, high $[Fe_i]$ region of the as-grown material (figure 3.17) shows line like structures of enhanced recombination activity. Some wafers show cloud-like regions of weakly enhanced recombination activity in some wafer areas. Density of EBIC structures varies greatly over the wafer surface, so it is advisable to use τ_{eff} and $[Fe_i]$ measurements for pre-selecting interesting regions for EBIC measurements before sample preparation.

Figure 3.17.: EBIC data of a typical as-grown mc-Si sample. The material shows line-like structures as well as weaker cloud-like regions of enhanced recombination activity. Not all of the line-like structures are originating from grain boundaries [60]. The thick black structure in the lower right corner is the tip of the EBIC current probe that is contacting the aluminum pad.

4. Influence of solar cell processing steps on the material quality

Here, the measurement methods that have been introduced in the previous chapter are applied to sets of wafers to observe the effects of gettering on τ_{eff}, $[\mathrm{Fe_i}]$, the surface-close recombination activity as measured by EBIC and especially the etch pit density. A main focus is on high-temperature gettering steps of various kind: boron- as well as phosphorous-based gettering is studied, based on conventional BBr_3 and $POCl_3$ processes as well as on doping glasses created with atmospheric pressure chemical vapour deposition (APCVD). Of high interest is also the influence that the thermal load of these processes alone, i.e. thermal processing in absence of external gettering sinks, exerts on the material quality. Finally, the effect of gettering, hydrogen passivation and the combination of these two steps on the EBIC signal is presented.

4.1. Gettering techniques

4.1.1. Diffusion furnace gettering: $POCl_3$ and BBr_3

The $POCl_3$ diffusion is considered the standard process for n-type emitter formation and P-gettering in silicon solar cells [3] [61]. Liquid $POCl_3$ is dispersed into a high temperature chamber at low pressures where in the presence of O_2, phosphorous-silicate glass (PSG) is created on the silicon surface, acting as a phosphorous diffusion source for emitter formation as well as a gettering sink for impurities [3]. In a $POCl_3$ process, gettering as well as in-diffusion of phosphorous is already taking place while the PSG layer is growing. Both wafer sides are exposed to the $POCl_3$ containing atmosphere, so automatically both wafer sides are covered with PSG.

A comparable process, based on the substance BBr_3 instead of $POCl_3$, can be used to facilitate boron diffusion gettering and the formation of a highly doped p^+ layer.

4.1.2. APCVD-based gettering

Unlike the previously described $POCl_3$ and BBr_3 processes, the APCVD technique [62] [63] [64] [65] [66] allows (1) a deposition of doping glasses that is independent from a high temperature diffusion step and (2) deposition on only one wafer side at a time. Unlike other low pressure or vacuum CVD methods, no vacuum pumping steps are required, so this process can be integrated into production lines. Depending on the machine's construction type, wafers are transported through the machine on a moving belt or on stationary rotating rollers. In case of PSG (BSG) deposition, phosphine (diborane), gaseous silane and oxygen react at temperatures in the range of 440 °C to 550 °C, thereby depositing a PSG (BSG) layer on one wafer surface. Typically higher temperatures are required for the phosphine reaction. Here, 440 °C is used for BSG layer deposition and 550 °C for PSG layers.
Doping glass layers of two different machines (belt- as well as roller-transport) have been studied here. While due to the differences in the machine layouts the composition of doping glass layers can not be expected to be identical, differences between the layers from both machines are irrelevant for the issues discussed in this thesis. With both types of machines, 40 nm thick PSG layers with high expected phosphorous concentrations ($> 18\,\%$) have been created. For BSG, layers of the same thickness with an estimated 5 % boron concentration have been used.

For APCVD gettering, doping glass deposition is a step that is realized entirely independent from the high temperature diffusion step, during which gettering and emitter formation take place [63] [65]. It can be argued that separating the steps of doping glass formation and dopant/impurity diffusion allows for a greater control of parameter space. The relevant parameters are the combination of process temperature and processing time and their chronology [67]. The process temperature determines the mobility of dopant and impurity atoms and provides the activation energy for dissolution of precipitates while longer process times generally lead to a higher intensity of the gettering effects [67] [68]. Unlike here, where the sole focus is on the gettering performance, diffusion parameters for solar cell processes have to strike a balance between good gettering performance and the properties of the emitter region that is created. For gettering, the chronology of the temperature profile has to be considered as well, e.g. short periods at very high temperatures can be used to dissolve precipitates in the beginning of a process [67] [68], while a subsequent extended period at lower temperatures provides gettering conditions for the dissolved impurities [67] [69].

4.2. Phosphorous gettering

This section contains a comparison of gettering results for $POCl_3$ and APCVD P-gettering in form of τ_{eff} and $[Fe_i]$ measurements as well as the influence of P-gettering on the EPD.

4.2.1. Effects of phosphorous gettering on τ_{eff} and $[Fe_i]$

Material quality results in the form of τ_{eff} and $[Fe_i]$ measurements are presented as a set of three sister wafers that, in addition to the gettered sample, include an as-grown reference and a temperature reference sample. The temperature reference sample is subjected to the same temperature load as the gettered sample, however without the presence of a gettering sink. While the processing temperature is the same for APCVD and $POCl_3$ based gettering, the processing time at peak temperature of the $POCl_3$ process (50 min) is considerably lower than the processing time at peak temperature of APCVD gettering (75 min). The actual temperatures as a function of time for the gettering processes used for this work are depicted in figure 4.1. Despite this difference, temperature reference samples of the APCVD gettering processes are used for $POCl_3$ gettering as well. This compromise was chosen for several reasons. Mainly APCVD-based processes have been studied for this thesis and therefore this temperature process is most relevant for comparison. Furthermore, microscopic defect structure can change significantly from wafer to wafer, so reducing the number of sister wafers is beneficial for overall comparability of results. One of the functions of the $POCl_3$ process is to act as industry standard reference process, therefore it was avoided to change processing times to match the APCVD process. Lastly, changes in processing time are expected to result in quantitative difference only, however changes that are different in kind are expected only with different processing temperatures that can facilitate processes with different activation energies.
Temperature reference samples reveal changes that take place during the high temperature step: Impurities can be re-distributed within the material and accumulate at localized sites, thereby improving material quality in grain centers at the cost of reduced material quality at these localized sites (grain boundaries, dislocations, precipitate sites) [67]. This so-called internal gettering can lead to an overall improvement of material quality without the presence of an external gettering sink [67].
Impurities can also accumulate at the wafer surface, despite the absence of a gettering sink [67]. Since after the high temperature step a few micrometer of surface material is removed, impurities located at the surface are removed together with the material. It can be argued that the removal of surface material characterizes this process as an external gettering mechanism.
The temperature reference sample allows for a distinction between external gettering effects in the presence of a gettering sink and internal gettering and gettering at the surface.

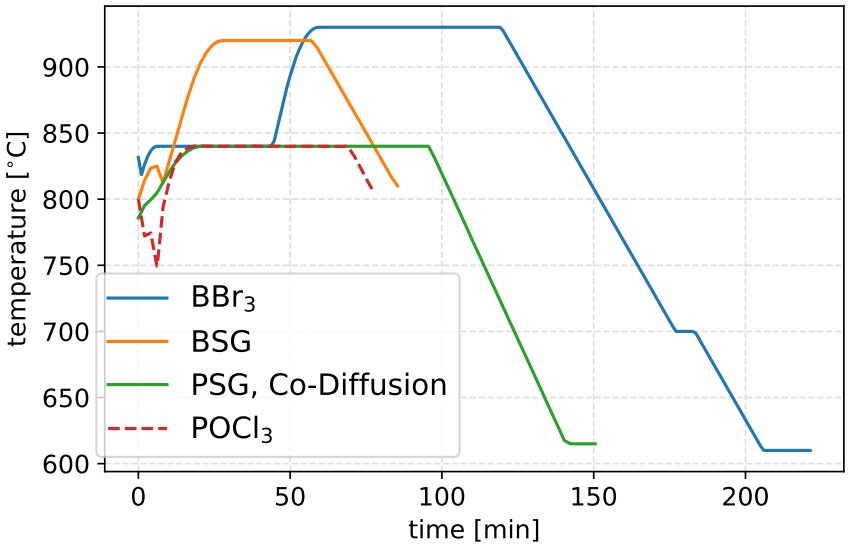
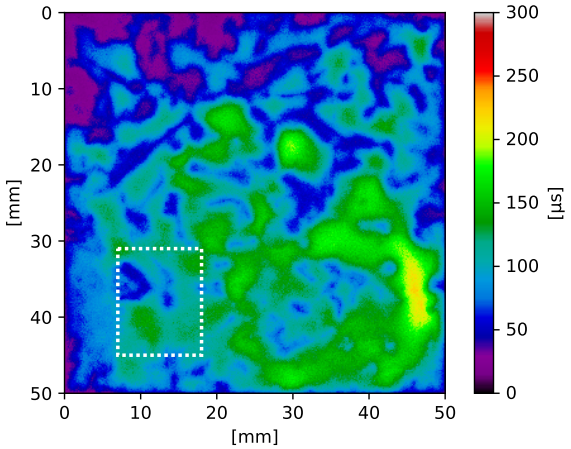


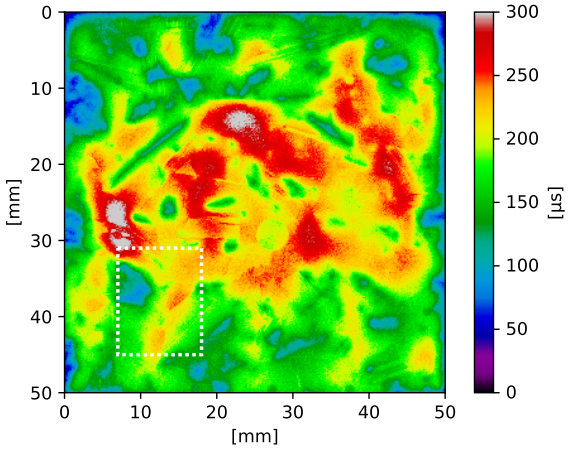
Figure 4.1.: Diffusion temperature profiles (measured values) of all the high temperature diffusions processes that are used in the context of this work.

Furthermore, other temperature induced effects, such as increases in impurity concentration due to precipitate dissolution or any changes in dislocation structure that may arise can be distinguished from gettering processes by comparison with a temperature reference sample.

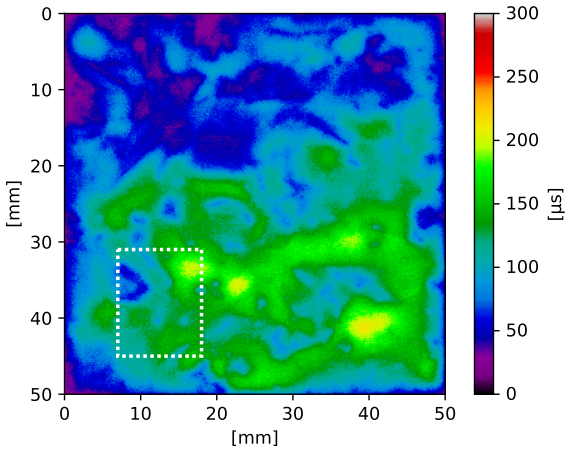
Lifetime maps after $POCl_3$ gettering (figure 4.2) show significant increases in τ_{eff} and a more homogeneous spatial distribution compared to the as-grown and temperature reference. This $POCl_3$ gettering step increases the harmonic mean lifetime from 77 µs in the as-grown state to 170 µs. The harmonic mean is used here since averaging τ_{eff} values corresponds to an average of (recombination) rates: In the same way that the total resistance of n parallel resistors of arbitrary resistivity R_n in an electrical circuit is equivalent to n parallel resistors, each with a resistivity of the harmonic mean of R_n, here the harmonic is used to calculate the mean recombination rate in each pixel of a recombination active surface.
The depicted wafer exhibits a noticeable difference between the top and lower wafer half in the as-grown state. The $POCl_3$ gettered wafer exhibits a homogeneous τ_{eff} distribution, removing the difference between both wafer halves. The temperature load of the gettering process affects both wafer halves differently: The side of the wafer that already exhibits lower lifetimes is further influenced negatively by the temperature process whereas the lower wafer half benefits from thermal treatment. The region that exhibits improvement due to temperature load is located further away from the block edge and therefore contains less contaminations from the crucible walls. Sets of wafers with similar distances to the crucible wall all exhibit impaired lifetimes for low and middle block heights. Comparable findings on the very same material have been published in [64].



(a) As-grown



(b) $POCl_3$ gettered



(c) Temperature reference

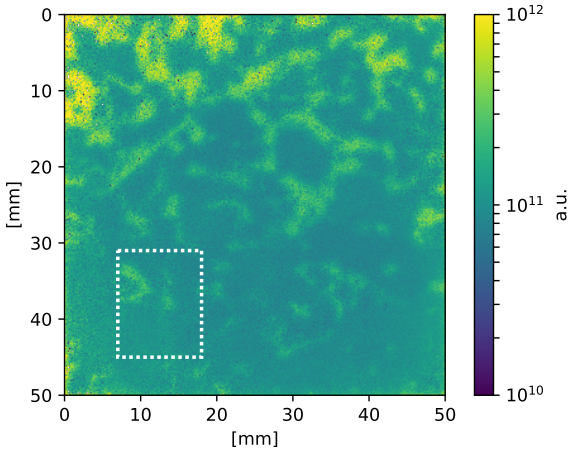
Figure 4.2.: PL measurements of τ_{eff} on sister wafers in the as-grown state (a), after an industry standard $POCl_3$ gettering process (b) and corresponding temperature reference (c). These measurements show the material in a state of dissociated FeB pairs. Gettering increases the harmonic mean lifetime from 77 µs in the as-grown state to 170 µs. For the marked region, a comparison of the etch pit density after a APCVD and $POCl_3$ gettering process will be discussed (figure 4.9).

However, when looking at temperature reference samples from upper block heights far from the crucible walls, consistent improvements in τ_{eff} relative to as-grown sisters are observed. This indicates that impurity compositions are changing with block height and with varying distance from the crucible wall.
Measurements of [Fe_i] after this $POCl_3$ process (figure 4.3) show higher interstitial iron concentrations at the northern wafer side that is closer to the block edge. The [Fe_i] results of the temperature reference show that interstitial iron is distributed over larger areas than what is observed in the as-grown state. Gettering is able to reduce the interstitial iron concentration in most regions, but seems to have little to no effect in a few localized regions.

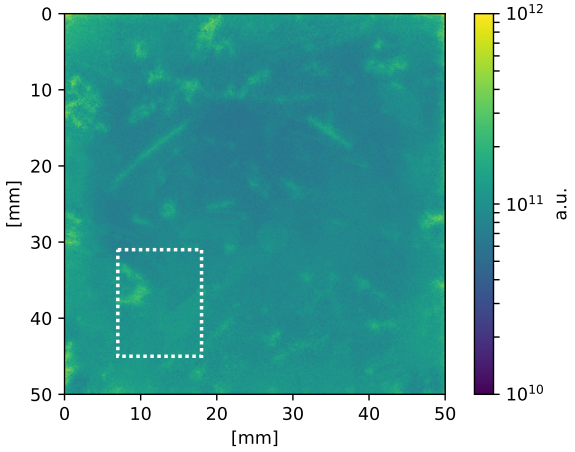
A direct comparison of τ_{eff} and [Fe_i] measurements between $POCl_3$ and APCVD gettering processes has been carried out using sister samples that were subjected to APCVD-based co-gettering (figure 4.4). For this co-gettering process, a wafer is covered with a PSG layer on one side and a BSG layer on the other side. Subsequently, the wafer is subjected to the high temperature diffusion process (figure 4.1). Lifetime results of the depicted sample are very similar to $POCl_3$ gettering, whereas [Fe_i] measurements indicate a stronger gettering effect in case of APCVD-based gettering. When comparing multiple sets of wafers from the same two processes, no consistent advantage of either APCVD-based gettering or the $POCl_3$ process is found in τ_{eff} and [Fe_i] results [64] [60].

Results that are comparable to $POCl_3$ gettering are achievable with APCVD P-gettering: The high temperature step that is used for APCVD gettering is of a peak temperature of 840 °C that is held for a duration of about 90 min (figure 4.1). A set of lifetime samples after APCVD P-gettering shows a significant gettering effect in measurements of τ_{eff} (figure 4.5) as well as in [Fe_i] measurements (figure 4.6). Already the as-grown lifetime of the depicted sample is relatively high, since the material depicted here is taken from a region of the block with relatively low impurity concentration (at about 70 % block height and close to the block center). The as-grown sample's harmonic mean lifetime of 148 µs is increased to 237 µs by the gettering process. The temperature reference sample exhibits considerable lifetime improvement for temperatures of 840 °C, indicating that internal gettering effects outweigh precipitate dissolution. This behavior is seen repeatedly for material from this block height, when processed in this temperature regime.

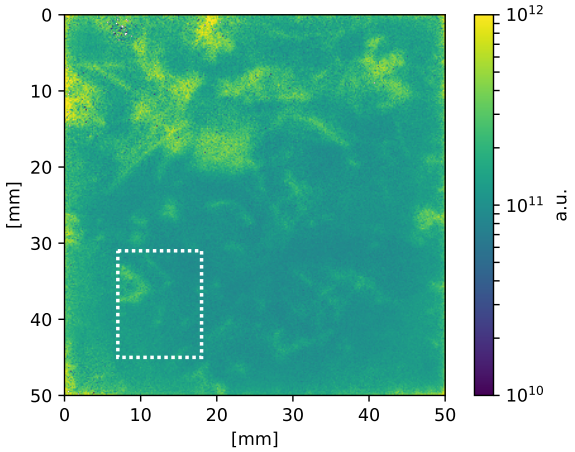
In summary, the described P-gettering processes have been shown to significantly improve τ_{eff} and a significant gettering of interstitial iron is observed. Gettering efficacy as indicated by measurements of τ_{eff} and [Fe_i] of APCVD-based P- and co-gettering are comparable with an industry standard $POCl_3$ diffusion gettering process.



(a) As-grown



(b) $POCl_3$ gettered



(c) Temperature reference

Figure 4.3.: Measurements of $[Fe_i]$ on the very same sample set as depicted in figure 4.2. Interstitial iron is distributed over larger areas for the temperature reference (c) in comparison to the as-grown state (a) while gettering results in a slight decrease of $[Fe_i]$, especially in the upper wafer half. For the marked region, a comparison of the etch pit density after a APCVD and $POCl_3$ gettering process will be discussed (figure 4.9). As detailed in section 3.2.5, only arbitrary units are given. Relative values between two samples, however, are reliable.

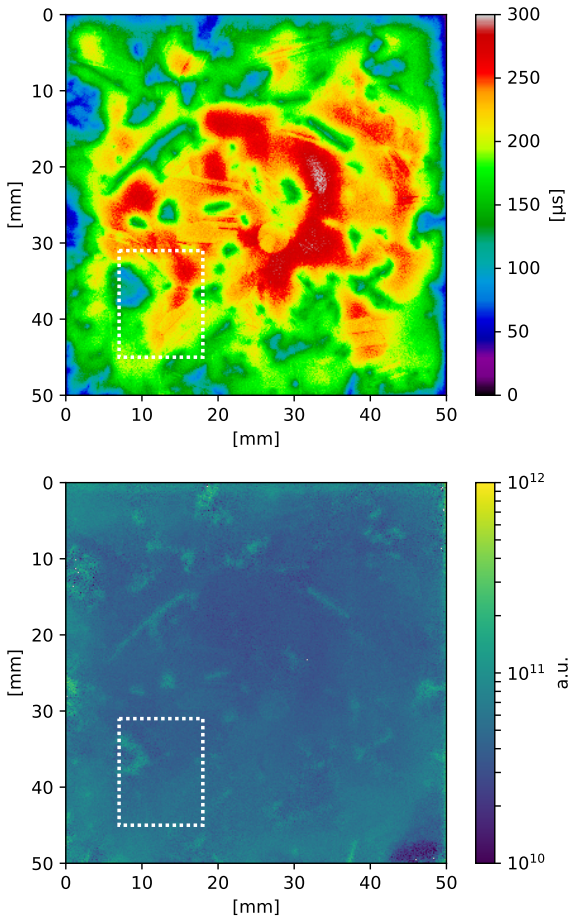
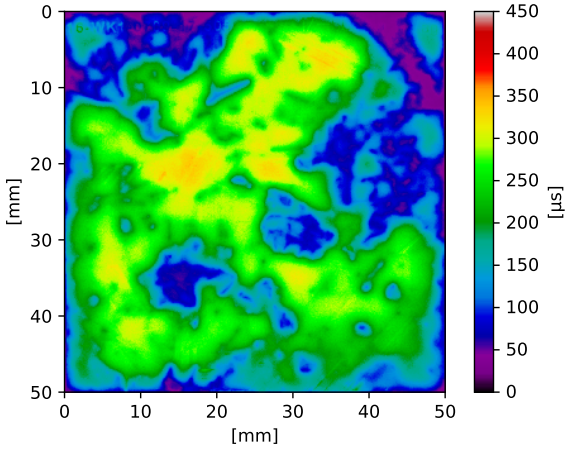
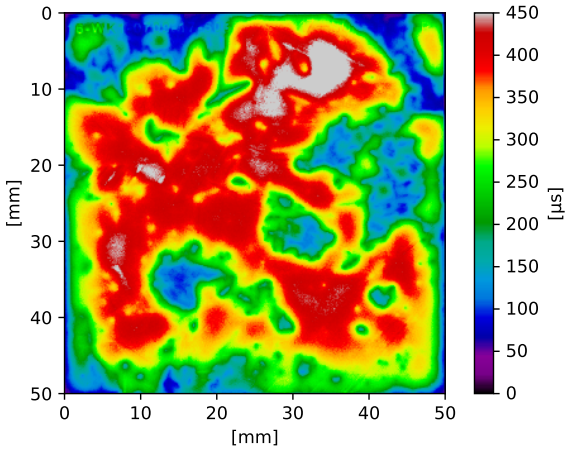


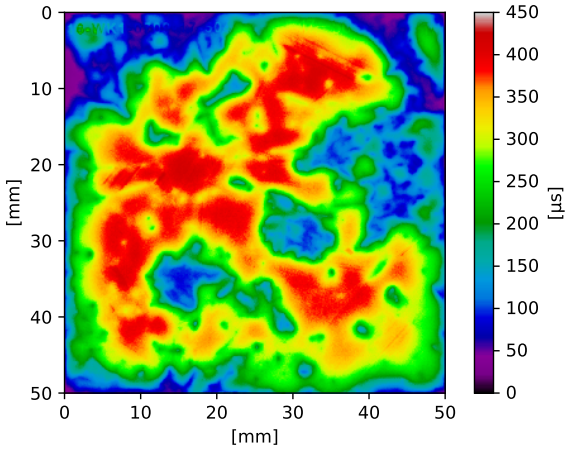
Figure 4.4.: APCVD (belt-transport) co-gettered sister samples to the $POCl_3$ lifetime set depicted in figure 4.2 and 4.3. Based on the τ_{eff} result, the gettering strength of the used APCVD and $POCl_3$ processes are similar. Results of $[Fe_i]$ show stronger gettering for the APCVD sample. The APCVD gettered sample depicted here is a so-called co-getterd sample, i.e. one side is covered with PSG, the opposite side with a BSG gettering sink. Other experiments have shown that at the used temperatures practically all gettering effect is due to P-gettering [64].



(a) As-grown

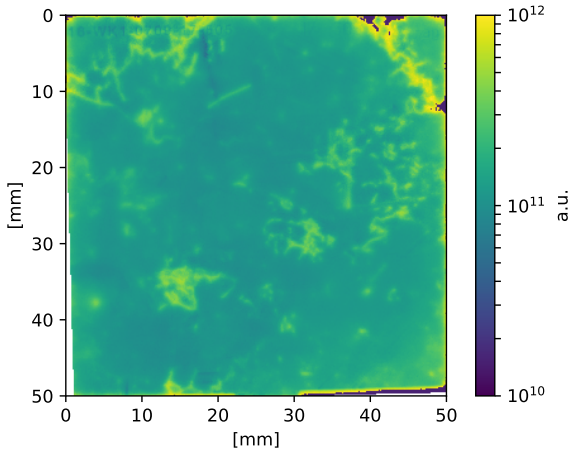


(b) APCVD P-gettered

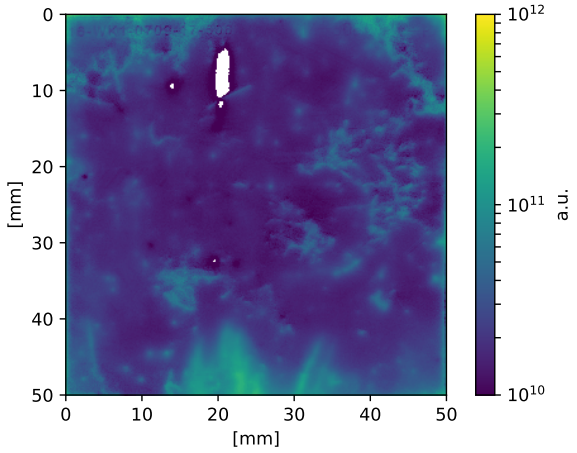


(c) Temperature reference

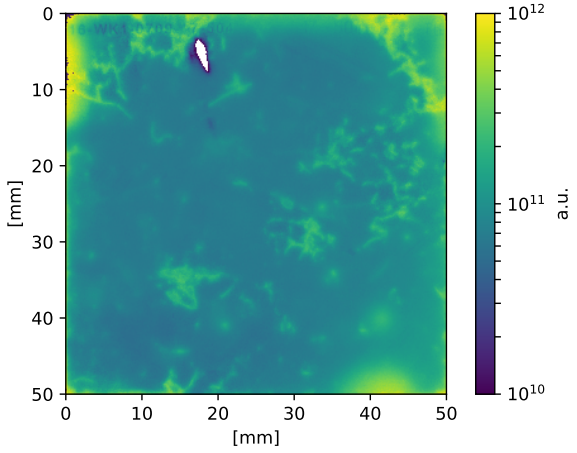
Figure 4.5.: PL measurements of τ_{eff} on sister wafers in the as-grown state (a), after APCVD P-gettering (b) and corresponding temperature reference (c). These measurements show the material state for dissociated FeB pairs. The APCVD P-gettered sample (roller-transport APCVD) exhibits a significant gettering effect (harmonic mean lifetime $\bar{\tau}_{\text{eff}} = 237\,\mu\text{s}$) when compared to the as-grown ($\bar{\tau}_{\text{eff}} = 148\,\mu\text{s}$) and temperature reference sample ($\bar{\tau}_{\text{eff}} = 190\,\mu\text{s}$). This is especially noteworthy when considering that the material used here is taken from regions of the silicon block for which the least impurity concentration is expected.



(a) As-grown



(b) APCVD P-gettered



(c) Temperature reference

Figure 4.6.: Measurements of $[Fe_i]$ on sister wafers show a strong reduction of the interstitial iron after APCVD P-gettering (b) when compared to the as-grown (a) and temperature reference (c). For regions drawn in white, the $[Fe_i]$ calculation fails. The depicted material is the same as shown in figure 4.5.

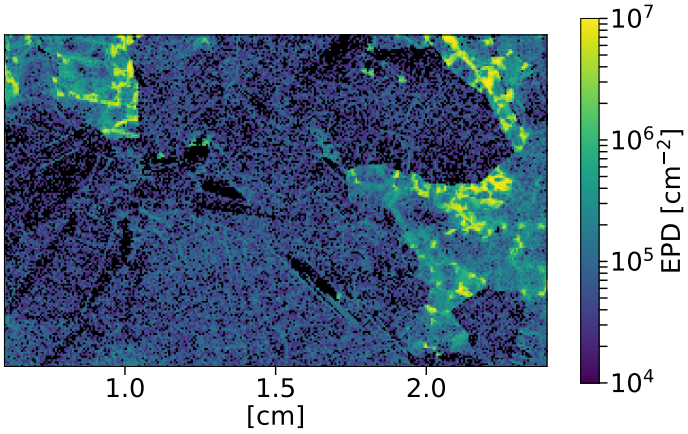
4.2.2. EPD after $POCl_3$ and APCVD P gettering

EPD measurements on sets of lifetime samples show that P-gettering leads to a significant reduction of etch pits. Comparable observations have been published before [19] [20], but the effect itself remained unexplained. In this section, results are presented that demonstrate EPD reduction after P-gettering using the developed large scale high precision analysis. Experiments that restrict possible explanations for EPD reduction are detailed in chapter 5.

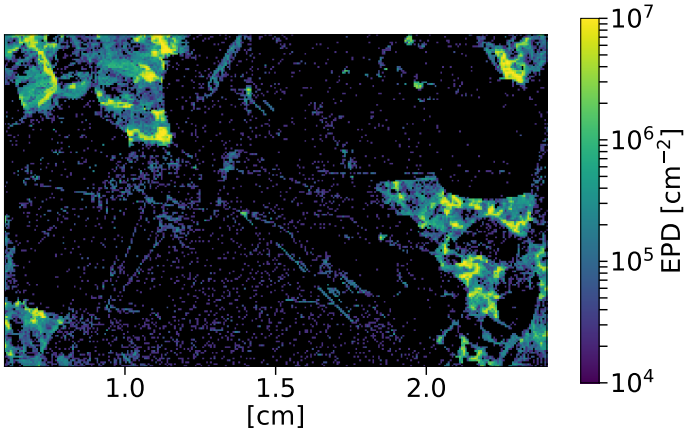
Again, sets of three sister wafers with a gettered sample, an as-grown reference and a temperature reference sample are shown in combination. A significant reduction of the EPD is observed on samples that were gettered with the previously discussed $POCl_3$ process (figure 4.7, 4.8). A reduction of the etch pit density is observed in regions where as-grown references exhibit mid and low EPD. Temperature reference samples show that the thermal load of the gettering process has no influence on the EPD.
Optical microscope analyses of high EPD regions on gettered and ungettered sister samples show no EPD reduction. Using the SEM for such a comparison, thereby testing whether this apparent absence of EPD reduction in clustered regions is a consequence of the optical microscope's detection limit for high EPD values (section 3.3.4), is not trivial: Since changes in crystal structure are very pronounced on microscopic scales (even between direct sister wafers) it has not been possible to identify corresponding structures of etch pit clusters on gettered and ungettered sister samples with the SEM. As will be seen, other circumstances (section 5.7) allow SEM comparisons between corresponding clustered regions in a gettered and un-gettered state on the very same wafer, thereby reducing the crystallographic difference to a workable degree. These results are presented in section 5.7.2.

A similar reduction of the EPD is observed for APCVD-based P-gettering. APCVD P gettering is used for most of the studies with which the nature of the EPD reduction effect is investigated (chapter 5) and EPD reduction results of this method are included in that context.

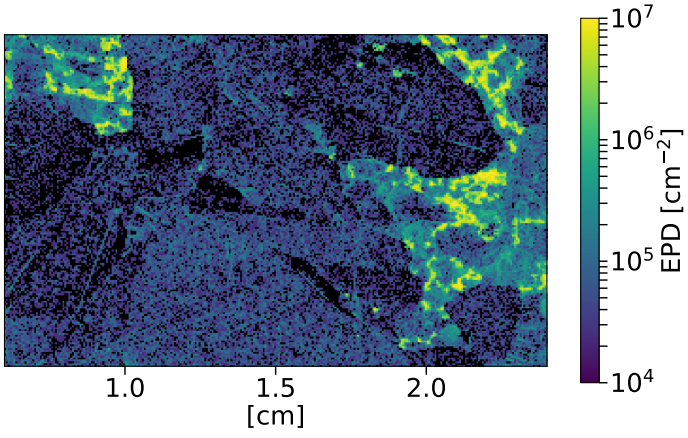
A comparison between the strength of EPD reduction after APCVD and $POCl_3$ gettering (figure 4.9) has been prepared with the same APCVD co-gettered samples whose τ_{eff} and $[Fe_i]$ measurements have been shown above (figures 4.2 and 4.4). The EPD measurements on APCVD co-gettered wafers have been obtained from the wafer side that was covered with a PSG during the high temperature step. Slightly stronger EPD reduction is observed for the APCVD gettered sample (figure 4.9). While overall, a similar gettering efficacy is measured for both processes, the local region on which the EPD is compared, shows higher lifetimes for the APCVD gettered sample (marked region in figures 4.2 and 4.4). Whether stronger gettering leads to stronger EPD reduction is studied further in an experiment of EPD reduction with explicit variation of the gettering strength, presented in section 5.6. The depicted EPD measurement (figure 4.9) shows an increase in the frequency of the lowest EPD regions after gettering.



(a) As-grown



(b) $POCl_3$ gettered



(c) Temperature reference

Figure 4.7.: EPD maps of as-grown, temperature reference and gettered sister samples, demonstrating EPD reduction after $POCl_3$ gettering. EPD changes between the as-grown and the temperature reference sample do not exceed the expected variance for sister samples (section 3.3.6). The corresponding EPD frequency is depicted in figure 4.8.

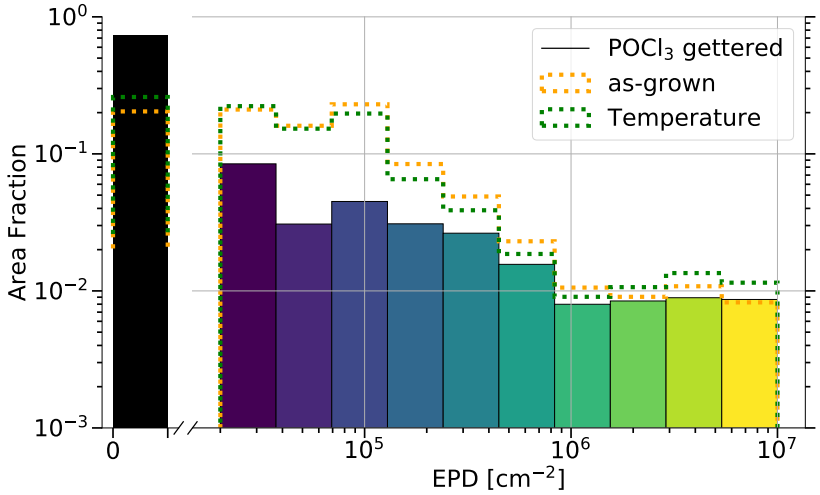


Figure 4.8.: One dimensional histograms of the EPD map set depicted in figure 4.7. The $POCl_3$ gettering step reduces the frequency of mid and low EPD regions, whereas the surface area that is totally free of etch pits has nearly doubled.

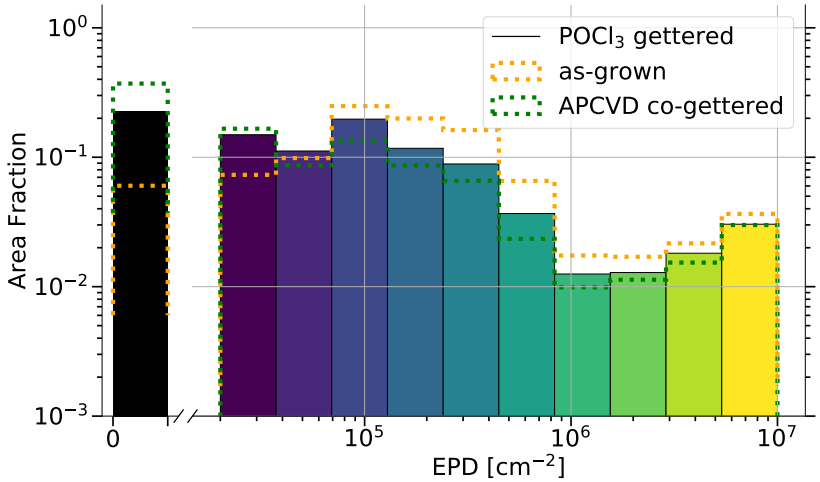
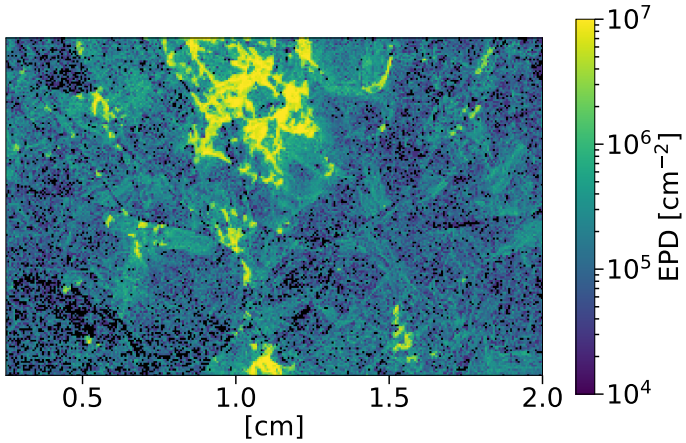
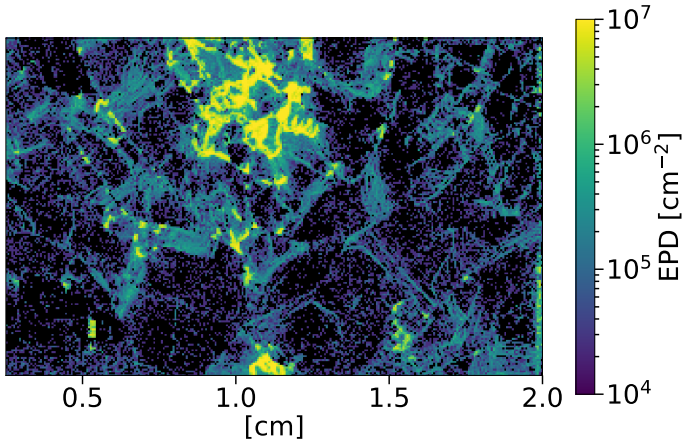


Figure 4.9.: Slightly stronger EPD reduction is observed for APCVD-based gettering when comparing with a sister sample after $POCl_3$ gettering. The origin of these EPD samples in τ_{eff} and $[Fe_i]$ measurements is marked with white rectangles in figures 4.2 and 4.4. From these measurements, it is apparent that the wafer region on which the EPD has been measured exhibits slightly higher lifetimes in case of the APCVD gettered sample. In the depicted case, gettering leads to an increase in the frequency of areas with the lowest EPD. This is caused by EPD reduction transforming mid EPD regions to low EPD regions (figure 4.10).

This is no contradiction of EPD reduction, but a consequence of EPD reduction in mid-EPD regions that are transformed into regions of low EPD by the gettering step. This phenomenon is apparent when looking at the corresponding EPD map (figure 4.10).



(a) As-grown



(b) APCVD gettered

Figure 4.10.: From this pair of as-grown and APCVD gettered sister samples, it is apparent how EPD reduction in large areas of mid-EPD can lead to an increase in the frequency of low EPD areas. The EPD frequencies in figure 4.9 are based on the here depicted EPD maps.

While τ_{eff} and $[Fe_i]$ measurements on temperature reference samples have shown different behavior depending on the block height and the distance from the crucible walls (page 4.2.1), thereby indicating changes in the composition of impurities, the existing EPD data shows no difference in EPD reduction in these cases. In total, EPD reduction after P-gettering relative to an as-grown reference has been observed in more than 30 different P-gettered samples. The null result of the influence of thermal loads during gettering processes has been verified on 9 sample pairs. EPD reduction has been independently verified on wafers from low, middle and upper regions of the block as well as on wafers that are as close as possible to the crucible wall. In all of these cases (various block heights and distances from the crucible wall), EPD reduction can lead to an effective EPD of zero (i.e. bins that contain zero etch pits) over large regions, demonstrating that the maximum intensity of this effect is independent of the different impurity concentrations originating from either the crucible wall or the impurity segregation due to ongoing solidification of the melt during the block casting process.

Correlation between etch pit structures and τ_{eff}

When correlating defect etching structures with measurements of τ_{eff}, a clear correspondence between etch pit structures and low lifetime regions is observed: Regions of impaired τ_{eff} and regions of high $[Fe_i]$ can be clearly and unambiguously identified with regions containing high density etch pit structures (figure 4.11). On gettered material, however, there can be high density etch pit structures that seem to have hardly any influence on τ_{eff}. Some etch pit clusters show a stronger response to gettering than others. Among other results, this finding has been published in [60].

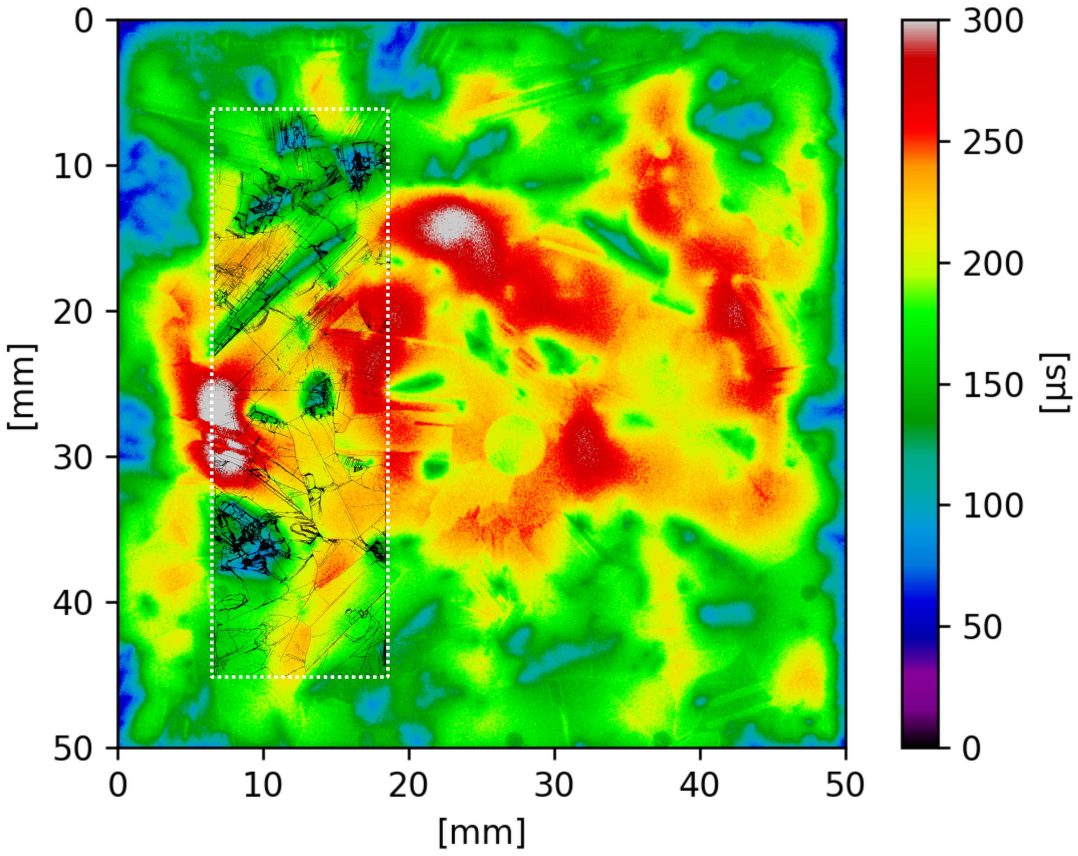
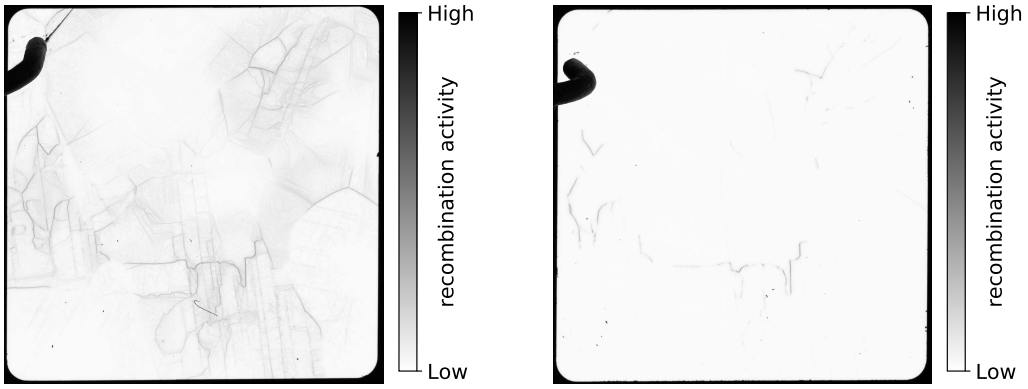


Figure 4.11.: The τ_{eff} measurement of a $POCl_3$ gettered sample (figure 4.2) is partly overlaid with optical microscope images of Secco etched samples (black structures inside the dotted rectangle). A clear correspondence between low lifetime regions (and high $[Fe_i]$ regions in figure 4.3) is seen. However, there are high density etch pit structures that seem to affect neither τ_{eff} nor $[Fe_i]$. Similar results have been published in [60].

4.3. The influence of hydrogen passivation and gettering on the surface-close recombination activity

The electron beam induced current (EBIC) measurement technique [57] allows to infer information on the surface-close recombination activity (section 3.4). Studies that combine EBIC measurements with hydrogen-free passivation techniques have been executed with the goal to separate the passivation effect of hydrogen from the influence of the gettering step, highlighting an unexpected interplay that gettering and hydrogen passivation exhibit on the EBIC contrast. In this section, details of this interplay are presented. While understanding the effect of hydrogen passivation and gettering on the EBIC signal is interesting in its own right, it is also required for the interpretation of the EBIC study in the context of EPD reduction, presented

in chapter 5.13.
Gettered lifetime samples exhibit a strong reduction in the number and intensity of surface-close recombination active structures, measured as a reduction of the EBIC contrast (figure 4.12). These findings have also been presented in [60]. For the lifetime samples that have been analysed in [60], gettering has always been studied in combination with hydrogen passivation, introduced as a by-product of surface passivation via SiN:H_x deposition in combination with fast firing. In the following, EBIC measurements are shown, that separate the steps of gettering and hydrogen passivation.



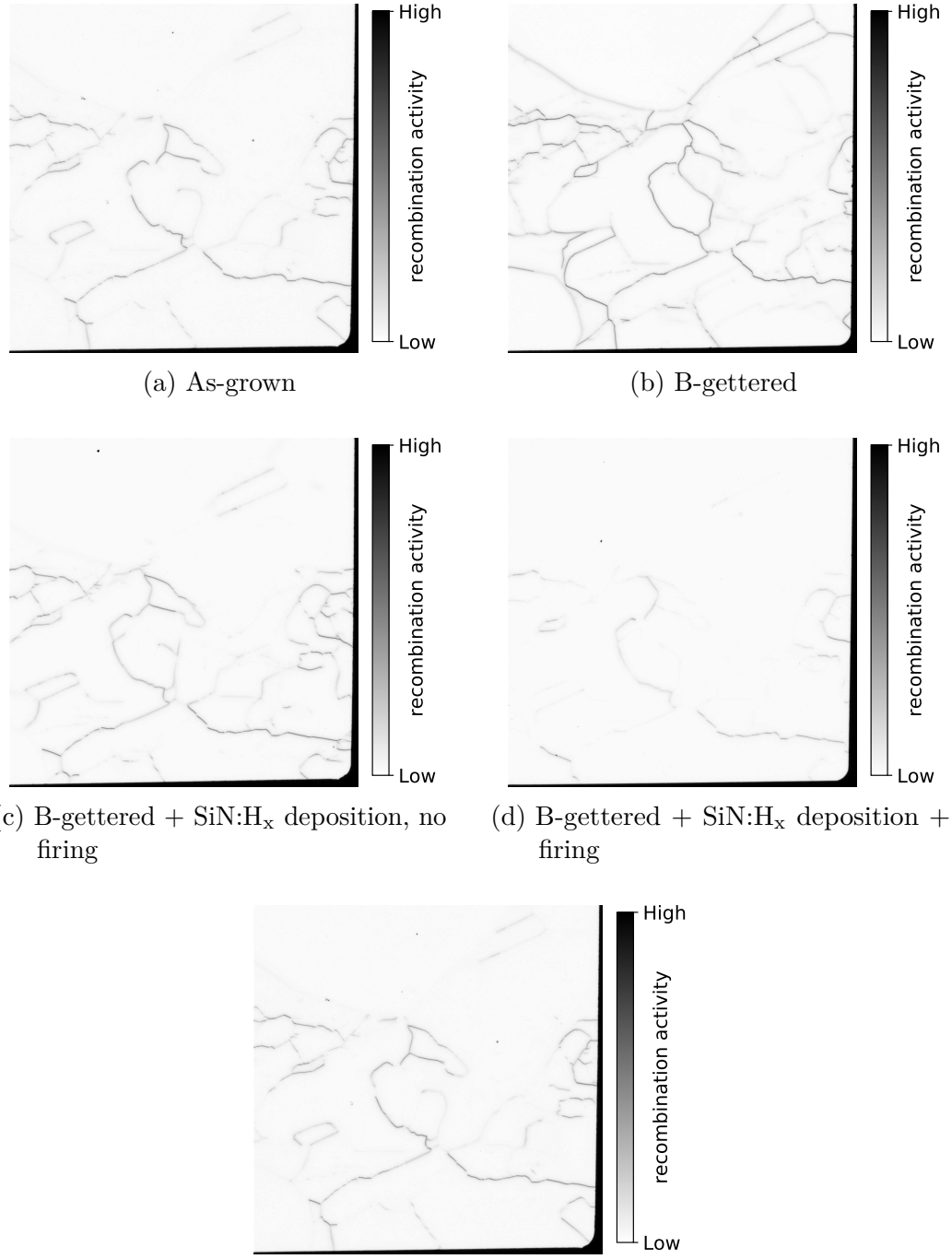
(a) As-grown (b) P-gettered + SiN:H_x + firing

Figure 4.12.: EBIC contrast of a set of sister samples in as-grown and P-gettered state. Both samples have been exposed to hydrogen passivation via SiN:H_x deposition and fast firing. The as-grown sample shows a typical distribution of recombination active structures as seen in an EBIC measurement: Most of the line-like structures in this example do not correspond to grain boundaries [60]. Gettering in combination with SiN:H_x deposition and fast firing reduces the measured recombination activity of most regions to values below the detection level. The dark segment in the top left corner is the tip of the current probe. The measured area is about 8.5 mm wide.

Three variants of hydrogen passivation are studied: 1. Hydrogen passivation by exposure to a microwave induced remote hydrogen plasma (MIRHP) [70]. 2. Hydrogen passivation by deposition of a hydrogen containing SiN:H_x layer [33] [34] [71]. 3. A similar SiN:H_x deposition followed by an additional fast firing step [33] [34] [71]. The deposition of SiN:H_x takes place at a temperature of 450 °C. The samples are exposed to a temperature of more than 400 °C for more than an hour, during which some hydrogen passivation effect is achieved [71]. The fast firing step, a brief exposure to a 850 °C environment (set point temperature), is known to strongly influence the passivation quality of the SiN:H_x layer and for facilitating hydrogen diffusion from the nitride layer to the silicon wafer [33] [34] [71]. The brief heating and the sharp drop in temperature after the fast firing process results in a hydrogen distribution that is substantially different from the slow cooling after SiN:H_x deposition.

The MIRHP treatment has been executed for 90 min at 375 °C at a pressure of 0.8 mbar, resulting from a continuous flow of hydrogen plasma and vacuum pumping. MIRHP, as a systematically independent hydrogen source, helps to identify influences that originate from the presence of the SiN:H_x layer.
This study has been executed on APCVD-B, APCVD-P, $POCl_3$ and BBr_3 gettered samples with corresponding as-grown samples as reference. Presented here are the APCVD-B gettered results, since these results are required for the results presented in chapter 5.13. The samples have been diffused in the high temperature process that is used for APCVD co-gettering throughout this thesis (figure 4.1).
From [60] it is known that as-grown samples, even when hydrogen passivation via SiN:H_x deposition and fast firing has been applied, show strong recombination activity in EBIC measurements (figure 4.12). Gettering followed by the same hydrogen passivation procedure (SiN:H_x deposition followed by fast firing) is known to result in a strong decrease of the EBIC contrast (figure 4.12). Here, when studying the effect of gettering in the absence of hydrogen passivation, surprisingly an increase of the recombination activity in the EBIC signal is measured (figure 4.13). The effect of reduced recombination activity observed in [60] (figure 4.12) is reproduced only when gettering is combined with hydrogenation by SiN:H_x deposition and fast firing (figure 4.13). The depicted example (figure 4.13) shows APCVD B-gettering results, but similar results are observed after $POCl_3$, BBr_3 and APCVD B-gettering: While gettering and hydrogenation from SiN:H_x deposition without the fast firing process results in a slight reduction of the EBIC signal and hydrogenation via MIRHP exhibits the same tendency with slightly increased intensity, the by far strongest effect is seen after hydrogenation and additional fast firing, where hardly any recombination active structures are remaining. Hydrogenation via SiN:H_x deposition and fast firing on as-grown material, i.e. in the absence of gettering, reveals a high density of recombination active structures (figure 4.12), indicating that the combination of gettering, hydrogenation via SiN:H_x deposition and fast firing is required for the observed effect.
Layers of SiN:H_x on their own can facilitate diffusion gettering processes [72]. However, the short timescale of the fast firing process discourage the interpretation that this effect is the result of diffusion gettering in SiN:H_x layers.

In summary, for all gettering methods, only the combination of gettering and hydrogen passivation leads to a reduction of the surface-close recombination activity. Gettering without hydrogen passivation increases the observed recombination activity while hydrogen passivation on its own exhibits hardly any effect. With increased diffusion temperatures (i.e. for the BBr_3 diffusion), the hydrogen-free recombination activity after the gettering step more and more exceeds that of the as-grown state. The reduction in surface-close recombination activity after P gettering in combination with SiN:H_x passivation and fast firing clearly exceeds the effect that is observed due to an otherwise similar B-gettering processes.



(a) As-grown

(b) B-gettered

(c) B-gettered + SiN:H_x deposition, no firing

(d) B-gettered + SiN:H_x deposition + firing

(e) B-gettered + MIRHP hydrogenation

Figure 4.13.: EBIC contrast of a set of sister samples in as-grown and B-gettered state. The B-gettered samples are shown in a hydrogen-free state (b) as well as after SiN:H_x deposition and after SiN:H_x deposition and an additional fast firing step. Surprisingly, recombination activity as measured by EBIC shows significant reduction only due to a combination of gettering and hydrogen release via fast firing. The gettering step alone leads to an increase in total recombination active structures. Hydrogenation via MIRHP has a small influence on the EBIC contrast, comparable to SiN:H_x deposition without firing. The measured area is about 4.5 mm wide.

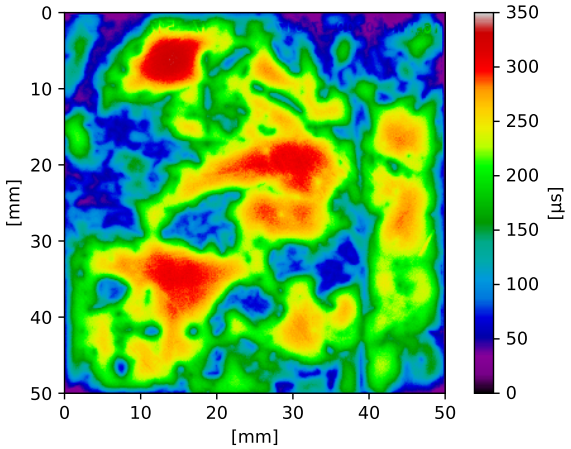
4.4. Boron based gettering

Boron based high temperature diffusion is either used for emitter formation on n-doped base material or can be used to create a region of very high doping (p^+) on p-doped material. The transition region between base doping levels and such highly doped p^+ regions exhibits an electric field (similar to the space charge region of a pn-junction) that is effectively shielding minority charge carriers from the surface, therefore reducing surface recombination activity. This technique can be used to passivate the back side of the wafer, a so-called back surface field (BSF), or it can be used for passivation of local contacts in advanced solar cell concepts.

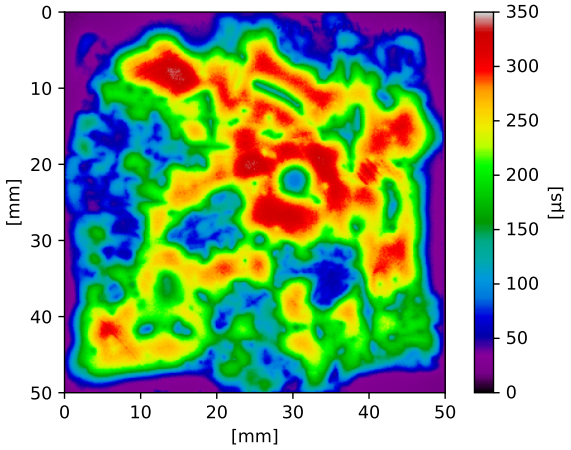
4.4.1. Effects of APCVD-B gettering on τ_{eff} and [Fe_i]

While it is possible to use boron diffusion gettering processes to significantly reduce, e.g., iron impurities from specifically contaminated material under certain conditions [69], boron diffusion gettering requires a high control of gettering conditions to be effective [69] [73]. Phosphorous diffusion gettering, on the other hand, achieves good gettering results for a wide range of processing parameters and typically results in a higher overall gettering efficacy than boron diffusion gettering [69] [73]. At the same time, diffusion of boron atoms into silicon requires considerably higher temperatures than P-diffusion process, therefore stronger detrimental effects of the high temperature step are expected for B-diffusion processes.
It has to be noted that the B-gettering processes that have been used here do not represent the state of the art of B-gettering: Most boron processes that have been used here were not intended to achieve high gettering results. Nevertheless, the results of these processes on τ_{eff} and [Fe_i] are presented. Some boron processes have been intended as part of a co-gettering step, using temperature regimes optimized for phosphorous diffusion gettering that are much lower than what is used for typical B-gettering processes. Other boron diffusion processes that have been studied here were meant to achieve high boron concentrations in the surface region, helping to distinguish between the effects of phosphorous and boron atoms on EPD reduction. However, several separate attempts to achieve significant boron gettering effects were not successful. The best gettering result achieved via boron diffusion gettering is presented in the following:

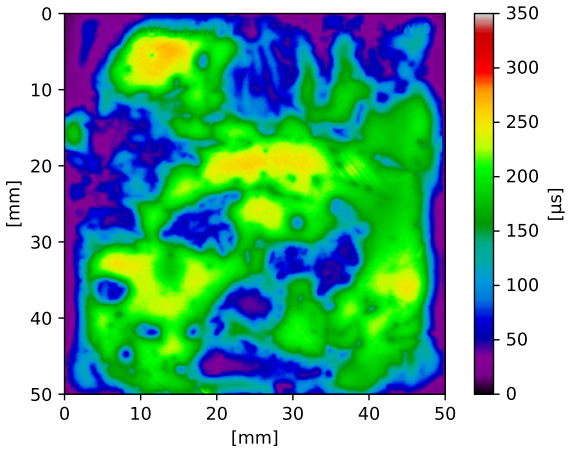
APCVD B-gettering results, using a BSG layer of 40 nm thickness, deposited at 440 °C with a nominal boron concentration of 4.5 %, show a slight gettering effect when compared to the as-grown reference sample (figure 4.14). This type of boron diffusion has been used with the aim to create surface boron concentrations that are as close as possible to phosphorous concentrations of the APCVD P-gettering process. A rather short diffusion time (920 °C peak, held for 30 minutes, figure 4.1) was chosen for this reason.



(a) As-grown



(b) APCVD B-gettered



(c) Temperature reference

Figure 4.14.: PL maps showing τ_{eff} of sister wafers in the as-grown state (a), after APCVD B-gettering (b) and corresponding temperature reference (c). The high temperature load of 920 °C during the B-diffusion results in reduced lifetimes of the temperature reference. Boron diffusion gettering can recover some of the influence of the temperature step and some regions exceed the performance of the as-grown state. However, hardly any net-gettering effect is observed for this APCVD B-diffusion process.

A considerable detrimental influence due to temperature load is observed in lifetime measurements (figure 4.14). Especially the wafer edges of the temperature reference as well as the B-gettered sample are affected by a considerable decrease in material quality. The harmonic mean of the innermost 3 cm × 3 cm is lowest for the temperature reference sample (132 µs) while gettering improves the material quality (182 µs) to a level slightly above the as-grown state (170 µs). Some gettered regions see improvement in lifetime measurements compared to the as-grown state, while some regions result in slightly reduced material quality. In comparison to the temperature reference, APCVD B-gettering has a slightly beneficial influence in all areas of the wafer, with the exception of the wafer edge.

4.4.2. EPD after boron diffusion

EPD analyses after the previously presented APCVD-B gettering process as well as after a BBr_3 diffusion have been carried out. While phosphorous diffusion gettering processes have been shown to lead to a reduction of the EPD, changes in EPD have neither been observed for APCVD B-gettering (figure 4.15) nor for the BBr_3 diffusion process (figure 4.16) or for respective temperature reference samples.
The temperature load of the BBr_3 diffusion with a peak temperature of 930 °C held over 60 min (figure 4.1) constitutes the largest thermal load that was studied for this thesis, therefore the absence of changes in EPD during this process is the most extreme data point contributing as evidence against the notion of dislocation mobility caused by thermal load.
The apparent correlation between the absence of EPD reduction in the absence of a significant gettering effect emphasizes the importance of studying EPD reduction after successful B-gettering. Unfortunately, a seemingly successful B-gettering step has been shown to result in no EPD reduction whatsoever - however, only very late into the writing process of the thesis has it been found out that the observed improvements in lifetime originate from different passivation methods of both samples [74] and can very likely not be attributed to the B-gettering step. Due to this mishap, it was long believed that B-gettering, even when resulting in significant improvements in lifetime, does not result in EPD reduction, while now, after discovering this mishap, this is still an open question.

In this chapter, various methods of gettering and their results have been presented. The here presented phosphorous-based gettering processes have been shown to improve material quality on the one hand and result in EPD reduction on the other hand. EPD reduction is not observed for Boron-based gettering processes, but at the same time, hardly any net-gettering effect could be achieved with these methods.
In the following chapter, several experiments are presented that allow to restrict existing ideas about the cause of EPD reduction. The characterization of the gettering steps that has been discussed here is central to the interpretation of these results.

In addition to that, the interplay between these gettering steps and hydrogen passivation as observed in EBIC measurements has been detailed, thereby giving sufficient background for the interpretation of the EBIC results of section 5.13.

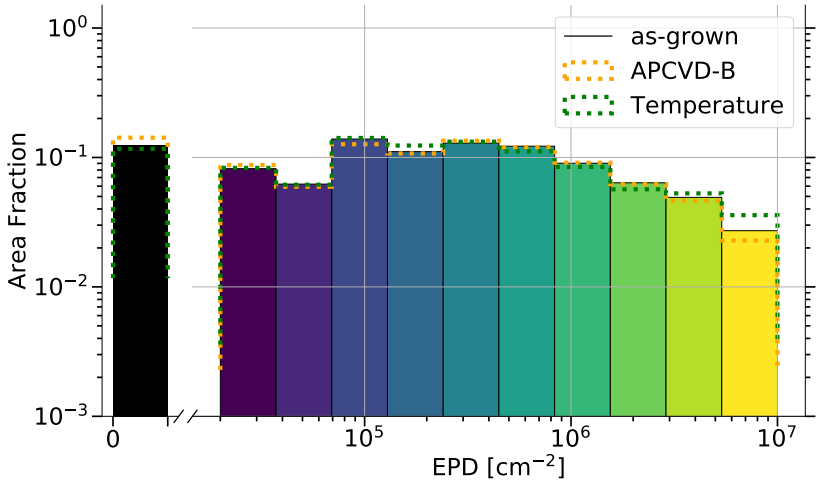
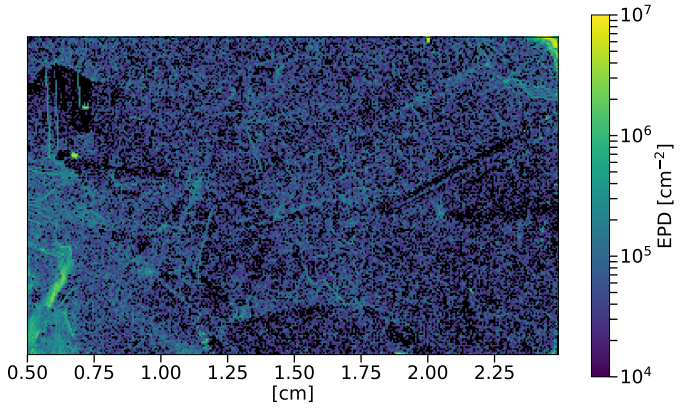
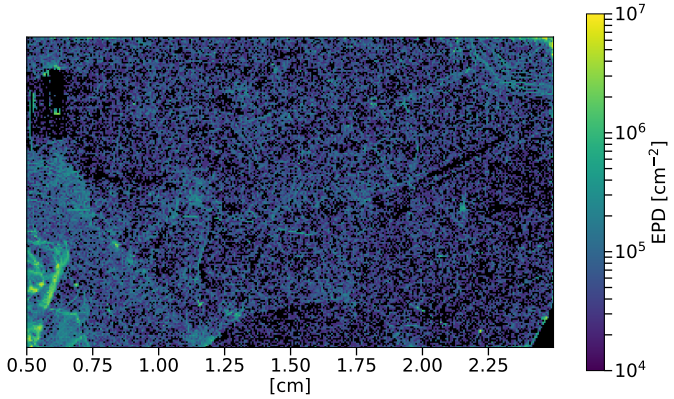


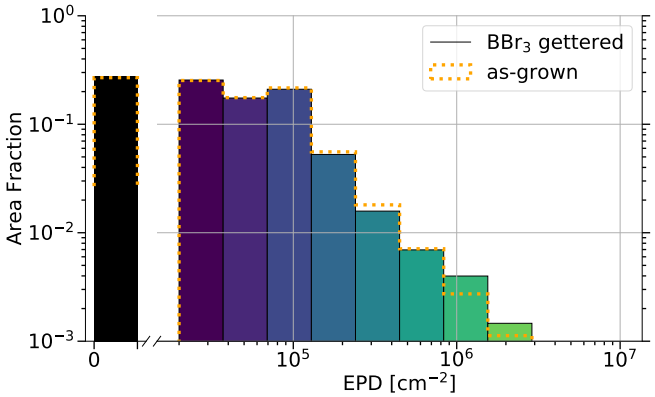
Figure 4.15.: EPD measurements of a set of sister samples, for studying the effect of APCVD B-gettering on the EPD: Neither the gettering process nor the temperature process in isolation is modifying the EPD.



(a) As-grown



(b) BBr_3 gettered



(c) Comparison

Figure 4.16.: EPD measurements of the as-grown and BBr_3 gettered sister wafer. No change in EPD is observed after BBr_3 gettering. Thermal processing peaks at 930 °C over the course of 60 min (figure 4.1), constituting the largest thermal load that was studied during this work. Temperature reference samples of a further sample pair show no influence on the EPD due to the temperature load. The BBr_3 processing and passivation has been the work of Christian Fischer [74].

5. Investigations on the EPD reduction mechanism

It has been shown that the EPD can be reduced by P-gettering. While EPD reduction has been described in the literature before [20] [19], so far there have been only speculations about the underlying mechanism. The ideas discussed in the literature often equate reduction of the EPD with the disappearance of dislocations. In the literature, various mechanisms are discussed that are hypothesized to facilitate dislocation motion at low temperatures [20] [19]. Once mobile, it is assumed that dislocations of opposite Burgers vectors can annihilate pairwise [20] [19] or that dislocations annihilate at grain boundaries or surface sinks [19]. Dislocation mobility has been studied in presence of external forces [75] whereas in absence of external forces, dislocation mobility is expected only for temperatures much closer to the melting point of silicon than what was used here during high temperature diffusions (840 °C) [17] [76] [18]. The following sections describe a compilation of experiments resulting in strong empirical evidence against the notion that annihilation of dislocations is the cause of EPD reduction. Some proposed mechanisms for the mobility of dislocations are falsified explicitly and in the contrary, various experiments show that mobility of dislocations is not required to explain the phenomenon of disappearing etch pits. Many parts of this chapter build upon results published in [65].

Ideas for explaining EPD reduction that do not require mobile dislocations revolve around the idea that the defect etch process is altered due to the effects of gettering [20]. EPD reduction in this view is a failure of the defect etch to enter a reaction with dislocations after gettering.

Diffusion gettering modifies the wafer in two ways: 1. New atomic species are diffusing into the crystal and 2. Metallic impurities are removed from the crystal. It is conceivable that either the added presence of atomic species that are introduced during the diffusion gettering process, i.e. either P, O or silicon self interstitials, inhibit the defect etch reaction at dislocation sites. Alternatively, the defect etch process might not be inhibited by in-diffusion of external atomic species but, conversely, dislocations might need to be decorated with certain impurities for the defect etch reaction to occur. EPD reduction might then be explained as the inability of the defect etch to enter a reaction with impurity-lean dislocations. In the following, a selection of experimental results are described that allow distinguishing these cases. The combined evidence of experiments presented here as well as observations found in the literature turn out to be explainable by a single simple principle. Parts of this chapter build upon [65].

5.1. EPD reduction close to grain boundaries

In regions with minimal EPD after gettering (typically regions of low EPD in the as-grown state), remaining etch pits are typically located close to grain boundaries. Often large grains of low EPD show zero etch pits for large parts of the grain, except in vicinity of grain boundaries (figure 5.1). For a typical low density grain of 6 mm^2, 57 etch pits have been counted close the grain boundaries (amounting to 9 % of the total grain area) whereas the remaining 91 % of the wafer area contain only 10 etch pits. Similar observations are typical for low EPD grains after gettering.
The large surface area of grain boundary defects is known to be a possible site for impurity element accumulation [77] as well as for precipitation [78], therefore dislocations close to such regions could, despite gettering, plausibly retain a highly decorated state. However, the metal concentration at grain boundaries tends to depend on the type of grain boundary [77] [78] and this aspect has not been studied in detail here.
A further possible explanation for the observation of less EPD reduction close to grain boundaries, as well as the observation of absence of EPD reduction in cluster regions, could be mechanical stress: In high mechanical stress regions, silicon bonds could be weakened and therefore defect etching increased. In this picture, EPD maps exhibiting EPD reduction after gettering would indicate regions of mechanical stress.

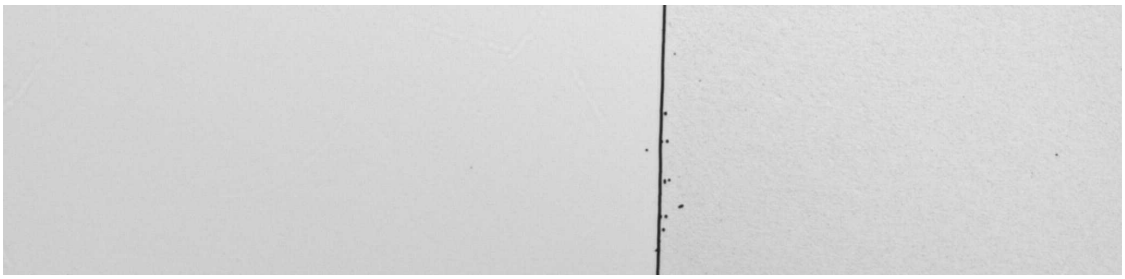


Figure 5.1.: A 1.5 mm wide section of the surface of a gettered wafer after Secco etch (a region of low EPD on the bottom left of same wafer that is depicted in figure 5.10a). Etch pits that are still present after gettering steps tend to be located close to grain boundaries.

5.2. EPD reduction with various defect etchants

In order to exclude that EPD reduction is a feature specific to a certain defect etch solution, a comparison of EPD reduction using different defect etch solutions has been carried out. Compared are the Secco etch [46], the Schimmel etch [47], the Sopori etch [53] and the Wright etch [48]. A pre-study on as-grown material that is not discussed here has been carried out with the purpose to find etching times and parameters for achieving comparable EPD values with all four of the solutions

used in the following.
For gettering, the same industry standard $POCl_3$ diffusion that has been discussed in chapter 4 has been used. The gettering effect of this $POCl_3$ process on the material used here is well known [64], [60]. For each etchant, the compositions, the etch process and results on as-grown samples, as well as on gettered and temperature control sister samples are detailed in the following.

Secco etch

Defect etching with the Secco etch has been carried out as described in section 3.3.2, using ultrasonic agitation, here using an etching time of 60 s. EPD reduction has been observed on numerous Secco-etched samples in previous experiments [60] and is clearly present in this experiment, too (figure 5.2). Temperature reference samples, that underwent the temperature load of the $POCl_3$ gettering process in absence of a gettering sink, show unchanged EPD compared to the as-grown state.

Wright etch

The Wright etch is intended as an etch suitable for (100) and (111) oriented silicon of either p- or n-type [48]. Because it is among the most common choices for defect etching crystalline silicon [45], it has been included in this study. The Wright etch has been used in a composition of two volume parts HF (50 %), one part HNO_3 (65 %), one part of a 5 molar aquatic solution of CrO_3, two parts of CH_3COOH (99.8 %) and two parts of an aquatic solution containing $1/30\,\mathrm{g\,mL^{-1}}$ of $Cu(NO_3)_2 \cdot 3\,H_2O$. A previously determined etching time of 240 s leads to an as-grown EPD that, for most regions, is comparable to what is observed after Secco etching (figure 5.2) and $POCl_3$ gettering results in EPD reduction with Wright-etched samples, too.
Some differences between Wright-etched results and EPD results of the other etchants can be noticed and are explained in some detail in the appendix (chapter A.1). The enhancement in the EPD of certain grains is explained by surface roughness, caused by the tendency of the Wright etch to react with dislocation free surfaces of certain crystal orientations. In other grains, the Wright etch shows a lower EPD when compared to other etchants. After gettering, the same grains exhibit a lower EPD than what is observed for the other etchants, too. Analysing the etch pit data shows that grains of reduced EPD feature systematically smaller etch pits than grains of enhanced EPD (chapter A.1). The observed differences are therefore likely due to crystal orientations that deviate from the (100) and (111) directions for which the Wright etch is intended.
For the scope of the argumentation of this chapter, it is sufficient that EPD reduction is present on Wright-etched samples, too.

Schimmel etch

A further popular defect etch that uses hexavalent chromium in the form of chromic acid as oxidizing agent is the Schimmel etch, consisting of two volume parts HF with a concentration of 50 % and one part of a 1 molar aquatic solution of CrO_3 [47]. This etchant does not require ultrasonic agitation. Results shown here have been obtained with etching times of 90 s and are similar to what is observed with the Secco etch (figure 5.2).

Sopori etch

Unlike the other etches discussed here, the Sopori etch does not contain chromium in a high oxidation state as oxidizing agent, but uses concentrated HNO_3 instead. First trials with the Sopori etch resulted in extreme over-etching even for etching times as short as 20 s. Reducing etching times even further will at some point negatively influence the repeatability of results: The part of the wafer that is close to the bottom part of the carrier is systematically longer in contact with the etching solution since the bottom wafer part is coming in contact with the etchant first when the wafer enters the solution and likewise it leaves the solution last, when a wafer is removed from the solution. In addition, for the amount of time between etching and rinsing, unevenly distributed etch solution is sticking to the wafer surface, continuing the etch process in some regions. The timescales of these processes, dipping the wafer, removing the wafer from the solution as well as the time for which the wafer has to be handled between the etching and rinsing step, should be small compared to the actual etching time for good repeatability.
Etching times can be increased by avoiding ultrasonic agitation, however for some solutions ultrasonic agitation is important to avoid surface stains (e.g. caused by gas bubbles forming and sticking to the surface during etching), hence this way for increasing the etching time was avoided. Other means to reduce the reaction speed are either dilution or cooling of the etchant. It was decided to use cooling in favor of dilution, as to not change the chemical composition of the etchant.
Here, the Sopori etch, a mixture of 36 parts HF with a concentration of 50 %, 15 parts of CH_3COOH (99.8 %) and 2 parts HNO_3 with a concentration of 65 %, has been used after cooling the etch to 0 °C with an ice bath before and during the etching process in addition to ultrasonic agitation. Results on as-grown and gettered sister wafers after an etching time of 80 s show EPD reduction with the Sopori etch in similar strength and fashion as observed with the Schimmel or Secco etch (figure 5.2). However, some regions featuring low EPD for the as-grown Secco and Schimmel sister wafers appear with increased EPD after Sopori etch. The affected regions are independent of the grain structure and therefore likely artifacts of the etching process. It is known that, for some defect etchants, cooling leads to unexpected results [55] and it is possible that the additional etch pits seen for the Sopori etched as-grown sample are artifacts appearing when solutions are cooled. Since here it is not intended to use the Sopori etch for further experiments, the

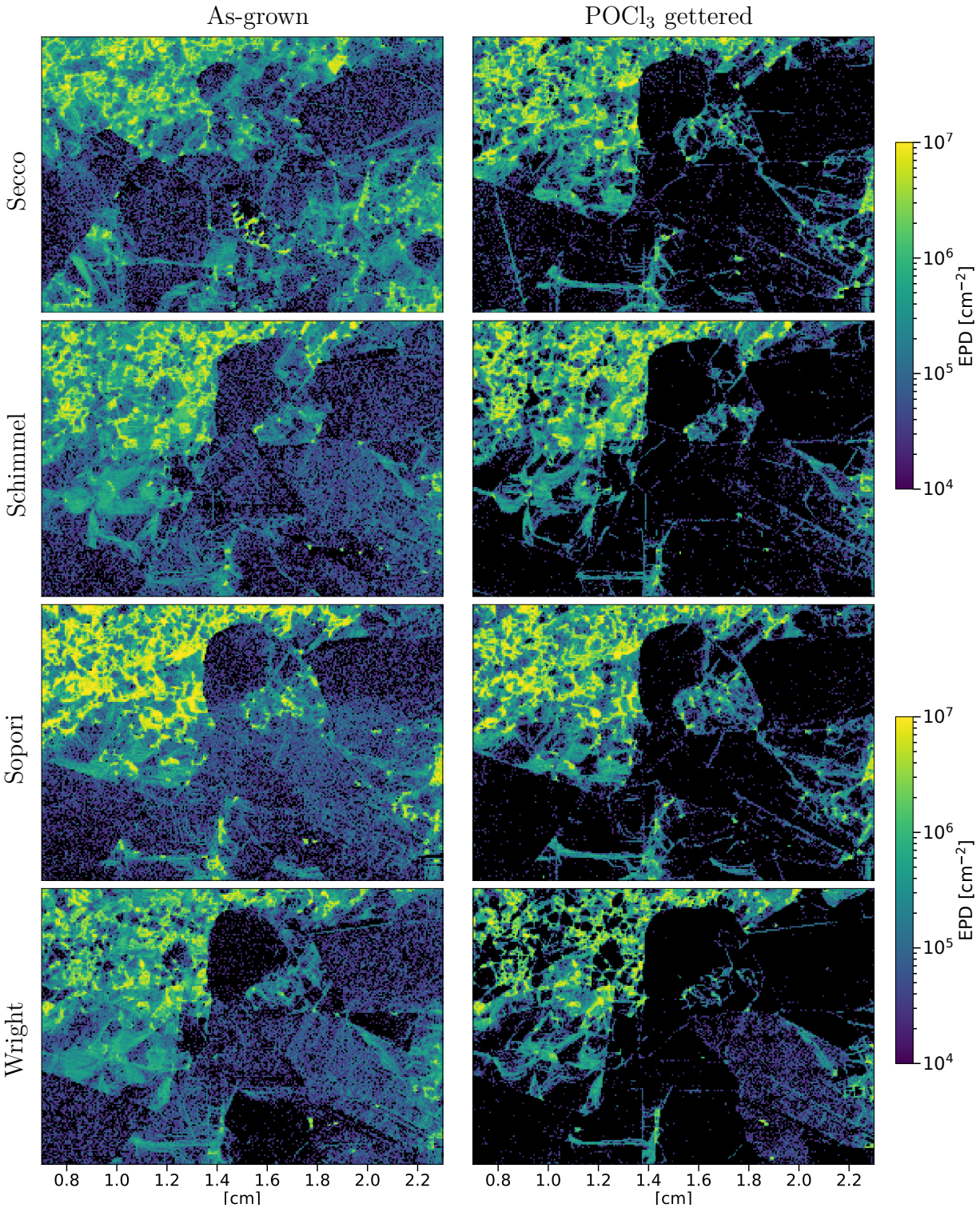


Figure 5.2.: EPD of as-grown (left) and $POCl_3$ gettered (right) sister samples after defect etching with various etchants. The overall EPD in the as-grown state is comparable among the samples shown. The number of etch pits in low and mid EPD regions is reduced by about one third in the gettered samples, while clustered EPD regions remain unchanged. EPD reduction occurs in all observed samples, regardless whether the oxidizing agent is chromium based or chromium-free, therefore it can be excluded that EPD reduction is an artifact specific to certain etch solutions.

result most important in this context is the presence of EPD reduction similar in strength and fashion to the Cr_6^+-based etchants.

In summary, all tested etchants result in a comparable overall EPD as well as similarly strong EPD reduction for all etchants (figure 5.2). EPD reduction as an artifact of a specific defect etching solution can thus be excluded.

5.3. EPD reduction on high performance mc-Si

In recent years, the pursuit of novel ways to grow mc-Si has lead to the development of so-called high performance mc-Si (HPMC-Si) material. This material is characterized by unusually high results in lifetime measurements. EPD measurements on a set of as-grown, $POCl_3$ gettered and temperature reference samples have shown that high performance material, too, is subject to EPD reduction after P gettering (figure 5.3), thereby demonstrating that this effect is not limited to certain kinds of crystal growth. Understanding EPD reduction therefore is relevant for the understanding of materials that are likely to be the future of mc-Si photovoltaic applications.

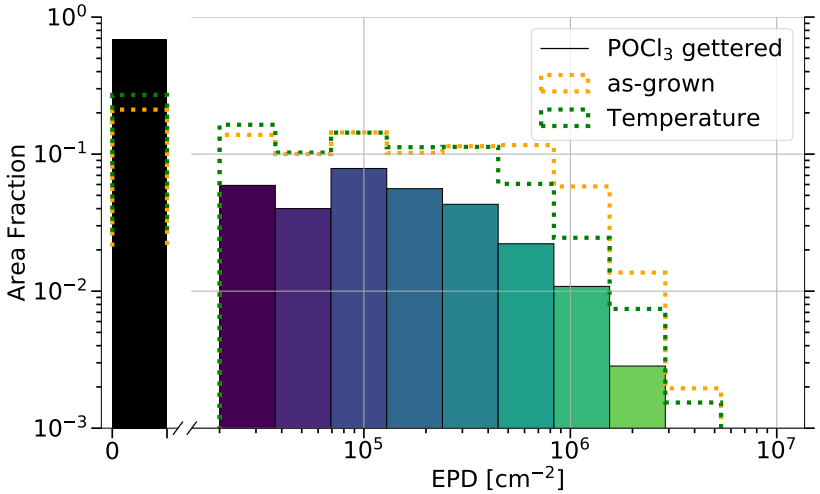


Figure 5.3.: EPD measurements after $POCl_3$ gettering demonstrate that high performance mc-Si material can be subject to EPD reduction, too. The samples that are shown here are nearly free of regions with clustered etch pits. In other regions of the same material, extended regions of clustered etch pits have been observed.

5.4. EPD with varying etching times

One motivation for this study are SEM images that show etch pits differing in size by about an order of magnitude (figure 5.4), demonstrating that there are circumstances that cause the etching rate on the same material to vary drastically. By explicitly varying the etching time, the question is addressed, whether EPD reduction could be a reduction in the etch rate alone. If new etch pits appear with increased etching time, EPD reduction could be explained by a modified etch rate for certain dislocations.

For this purpose a $POCl_3$ gettered wafer, exhibiting EPD reduction, is treated repeatedly with the Secco etch for a total duration of 1200 s. In between etch steps, optical microscope images of the wafer surface are taken for EPD analysis. Because the long etching time considerably degraded the surface quality over large parts of the wafer, the EPD analysis was restricted to a rectangular area of size 11 mm^2. The chosen analysis region is part of a single grain which kept a sufficiently good surface quality for automatic analysis. Furthermore, the optical microscope analysis has been cross-checked with SEM scans. Etching for even longer times has not been found practical: Wafer regions of high EPD are dissolved completely after 1200 s of Secco etch, grain boundaries are becoming extremely fragile and most of what remains of the wafer can hardly be used for automatic EPD analysis.
The wafer region that has been analysed corresponds to a typical low EPD region in the as-grown state (figure 5.5). It turns out that EPD reduction can be partially reversed by extreme etching times (figure 5.6), however there is still an order of magnitude difference between the as-grown EPD and the EPD that could be reached by increasing the etch time. We therefore conclude that a reduction of the defect etch rate is at least part of the reason for the phenomenon of EPD reduction after P-gettering.

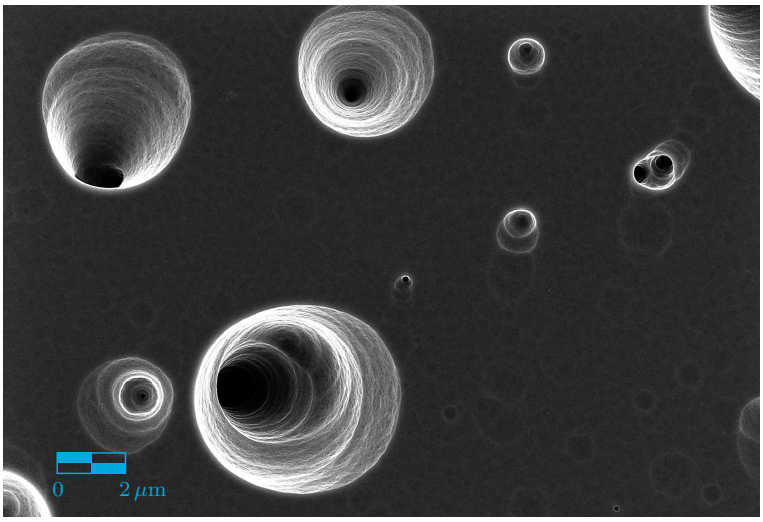


Figure 5.4.: Etch pits on the same material can vary in diameter by more than an order of magnitude. This indicates that there is a mechanism causing preferential etching for certain dislocations. Different shapes of etch pits, i.e. in case of the Secco etch whether the dark center of an etch pit is located in the middle or at the border of an etch pit, indicates the inclination of the dislocation line to the wafer surface [43] [79].

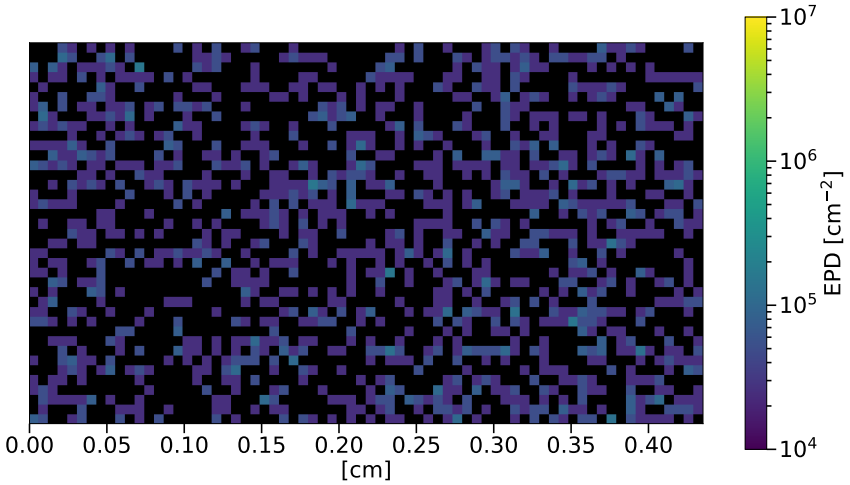


Figure 5.5.: As-grown EPD map of the region analysed in figure 5.6 after a 90 s Secco etch. Only a 4.4 mm wide subregion of a single grain is used for this analysis, therefore the EPD map shows a rather homogeneous distributions of etch pits. This figure demonstrates that the region that is studied in this experiment (figure 5.6) is a typical region of low EPD in the as-grown state.

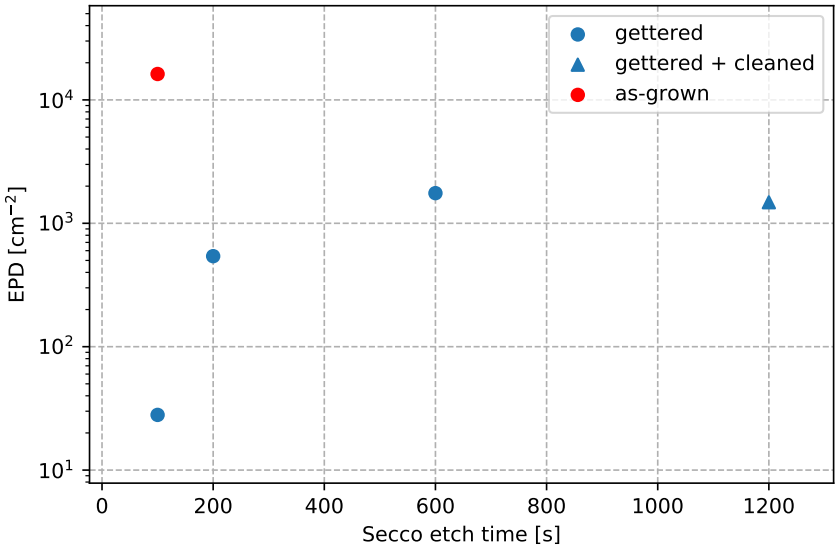
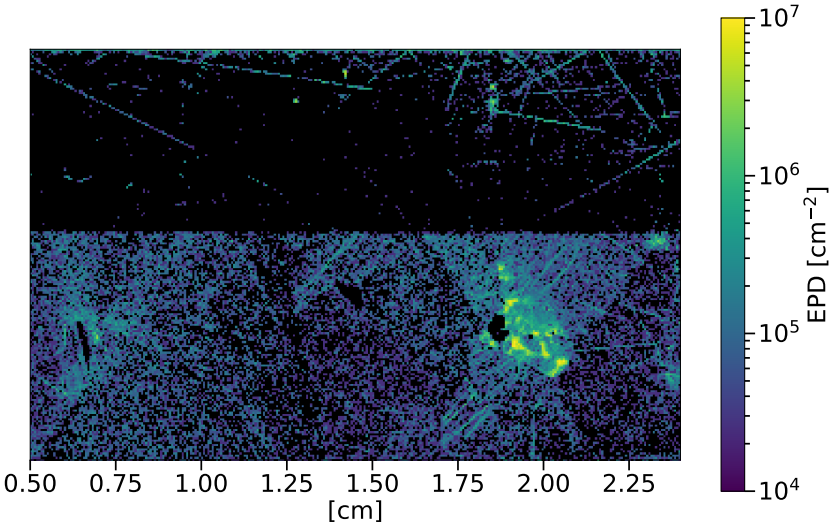


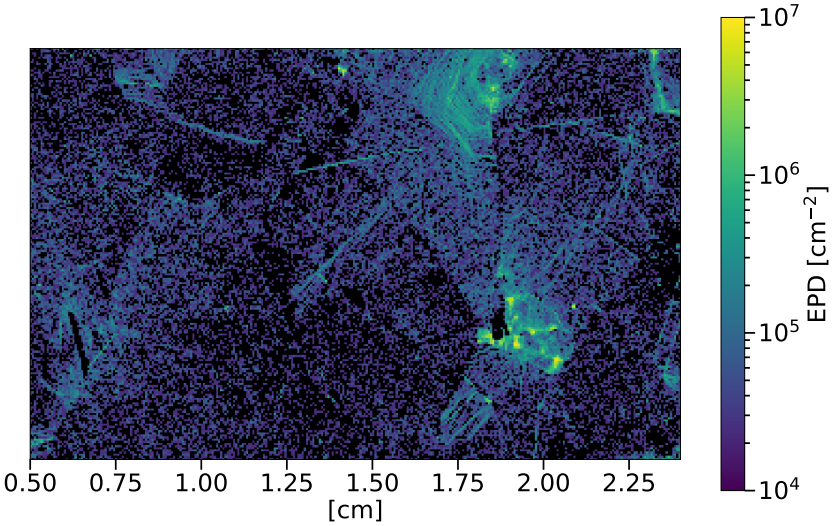
Figure 5.6.: Mean etch pit density of a gettered wafer after Secco etch, averaged over a 11 mm^2 sized region within a single grain, plotted as function of etching time. The EPD of an as-grown sister wafer is given as reference (red dot) and corresponds to a typical low EPD region (depicted in figure 5.5). After gettering and 100 s of Secco etch, hardly any etch pits remain. With increasing etching time, new etch pits appear. This effect seems to plateau at an EPD that is about an order of magnitude below the value of the as-grown state. EPD reduction therefore is, at least in part, caused by a reduction of the defect etchants reaction rate. Due to heavy surface staining at prolonged etch times, the sample surface had to be cleaned with a 30 s manual fine polishing step (Syton SF1 polishing, see chapter 3.3.1) before the data point at 1200 s could be recorded. Despite this cleaning step, only a 5 mm^2 region (a subset of the very same region used for the other data points) could be used for the EPD measurement. It is remarkable that during this process, etch pit cluster regions of the wafer have dissolved completely.

5.5. EPD after gettering of partially masked surface

During the APCVD P-glass deposition, parts of the wafer can be masked by placing a small strip of dummy silicon material on top of the wafer that is to be processed. Thereby, gettered and ungettered regions are created next to each other on the very same wafer. In this way systematic differences due to material and processing steps can be minimized. The masked area features an EPD comparable to the as-grown wafer, whereas the unmasked region exhibits EPD reduction (figure 5.7). This result excludes that systematic differences due to processing differences between wafers are causal to EPD reduction. Furthermore, a comparison between gettered material and a temperature reference sample is achieved without the use of a sister wafer.



(a) Partially masked wafer



(b) As-grown sister

Figure 5.7.: EPD map of a wafer that has been partially masked during APCVD P glass deposition (a) and as-grown sister sample (b). Only the unmasked region (upper half of (a)) exhibits EPD reduction.

5.6. EPD after multiple gettering steps

In this section it is studied how a repeated application of the same gettering step for multiple times affects EPD reduction. EPD maps after a single gettering step are compared with a sister sample for which the gettering step is repeated multiple times, thereby increasing the effects of the gettering step. For this purpose, sister samples have been prepared to compare the EPD between an as-grown, as well as a standard $POCl_3$ gettered wafer with a wafer for which $POCl_3$ gettering and emitter removal process was done for five times in total. Gettering multiple times increases the EPD reduction effect in mid and low EPD regions when compared to a single gettering step (figure 5.8). EPD reduction is thus shown to be a gradual effect. No significant effect on cluster regions is observable with the optical microscope based analysis (figure 5.9).

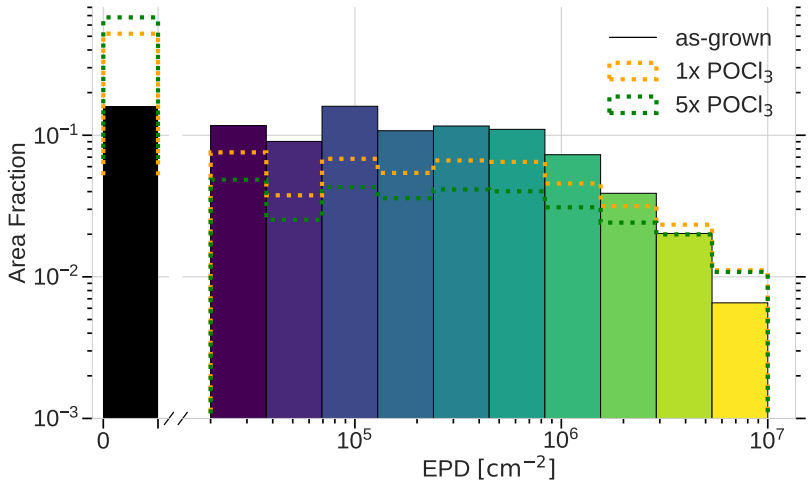
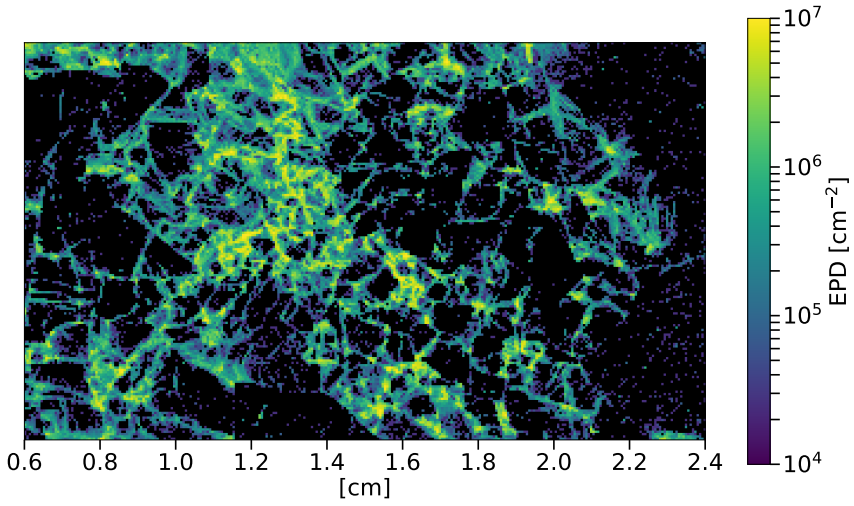
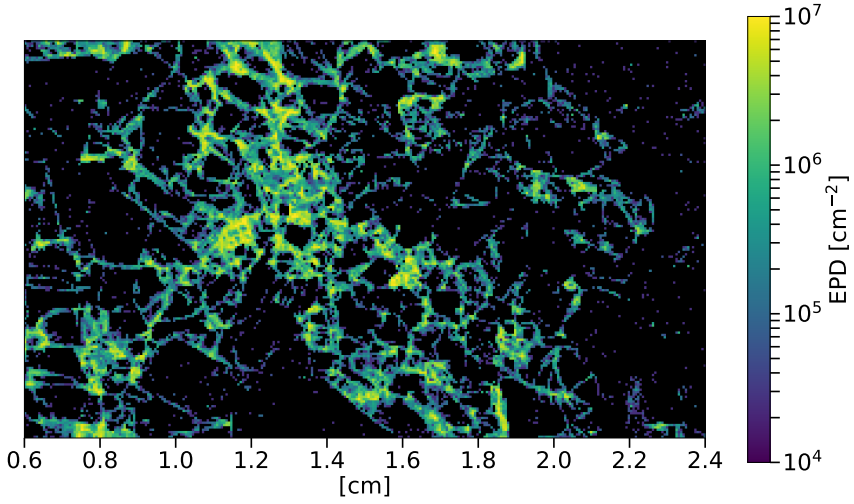


Figure 5.8.: Comparison of EPD sister samples after a single as well as after five repeated $POCl_3$ gettering steps. A comparison with the as-grown reference sample shows that the first gettering step is the dominant contribution to EPD reduction. With the combination of four additional gettering steps, a significant further reduction of the EPD is achievable.



(a) Single $POCl_3$ gettering step

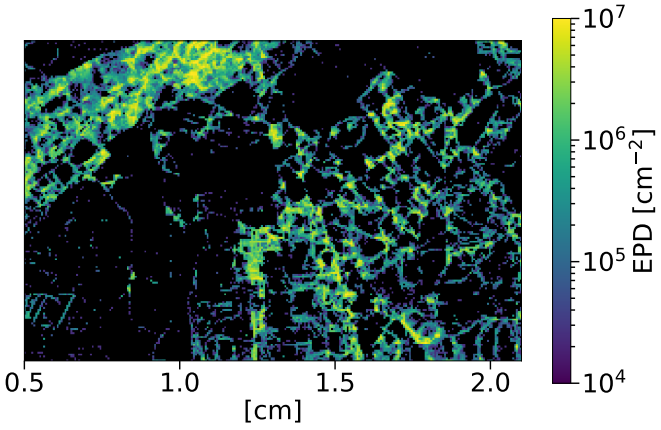


(b) 5x $POCl_3$ gettering

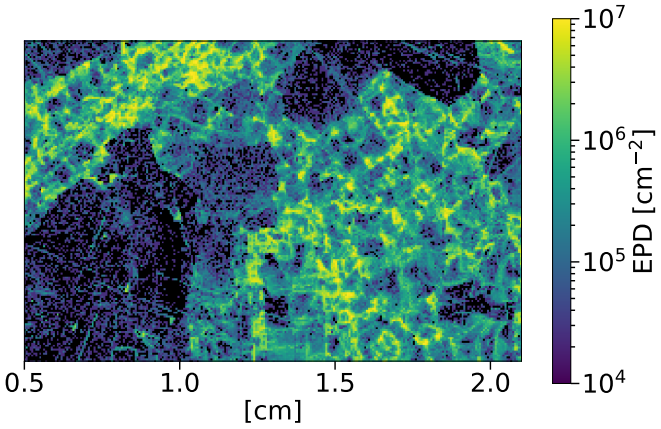
Figure 5.9.: EPD of a $POCl_3$ gettered sample (a) and a sister sample for which the same $POCl_3$ gettering process was executed five times in succession (b). Increasing the strength of the gettering effect by repeating the gettering step leads to stronger EPD reduction in mid and low EPD regions. Cluster regions remain unaffected by repeated gettering.

5.7. EPD reduction with one-sided gettering

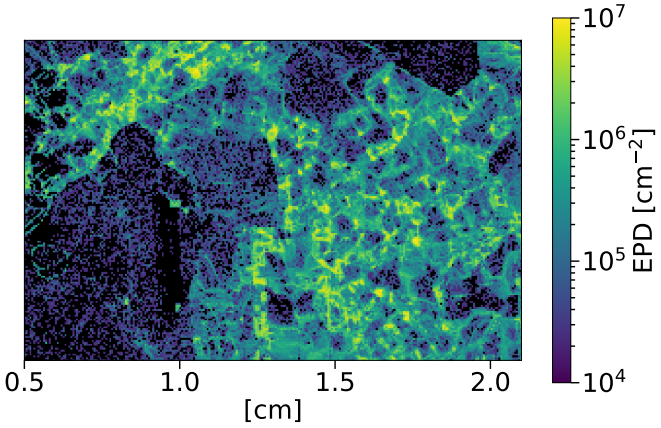
With APCVD-based diffusion gettering, the P-glass deposition process is separate from the diffusion step and it is easily possible to apply a gettering sink and execute a gettering process only on one side of the wafer while the other wafer side is left untreated. Experiments with such a one-sided gettering process and subsequent EPD analysis of both wafer sides on the very same wafer have shown that EPD reduction occurs only on the gettered wafer side, i.e. that side of the wafer on which the doping glass has been deposited (figure 5.10). The EPD of the ungettered wafer side that was not covered by a doping glass during diffusion remains largely unchanged compared to the as-grown state (figure 5.11). One-sided EPD reduction after one-sided gettering is central empirical evidence against the hypothesis that dislocations could be mobile in the applied thermal conditions (figure 5.12).



(a) Gettered wafer side



(b) Ungettered wafer side



(c) As-grown reference

Figure 5.10.: EPD maps of both sides of a one-sided gettered wafer and of a sister as-grown sample. The gettered wafer side (a) exhibits EPD reduction whereas the flip side of the very same wafer (b) shows an EPD similar to the as-grown reference (c). This is central evidence against the hypothesis that dislocations could be mobile in the applied thermal conditions (figure 5.12).

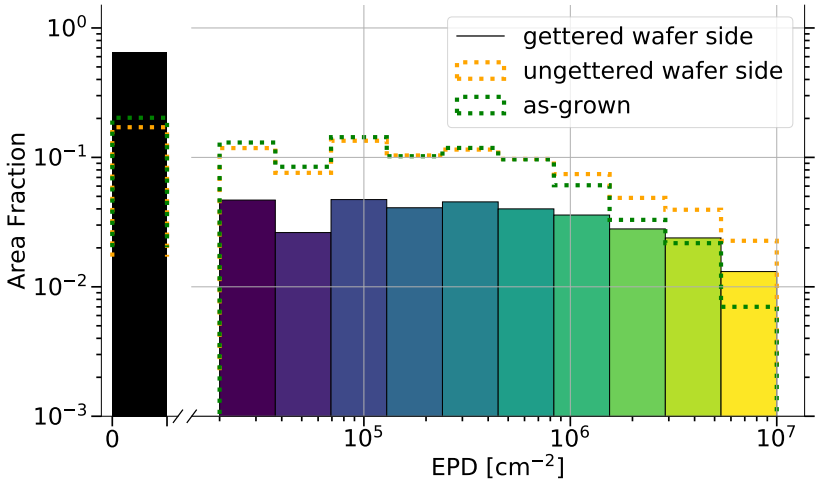


Figure 5.11.: EPD frequency of the samples depicted in figure 5.10 shows that the ungettered wafer side exhibits similar EPD as an as-grown sister for most EPD bins.

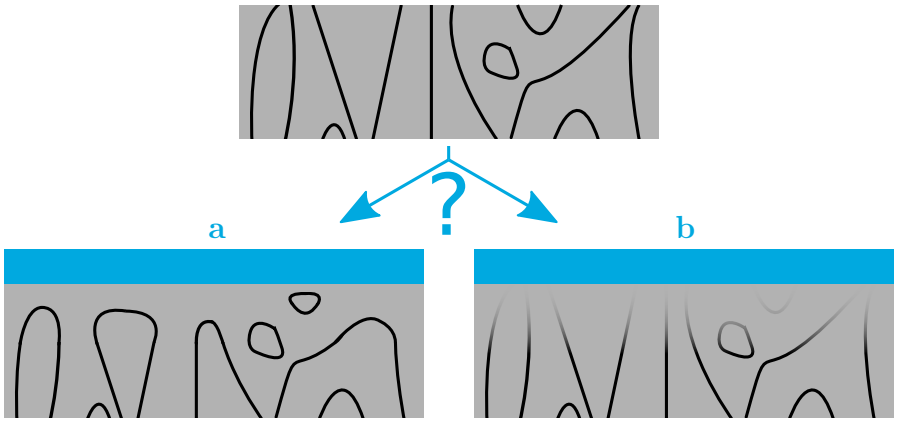
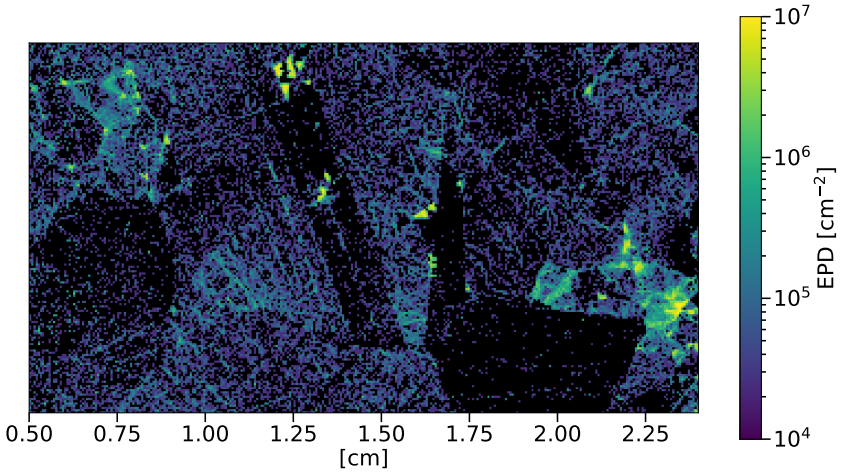


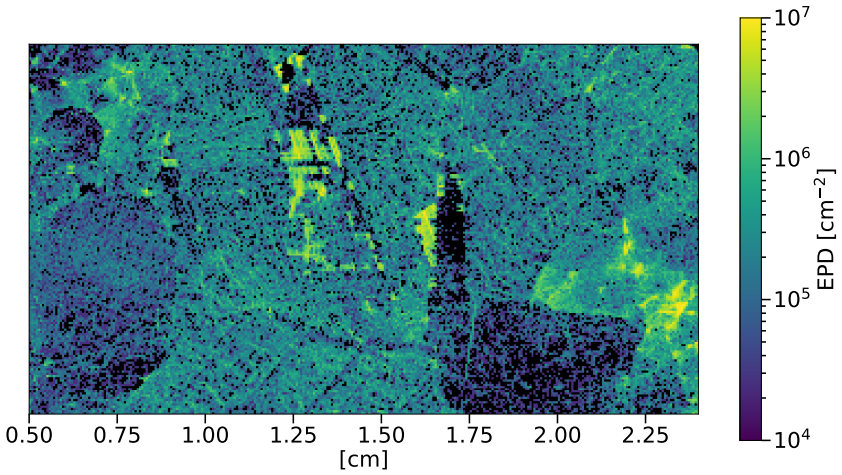
Figure 5.12.: Schematic drawing of dislocations in the as-grown crystal (top) and in the case of one-sided EPD reduction (bottom). The gettered side is marked in blue. If EPD reduction is the consequence of dislocations becoming mobile and vanishing from the material, one-sided EPD reduction would have to result in a situation as depicted in case **a**. Such a model requires each a pair of joining dislocations to actually come together and have the same Burgers vector. These assumptions are unlikely and unfounded as well as hard to reconcile with strong EPD reduction in low-EPD regions, where due to low dislocation density, the probability for two dislocations to merge should be reduced, relative to mid-EPD or cluster regions. A much simpler interpretation is case **b**: EPD reduction is the inability of the defect etch to delineate dislocations after gettering whereby the location of dislocations remains unaltered

5.7.1. One-sided EPD reduction with APCVD co-gettering

Combining the observation presented in the previous section that one-sided gettering leads to one-sided EPD reduction and the observation that B-gettering does not result in EPD reduction (section 4.4.2), it is not surprising that co-gettering results in one-sided EPD reduction, too (figure 5.13).



(a) P-gettered wafer side



(b) B-gettered wafer side

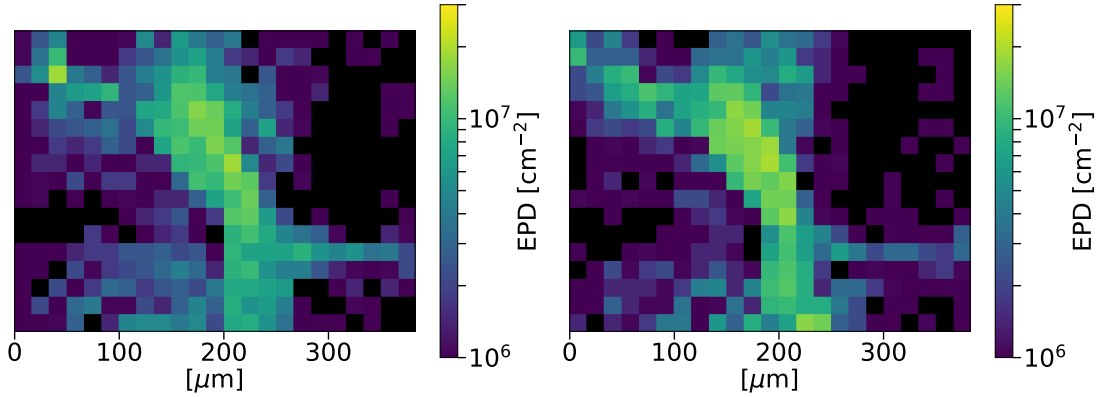
Figure 5.13.: EPD measurement of both sides of the same co-gettered wafer exhibit one-sided EPD reduction similar to what is observed after one-sided P-gettering. This is in agreement with the observation that B-gettering does not cause EPD reduction.

5.7.2. Cluster EPD on opposing wafer sides after one-sided gettering

Opposing wafer sides on the very same wafer exhibit a similarity between grain structures that is much higher than what is observed in sister samples. When comparing both sides of the same wafer, steps that contribute to thinning of the wafer (saw damage removal, emitter removal, polishing) reduce the distance between the two surfaces under study. For sister wafers, however, a thinning of the wafer increases the distance between the surfaces of EPD analysis, and therefore increases the observed dissimilarities. Additionally, between two sister wafers, there is material loss due to the wafer cutting process.
It is possible that the observed absence of EPD reduction in etch pit clusters is simply due to the limitation of the optical microscope. However, a study of etch pit clusters in sister samples has been unsuccessful because etch pit structures on both wafers at the required magnifications are too different to find unambiguous correspondence between cluster regions on both wafers. For one-sided gettered wafers where the EPD can be measured on both wafer sides, regions with unambiguous correspondence can be identified, enabling the study of possible changes in the EPD of etch pit clusters. In total five cluster regions have been compared for evidence of EPD reduction. EPD data based on SEM images shows no reduction of EPD in etch pit clusters (figure 5.14) for any of the studied regions. On the contrary, the depicted example exhibits a slight increase in cluster EPD on the gettered wafer side. From the SEM image of the etch pit cluster, it can be seen that the cluster is confined to a single grain and that this grain is smaller on the gettered wafer side (figure 5.15). When restricting the analysis to the cluster contained by the grain in the center of the SEM image, the absolute number of etch pits is changing by 6 % with the higher number of etch pits (about 1700) in the cluster on the gettered wafer side. It is noteworthy, that the etch pit counting in SEM images with the presented algorithm is prone to similar uncertainties as have been discussed for the optical microscope: Etch pit structures recorded via SEM can form conglomerates in the binary image, too, but since the etch pit size in clusters is varying strongly, a simple correction by etch pit size is not possible and therefore not applied here.

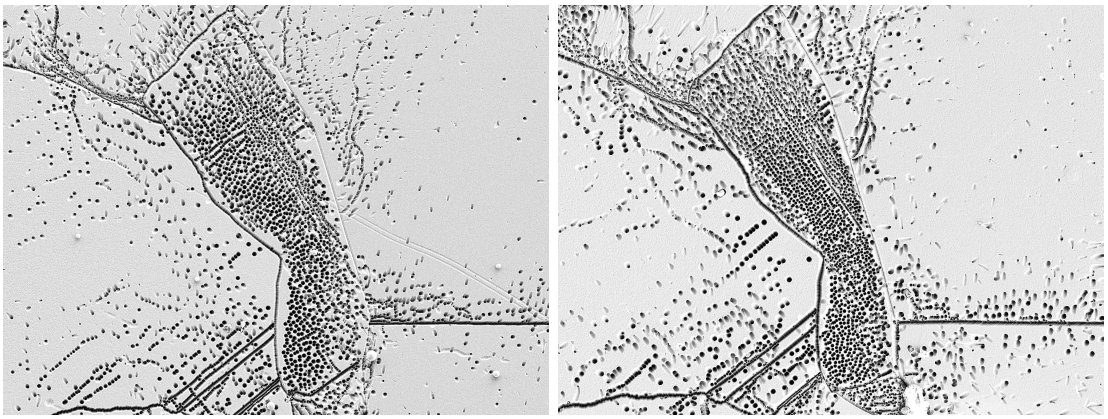
5.7.3. Etch pit size reduction on opposing wafer sides after one-sided gettering

When analysing both sides of the same wafer (here, the sample depicted in figure 5.10a and figure 5.10b is used), it is possible to find a few regions where etch pit structures on both wafer sides are highly correlated (figure 5.16). A natural interpretation is that pairs of such etch pits on both wafer sides originate from the same dislocation line.
Comparing the size of these etch pits on both wafer sides, it turns out that etch pits on the gettered wafer side appear with noticeable less depth and than on



(a) Ungettered wafer side (b) Gettered wafer side

Figure 5.14.: EPD measurement of an etch pit cluster based on SEM images of the front and back side of a one-sided gettered sample (figure 5.15). No reduction of the EPD in clusters is observed. The color scale has been adjusted compared to EPD maps based on optical microscope data to adjust for the higher resolution of SEM images.

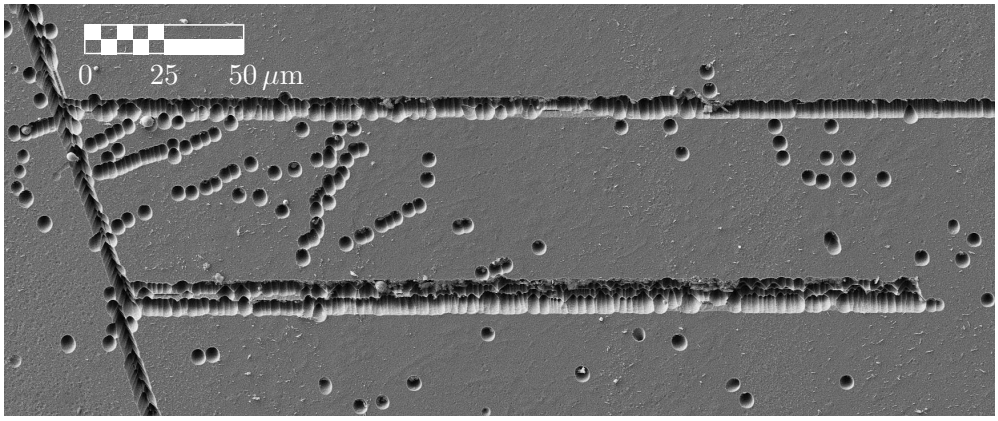


(a) Ungettered wafer side (b) Gettered wafer side

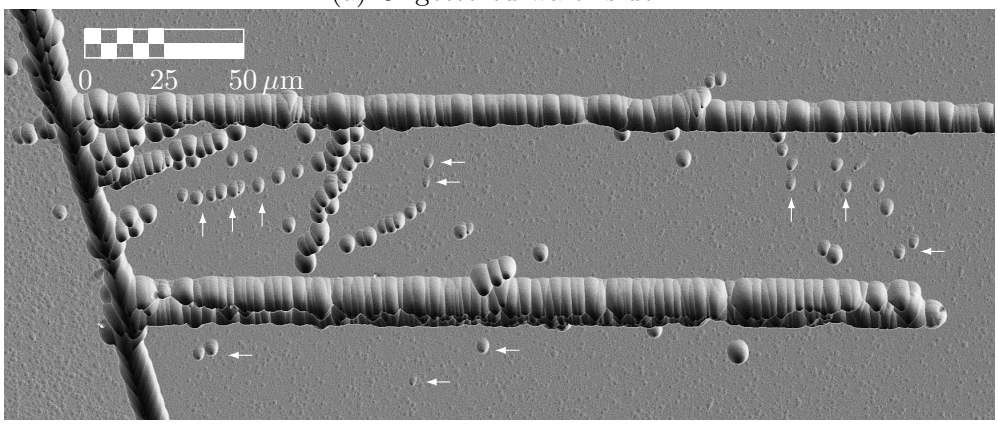
Figure 5.15.: SEM image depicting the same etch pit cluster as it appears on the gettered and ungettered wafer side of a one-sided gettered wafer. Both, the maximum EPD and the absolute number of etch pits in this cluster-filled grain is slightly higher on the gettered side. In all five cluster regions that have been investigated, no EPD reduction is observed.

the ungettered wafer side. While this phenomenon is observable with the optical microscope, too (i.e. the median etch pit area in the ungettered sample side as depicted in figure 5.10b is 18 pixels whereas the median etch pit area on the gettered side, as depicted in figure 5.10a, is only 8 pixels), it is especially interesting to observe this phenomenon in etch pits that, due to the high correlation in location, are likely to originate from the same dislocation line. For the same reason, the dislocation line is likely to be aligned perpendicularly to the wafer surface, therefore

the angles with with the dislocation intersects with the surface should be similar, too.
This is evidence for a modification in the reaction rate of the defect etch that is caused by the gettering process. This observation complements the observed gradual increase in EPD after gettering, that is observed when prolonging the etch time (section 5.4): Both cases point towards a slower reaction rate after gettering.



(a) Ungettered wafer side



(b) Gettered wafer side

Figure 5.16.: SEM image of both sides of a one-sided gettered wafer after polishing and Secco etch. This region exhibits highly correlated etch pit structures on both wafer sides, that are here interpreted as originating from the same dislocation lines. Most of the etch pits on the gettered side are visibly less deep (some of the most significant examples are marked with arrows). It is noteworthy that the amount of material that is removed by the defect etch is determined by the depth as well as the width of an etch pit (figure 5.27 depicts a cross section of shallow and deep etch pits). While the overall diameter of etch pits is similar (or in some cases even larger) than what is observed on the gettered wafer side, etch pits on the ungettered side are significantly deeper, as indicated by the relative size of the black center of each etch pit. In optical microscope images, the reduced depth is visible as a reduction in the observed etch pit diameter: Over the total wafer area, the median etch pit size on the gettered wafer side is less than half of what is observed on the ungettered side.

5.8. EPD reduction as function of distance to the doping glass

One-sided gettering leading to one-sided EPD reduction naturally leads to the question how the EPD is behaving in between the two wafer sides. EPD reduction as function of distance to the doping glass is studied by two methods:

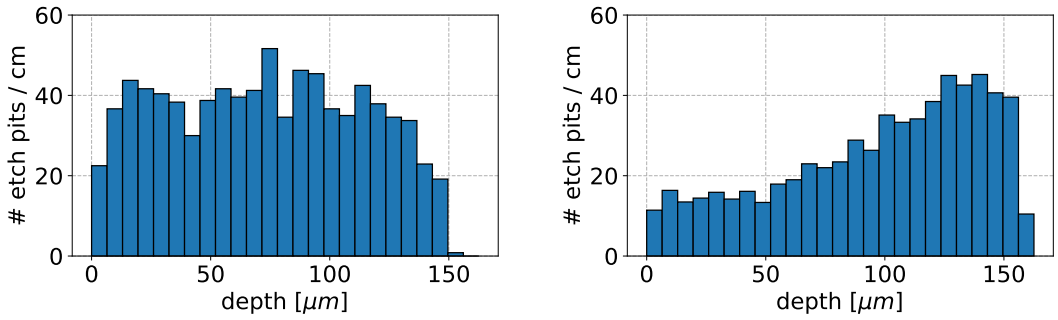
1. EPD analysis on a wafer's edge (direct measurement of EPD as function of depth)
2. APCVD PSG deposition on already polished wafer surface (direct measurement at distance of zero)

The following two sections address these two approaches.

5.8.1. The depth profile of EPD reduction: analysing the wafer edge after one-sided gettering

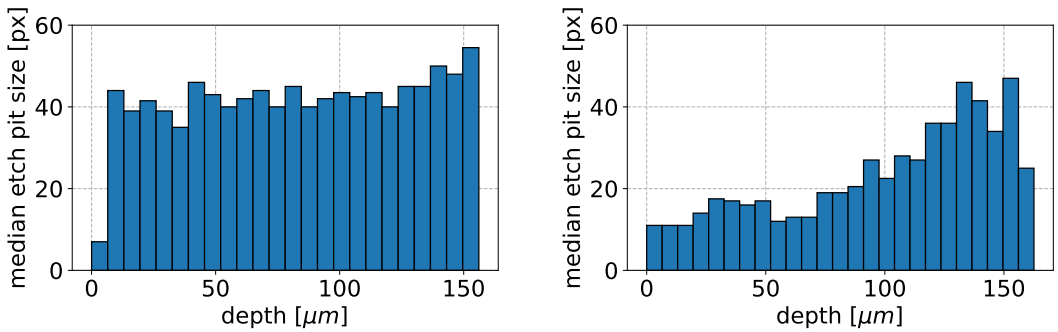
EPD reduction as function of depth can be measured directly by analysis of the EPD on the wafer edge, perpendicular to the gettering sink. While the wafer edge is less than 1.5 % of the wafer surface area, the total analysis area can be increased by using multiple sister wafers so that a reasonable statistical sample of etch pits is obtained.
Here, the depth profile of as-grown wafer edges is compared to results after one-sided gettering. In total, a set of five sister wafers, one as-grown and four gettered wafers, is used. Histograms that show the number of etch pits in bins of increasing distance from the gettering sink along a 2.5 cm long wafer edge show a distribution that is compatible with a constant value throughout the wafer depth for the as-grown case (figure 5.17). The outermost bins of the as-grown distribution are systematically lower, because the wafer thickness along the edge is reducing towards one end of the wafer - a typical consequence of wet chemical polishing where wafer regions close to the carrier are etched faster. All gettered wafers individually show a decrease in etch pit density towards the side of the gettering sink. Combining the data of four gettered sister samples results in a distribution that shows a constant EPD in a 0 µm to 50 µm distance from the gettering sink, beyond which the EPD increases to the ungettered wafer side (figure 5.17b). This observation of constant EPD reduction close to the gettering sink fits nicely with the EPD measurements on the wafer surface, where no variation due to the natural variances of the polishing process have been found. The trend of increasing EPD is accompanied by a similar increase in the median etch pit size (figure 5.18). Both, increases in the number as well as in the size of etch pits towards the ungettered wafer side, can be spotted in the raw image data (figure 5.19).
Edges were polished through the same regions of the same grains on all five sisters wafers. The wafer edges that contribute to the data shown in figures 5.17 and

5.18 do not contain etch pit clusters. Some parts of the wafer edge are stained



(a) As-grown (b) Combined gettered data

Figure 5.17.: The number of etch pits per unit length on the wafer edge as function of distance from the gettering sink. The as-grown wafer (a) has a constant depth profile, whereas the combined data of four samples after one-sided gettering (b) show less etch pits near the gettering sink. The edge was polished through the same grains on all five sisters wafers. The bin width for both histograms has been chosen by applying Knuth's rule [80] to the combined data of the gettered wafers.



(a) As-grown (b) Combined gettered data

Figure 5.18.: The median size of etch pits as measured on the wafer edge as function of depth for the as-grown (a) and the combined data of gettered wafers (b). Etch pits reduce in size when they are located closer to the gettering sink. The bin width in both histograms is kept similar to figure 5.17.

or scratched and must be ignored in the analysis, therefore the histogram bins in figure 5.17 are weighted by the total length of the wafer edge that entered the analysis, resulting in a bin height with the dimension $\frac{\text{number of etch pits}}{\text{unit length}}$. The bin height multiplied by the bin width results in a mean EPD value for that slice of the wafer edge that corresponds to the bin. Ignoring the rightmost bin, the mean bin

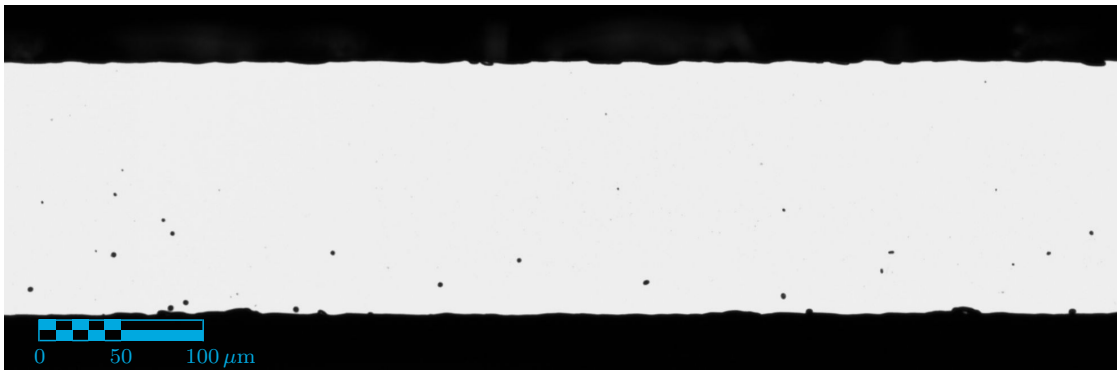


Figure 5.19.: Raw optical microscope image, depicting a section of a polished and Secco-etched wafer edge after one-sided gettering. The gettered wafer side is at the top of the image. It can be seen that etch pits tend to be higher in number and in size towards the bottom side of the wafer edge, i.e. with higher distance from the gettering sink.

height of the last six bins in figure 5.17b, corresponding to an assumed constant EPD on the ungettered wafer side, is $\bar{n}_{\text{max 6, gettered}} = (41.6 \pm 2.6)\text{cm}^{-1}$. Ignoring the first and the last three bins of the as-grown data, which are affected by described change in wafer thickness, the mean bin height is $\bar{n}_{\text{ag}} = (38.7 \pm 5.9)\text{cm}^{-1}$. The difference is $\bar{n}_{\text{max 6, gettered}} - \bar{n}_{\text{ag}} = 2.9 \pm 6.4$, compatible with zero, i.e. the observed EPD close to the ungettered side of the wafer edge and on the as-grown wafer edge is the same.

Assuming that EPD reduction is caused by out-diffusion of metallic impurities, a naive assumption about the depth profile of the number of etch pits as a function of the distance from the gettering sink could be a direct proportionality between the concentration gradient of metallic impurities and the number of etch pits. The concentration of metallic impurities can be easily calculated with Fick's second law of diffusion, assuming a gettering sink of constant impurity concentration throughout the gettering process located at a depth of 0 µm. In this case, the impurity concentration takes the shape of the complementary error function, i.e. a concave function for increasing distance from the gettering sink. Simulations of comparable systems also result in concave impurity profiles [81]. The naive assumption that the number of etch pits is directly proportional to the impurity concentration is not compatible with the observed convex depth profile of the number of etch pits as function of distance from the gettering sink (figure 5.17b). Subscribing to the view that EPD reduction is caused by the inability of the defect etch to enter a reaction with impurity lean dislocations, this observation suggests a highly non-linear behavior of reaction rate and the impurity concentration at dislocations.
The observed depth profile shows significant EPD reduction at depths of more than 100 µm (figure 5.17). The diffusivity of P and O in silicon as well as the diffusivity of silicon self interstitials is much too small for these substances to traverse this distance [82]. Ordinary diffusion of P, O or silicon self interstitials as cause for

EPD reduction can thus be ruled out.
The literature discusses enhanced diffusivity along dislocation lines (pipe diffusion) [20] which could cause these species to reach much deeper into the wafer than ordinary diffusion would allow. Further evidence against the notion that EPD reduction is caused by the presence of P, O or silicon self interstitials, as well as evidence against pipe diffusion in particular, can be made with the experiment presented in the following section.

Analysing the various sample edges that have been prepared over the course of this work, it has been found that absolute EPD values on the wafer edge are comparable to what is measured on the wafer surface (figure 5.20), i.e. etch pit clustering after defect etch can happen on the wafer edge similarly as on the surface. This is evidence that dislocations lines are likely strongly curved in the material that is studied here. Subscribing to the view that EPD reduction is caused by the presence of P, O or silicon self interstitials facilitated by enhanced pipe diffusion, at this point it can not be ruled out whether the observed absence of EPD reduction in dislocation clusters is the consequence of strong dislocation curvature in these regions: When the mean curvature radius in clusters is very small compared to the pipe diffusion length, it could be the case that such dislocations - despite great length - do not reach far into the wafer and consequently, dislocation segments that are affected by pipe diffusion could be removed by polishing.
This possibility, too, can be falsified by the experiment presented in the following section.

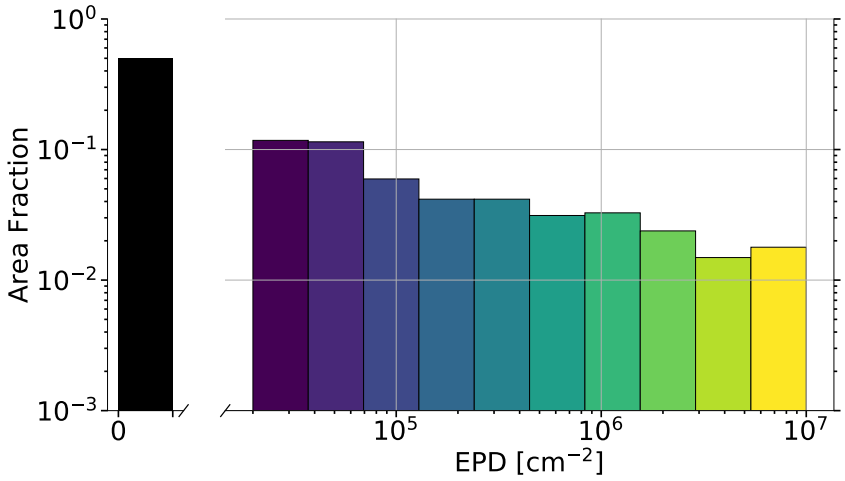


Figure 5.20.: As-grown EPD values and their frequency as measured on the wafer edge. Absolute EPD values are similar as measured on the wafer surface.

5.8.2. EPD after PSG diffusion on polished surface

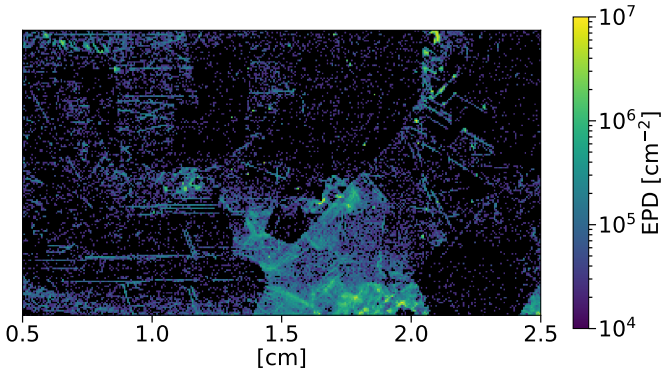
A simple method to check whether P, O or silicon self interstitials are causing EPD reduction is to execute a gettering process directly on the polished surface on which the EPD is measured. No material has to be removed between gettering and the EPD analysis, therefore it is certain that enhanced quantities of P, O and silicon self interstitials are present in the crystal region that reacts with the defect etch. This applies to regions of low and mid EPD as well as to regions containing etch pit clusters, hence EPD reduction in all of these regions must be expected if EPD reduction is caused by in-diffusion, regardless of the curvature of dislocations.

Consequently a sample that was polished first, and only then an APCVD PSG was deposited on the polished surface, was subjected to a high temperature step facilitating a diffusion gettering process. A polished sister sample without doping glass has been processed as temperature reference in the very same fashion and an additional sister sample has been prepared to provide the as-grown EPD reference. This high temperature step, here, is executed in a rapid thermal processing (RTP) furnace. The use of an RTP furnace instead of a typical quartz tube diffusion furnace is required here, since the mechanical polishing process releases finely dispersed iron that would contaminate the environment of the quartz tube diffusion furnace. Unlike the quartz tube diffusion furnace, this RTP furnace has been routinely used for processing of metallized samples of various kind.
The total time in the RTP furnace amounts to 154 min of treatment in nitrogen atmosphere and consists of 30 min ramp up from 620 °C to a peak of 840 °C, held for about 75 min, followed by a ramp down to 620 °C over the course of 50 min. These process times replicate the APCVD P diffusion processes used in this work (figure 4.1). Before defect etching, the PSG is removed from the polished surface with diluted HF.

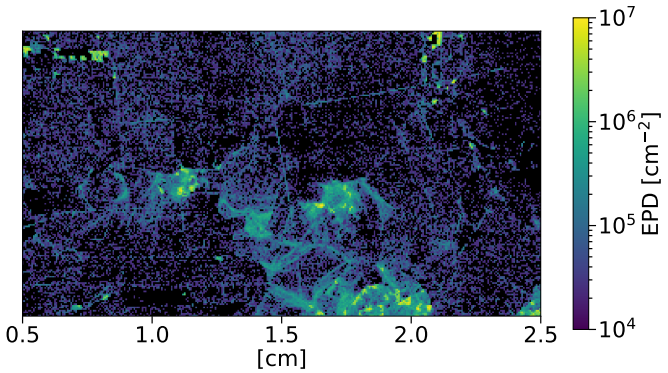
Gettering directly on the polished surface results in EPD reduction after Secco etch when compared to the as-grown reference. EPD reduction mainly occurs in regions where the as-grown reference features low EPD (figure 5.21a). Yet, the intensity of the EPD reduction effect is significantly less than what has been observed for samples that are polished after the diffusion gettering processes. Gettering on the polished surface directly maximizes the concentrations of atomic species like P, O or by silicon self interstitials at the site of EPD measurement, consequently the idea that the presence of these atomic species is causing EPD reduction must be rejected.

Surprisingly, the gettered sample features regions of mid EPD that are pronounced stronger when compared to the as-grown state. Explanations for both observations, the stronger pronounced mid EPD regions and the reduced effect of EPD reduction can be inferred from a comparison of the as-grown reference and the temperature reference: The temperature reference that was treated in the RTP furnace shows significant increase in EPD for mid and low EPD regions (figure 5.21c). The increase in EPD is systematically different for individual grains, which strongly suggests that the observed effect is coupled with the crystal's interior state and is not caused by

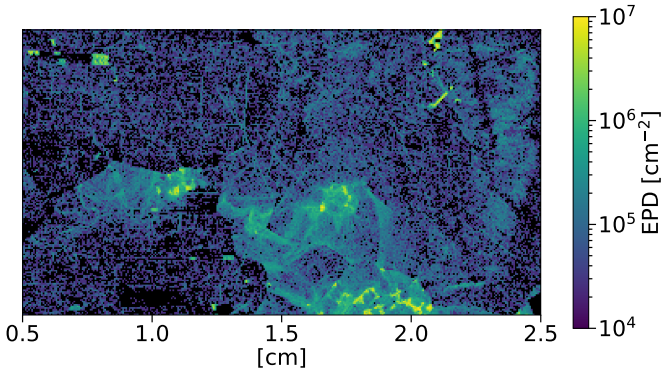
modifications of the polished surface during the RTP treatment. Pairs of as-grown and temperature reference samples that have experienced the same thermal history, but in the clean environment of a diffusion furnace, have never shown changes in EPD (section 4.2.2). Therefore, the observed difference is interpreted as the result of contamination with metallic impurities: Dislocations that have previously been lean in certain species of impurities were decorated with impurities during the RTP process and therefore can be revealed by the defect etch. The result of reduced EPD reduction intensity of the RTP gettered sample can be understood with the same line of thought: The presence of metallic impurities, introduced by processing in the contaminated environment of the RTP furnace, is countering EPD reduction.



(a) APCVD PSG + RTP diffusion



(b) As-grown

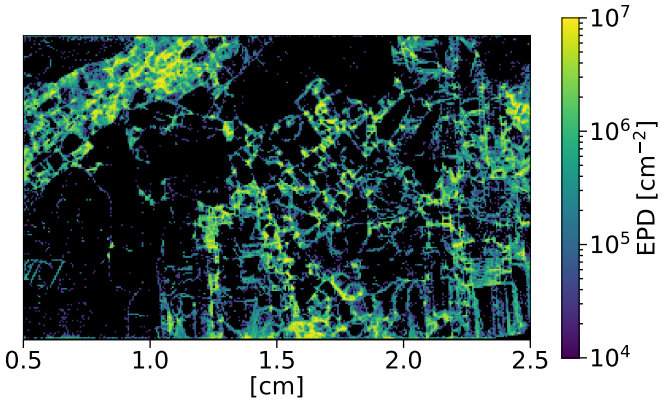


(c) RTP temperature reference

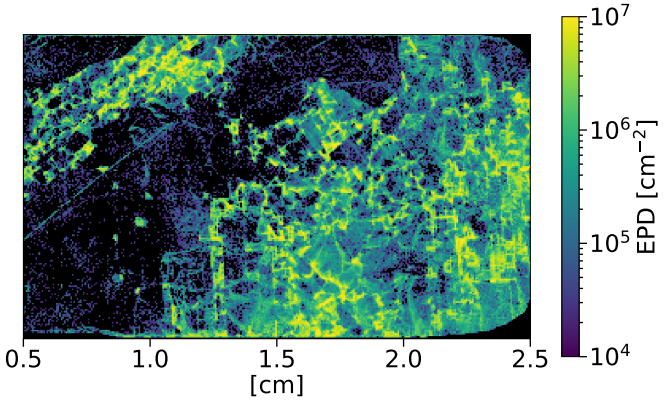
Figure 5.21.: Set of EPD measurements showing the effect of gettering directly on the polished surface (a) with as-grown (b) and RTP temperature reference (c). EPD reduction is present but with less intensity when compared to diffusion furnace gettering and subsequent polishing. The temperature reference sample shows a grain-dependent increase over the as-grown EPD. An interpretation of these results is given in the text.

5.9. Reversing EPD reduction

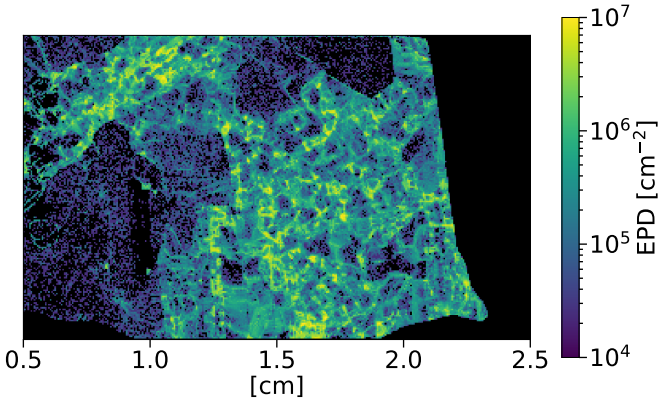
It has been shown that a high temperature step similar in duration and temperature budget to a typical diffusion process, carried out in a metal containing environment, can lead to an increase in EPD compared to the as-grown state (section 5.8.2). Because similar high temperature steps in a clean environment do not affect the EPD (section 4.2.2), the increase in EPD is interpreted as the effect of contamination with metallic impurities. From the literature it is known that high temperature processing can cause measurable increases in metal concentrations of high purity silicon material: Even in a clean environment, furnace treatment alone can cause an order of magnitude increase in $[Fe_i]$ contamination in high purity float zone silicon [69].
Further evidence to restrict the mechanism of EPD reduction has been obtained by repeating this contamination procedure on gettered material: An already gettered sample, exhibiting EPD reduction, has been polished and subsequently treated in the RTP furnace, using the same processing parameters as described in the previous section. Compared to a similarly gettered sister sample (figure 5.22a), the gettered sample after processing in the RTP furnace shows an increase in EPD (figure 5.22b): After RTP treatment, the EPD reverts back and even surpasses the EPD observed in mid EPD regions of the as-grown reference (figure 5.22c). Low EPD regions show an increase in EPD, too, but do not revert back to the as-grown state. It is especially remarkable that EPD reduction reversal seems to lead back to a similar spatial EPD distribution as is measured on the as-grown sister sample: Regions that revert to mid-EPD levels appear with mid-EPD in the as-grown sister. Likewise behavior, i.e. a seemingly persisting memory of each regions as-grown EPD throughout the process of EPD reduction and EPD reduction reversal (EPD memory), is observed for low-EPD regions.
If it is assumed that mobile dislocations and annihilation of dislocation pairs with opposite Burgers vectors are causing EPD reduction, it follows that the RTP furnace process has created new dislocations - a highly problematic proposition. Moreover, this view requires an additional mechanism that favors the creation of dislocations in mid EPD regions over low EPD regions and an additional explanation for why these regions are distributed similarly to what is observed in the as-grown sister (EPD memory).
A simpler and more fitting interpretation of these observations is, again, that only the etch pits disappear while the dislocations remain in the material. Especially the observation that contamination tends to recreate the spatial EPD distribution, as it has been before EPD reduction, strongly favors explanations that leave the actual dislocation distribution unchanged: EPD reduction does not remove dislocations from the material. Rather, dislocations are still present but hidden after gettering. The RTP furnace treatment is interpreted to cause decoration of dislocation sites with metallic impurities such that more dislocations are revealed by the defect etching process.



(a) Gettered reference



(b) Gettered and contaminated sister sample



(c) As-grown reference

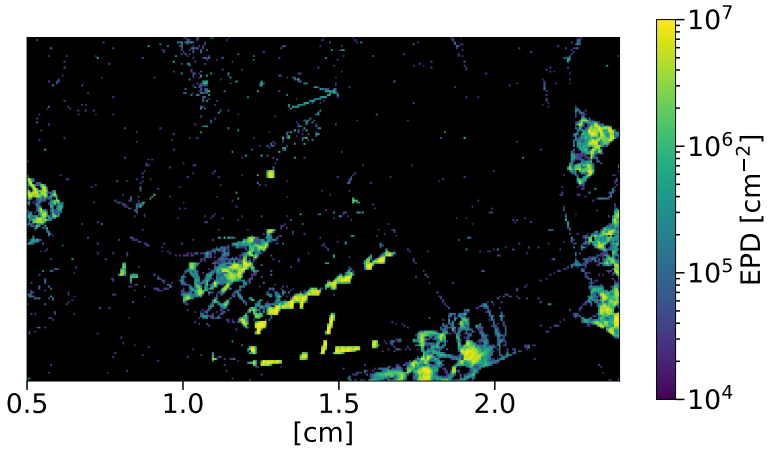
Figure 5.22.: EPD map of a gettered sample, featuring EPD reduction (a) and a gettered sister wafer after contamination (b). The gettered and subsequently contaminated wafer shows less EPD reduction compared to the gettered sample. This demonstration that EPD reduction can be reversed by contamination is strong evidence against the notion that dislocations are removed from the crystal. In low EPD regions, the as-grown reference (c) exhibits higher EPD than the contaminated sample whereas mid EPD regions are at least equally pronounced in the contaminated sample.

Unlike the results presented in figure 5.21, the experiment shown here (figure 5.22) includes a second high temperature diffusion step taking place after the gettering step. The picture of EPD reduction reversal is completed by studying the influence of this second high temperature step.

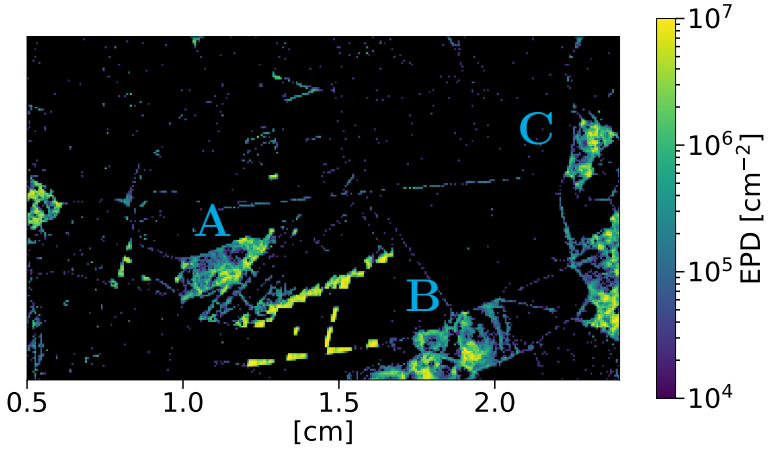
5.9.1. Cross-check for temperature load

A systematic difference between the previously studied gettered sample that has been contaminated in the RTP furnace and other gettered samples studied so far, lies in the temperature budget: The contaminated sample has been subjected to the temperature profile of the diffusion step two times - one time during gettering and a second time for the contamination process. Here, a cross-check is presented, where the additional second high temperature step is replicated in the clean environment of the diffusion furnace.
Sister wafers after one-sided gettering are used for comparison. Two of those wafers are subjected to the additional high temperature step. For one of these two wafers, the emitter is chemically removed before the high temperature step, for the other wafer, the emitter is kept. A third wafer is used as reference without any additional high temperature step.
EPD maps of these three wafers show that EPD results of a second high temperature diffusion step executed in a clean environment (figure 5.23) are different from the RTP results (figure 5.22): Unlike for the previously discussed RTP process, no reversal of EPD reduction is observed in regions that exhibit zero EPD after gettering. This is interpreted as evidence for contamination with metallic impurities during the RTP furnace process. However, significant regions of mid EPD are appearing on the gettered material after this second high temperature step in a clean environment (marked as A, B and C in figure 5.23b). The sample that was processed in the RTP furnace (figure 5.22) contains a high fraction of such mid-EPD regions and it is likely that EPD reduction reversal in these mid EPD regions can be attributed to the temperature influence. The given interpretation does, however, not change regardless whether contamination is due to an internal re-distribution or due to impurity contamination from the furnace environment. The characteristics of EPD reduction that have been inferred, rely on the observation that EPD reduction is a reversible process.

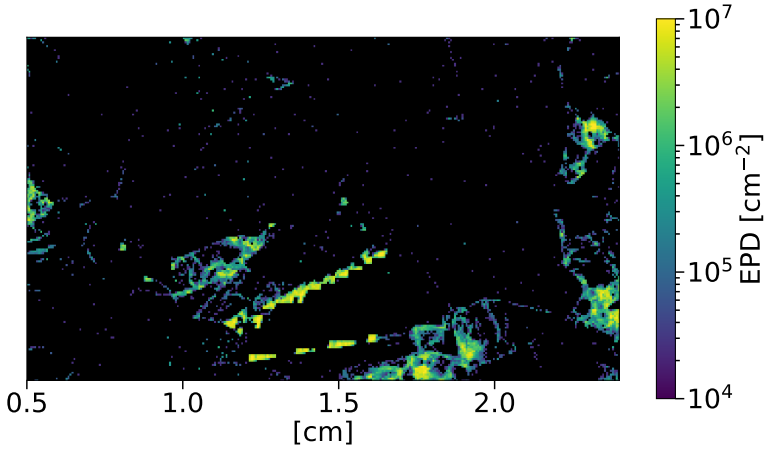
An additional view into the influence that a second high temperature step has on the presence of etch pits, is obtained by measuring the EPD depth profile on the wafer edge. For this purpose, four samples have been cut from the same wafer from which the sample depicted in figure 5.23a originated from, i.e. a one-sided gettered wafer, that has experienced a second high temperature step without removal of the highly n-doped emitter region. Etch pit information from these wafer edges is compared with EPD results from the wafer edge presented in section 5.8.1 that is comparable in block height and position and, likewise, has not been subjected to an emitter removal.



(a) Gettered + T



(b) Gettered + emitter removal + T



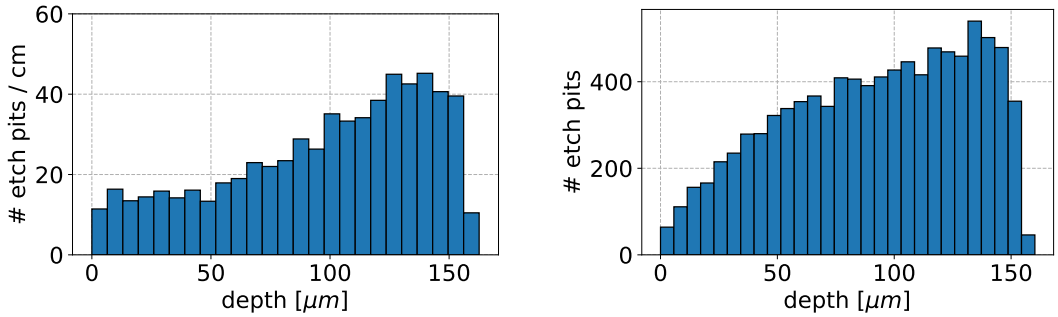
(c) Gettered

Figure 5.23.: EPD of sister wafers gettered on one side with (a, b) and without (c) a second high temperature step. Unlike for the RTP process, no reversal of EPD reduction is observed in regions that exhibit zero EPD after gettering. The additional high temperature step leads to an increase in mid EPD regions (marked A, B and C in figure b).

A comparison of the frequency distribution of etch pits as function of depth shows that the convex profile observed on one-sided gettered material changes to a concave profile after an additional high temperature step (figure 5.24). The convex profile observed after one-sided gettering (figure 5.24a) shows the effect of EPD reduction, as has been discussed in section 5.8.1. The changed profile in the etch pit frequency distribution as function of depth is indicative of a reversal of EPD reduction.
Such a reversal can be explained in two ways: 1. Subscribing to the picture that EPD reduction is explained as annihilation of dislocations, re-appearing etch pits must be interpreted as the creation of new dislocations. There is neither evidence nor mechanisms discussed in the literature that would support this interpretation. 2. Subscribing to the picture that EPD reduction is explained as the inability of the defect etch solution to react with dislocations under certain conditions, such as the decoration state of dislocations with metallic impurities, re-appearing etch pits can be explained as a reversal of the dislocation's impurity decoration. In this case, re-appearing etch pits can simply be interpreted as internal re-distribution of impurities from the ungettered wafer back-side.
Since non-sister wafer data has been used for figure 5.24b, a comparison of EPD values is not meaningful. In both cases depicted in figure 5.24, the median etch pit size as function of wafer depth is highly correlated to the etch pit frequency distribution (figure 5.25), i.e. the change that the additional temperature step introduces to the frequency distribution is reflected in the distribution of etch pit size, too. This indicates that EPD reduction and the reversal of this process are governed by the same mechanism. A qualitatively similar reduction has been observed on the front and back side of a one-sided gettered sample (section 5.7.3.

5.9.2. Etch pit shape after contamination

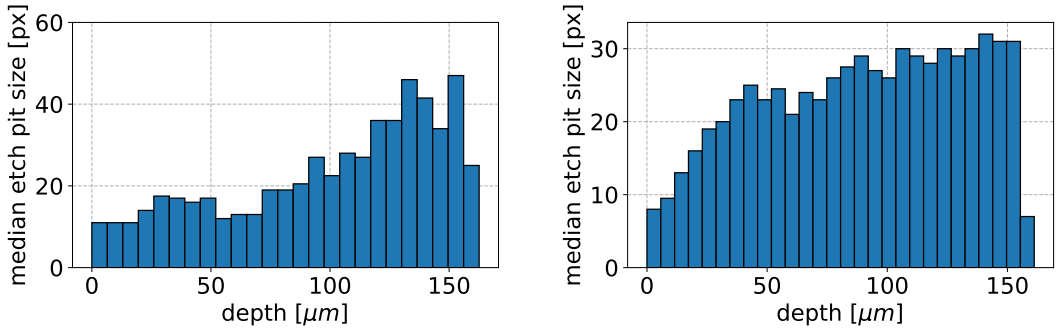
SEM scans of areas in which the EPD of the RTP contaminated sample (figure 5.22b) has increased, show two types of etch pits (figure 5.26). Using focused ion beam (FIB) milling, cross sections of these two types of etch pits have been analysed, confirming that the two types of etch pits differ in depth by about a factor of 4 to 5 (figure 5.27). Etch pits that exhibit a comparably reduced depth have been observed after P-gettering (section 5.7.3). Both kinds of etch pits, deep and shallow, contribute to the observed increase in EPD.



(a) One-sided gettering

(b) One-sided gettering + second high temperature step

Figure 5.24.: The number of etch pits on the wafer edge as function of distance from wafer surface after one-sided gettering, depicted with and without the additional second high temperature step that is affecting the RTP contaminated samples. The convex profile in the etch pit frequency distribution after gettering (5.24a) changes to a concave profile with the additional temperature step (5.24b). This is a second, independent experiment, demonstrating that EPD reduction can be reversed. Interestingly, the median etch pit size shows a highly correlated behavior for the two compared sample sets (figure 5.25). The bin width for each histogram has been chosen by applying Knuth's rule [80] to the corresponding data sets.



(a) One-sided gettering

(b) One-sided gettering + second high temperature step

Figure 5.25.: The median etch pit size as function of distance from the gettering sink for one-sided gettered wafers, with and without the additional second high temperature step that is affecting the RTP contaminated samples. A strong correlation between median etch pit size and the number of etch pits is observed, indicating that the mechanism responsible for changes in the EPD is the same in both displayed cases.

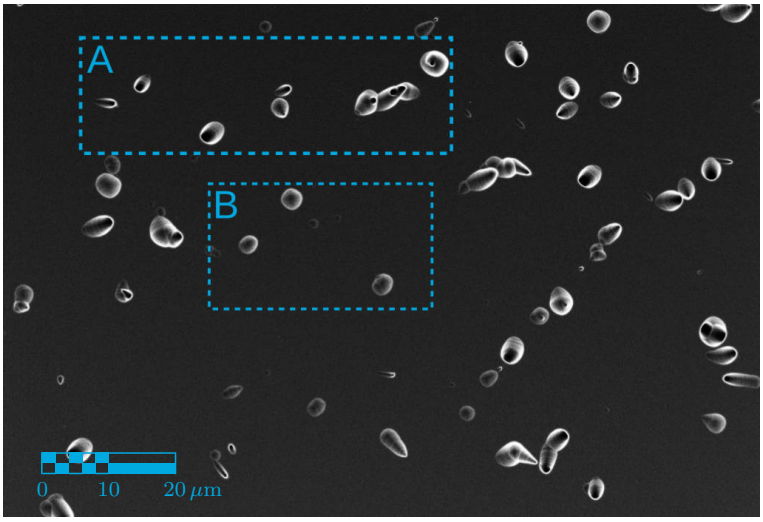


Figure 5.26.: SEM in-lens detector image of Secco etch pits in a region that has shown an increase in EPD after RTP furnace treatment. While the region marked A contains etch pits typical of a Secco etch, the etch pits in region marked B have a comparatively stronger SEM signal in the center. Cross sections of etch pits from these regions show that etch pits similar to those in region A are 4 to 5 times deeper than those in region B (figure 5.27).

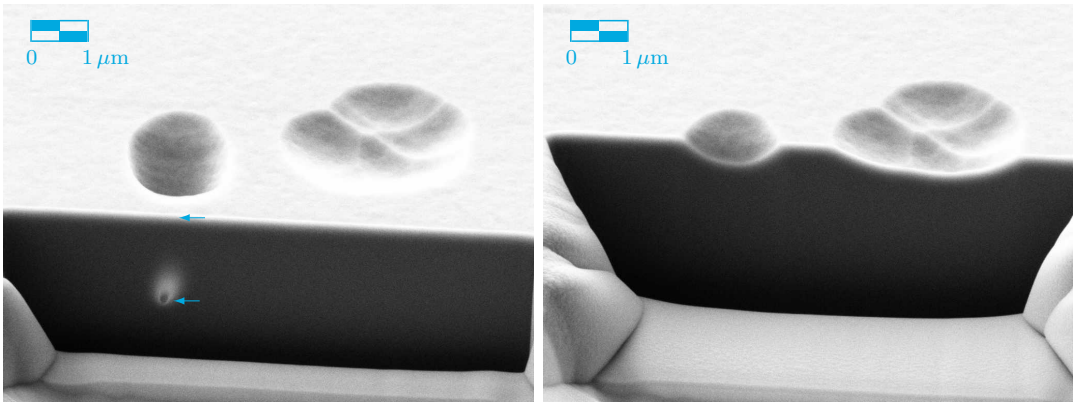


Figure 5.27.: SEM images after FIB milling through a normal and a shallow etch pit after Secco etch, located close to the region depicted in figure 5.26. From the relative distance from the milling edge to the lowest point of the etch pit (marked with arrows for the deep etch pit), the relative depth of these types of etch pits can be measured. Due to tilting of the sample during recording, the scale bar only applies in horizontal direction.

5.10. Repeatability of contamination experiments

Considerable effort has been made to isolate the influence of the RTP treatment that leads to the observed increases in EPD. Several attempts have been made

to recreate the results that are interpreted as consequences of contamination in the RTP furnace (section 5.8.2 and 5.9). The successful contamination events have taken place within a short period of time. Right before this time, the RTP furnace has been repeatedly used with molybdenum containing substrates, therefore contamination procedures with this element, as well as iron, and tungsten have been executed in various ways. Only two of these experiments have succeeded in reversing the effect of EPD reduction, but not without ambiguity:
Wafers that can be interpreted as successful repetition of the contamination experiments have experienced 195 min at 840 °C instead of the 90 min that have been used before. The surface of one of these wafers has been heavily scratched in the attempt to clean the surface with a short manual fine polishing step. In areas that are less affected by scratching, increased EPD in comparison to a reference sample has been recorded. Repeating the full polishing procedure has resulted in an increase in mid and low EPD regions in some grains. Similarly as observed in sections 5.8.2 and 5.9, changes in EPD are systematic to certain grains. It must be noted that the second polishing step that had to be used, results in additional material removal estimated to be $21.0 \pm 5.3\,\mu m$ (section 3.3.1). This, as well as the increased processing time at high temperature likely mean that the observed reversal of EPD reduction is at least partly due to the described internal re-distribution of impurities (section 5.9.1). A second sample that has been identically processed, except for the manual cleaning step and subsequent second polishing step, is affected by more than the usual amount of scratching, too. Results show an increase of etch pits in low EPD regions, yet, mid-EPD regions seem hardly affected by the contamination process.

While the unambiguous identification of a repeatable contamination process would be useful for further experiments, the chain of arguments required for a decision between the various discussed mechanisms for EPD reduction is sufficiently supported by the observation that EPD reduction is reversible. Whether this reversion is caused by external contamination or by the high temperature step and a re-distribution of internal contaminants has no influence on the significance of the evidence in this context.

5.11. EPD reduction without net impurity flux

Especially interesting results involving EPD reduction have been reported in combination with copper contamination [19]. The experimental setup in this publication includes samples that feature a gettering sink on one side and a copper layer on the opposite wafer side, such that the net impurity flux between copper layer and gettering sink is maximized. It has been found that EPD reduction is stronger in the presence of such a copper layer. The authors interpreted EPD reduction as a consequence of annihilating dislocations, the movement of which is driven by a force that the net flux of impurities towards the gettering sink is exerting on the dislocations. The observation of stronger EPD reduction in the presence of the

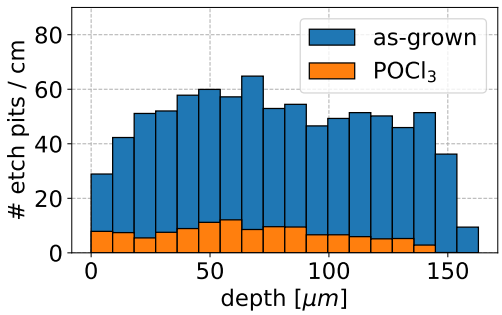


Figure 5.28.: The number of etch pits per unit length as measured on the wafer edge of as-grown and $POCl_3$ gettered samples. Since $POCl_3$ gettering is symmetric to the center plane of the wafer, the net flux of impurities in the wafer center is zero (equal flux towards both wafer sides). The hypothesis that a net impurity flux is causal to EPD reduction, as put forward in [19], would therefore predict an absence of EPD reduction for the center bins of this $POCl_3$ gettered wafer edge. The here depicted measurement falsifies this hypothesis.

copper layer is explained by the increase in net impurity flux due to diffusion from the copper layer towards the gettering sink.
Here, an experiment is presented that suppresses the net flux of impurities, the aspect that is central to the before mentioned interpretation, by measuring the EPD on the wafer edge of a sample that has been gettered symmetrically on both sides, resulting in equal flux towards both wafer surfaces for the center region of the wafer edge (i.e. the region of equal distance from both gettering sinks).
Corresponding wafer edges from a set of six sister samples, two as-grown, and four samples that have experienced five consecutive symmetrical $POCl_3$ gettering steps (material presented in section 5.6) have been analysed for etch pits (figure 5.28). As it was the case in the EPD analysis on the wafer edge above, some parts of the wafer edge are stained or scratched and therefore must be ignored in the analysis. The histogram bins in figure 5.28 are weighted by the total length of the wafer edge that entered the analysis, such that the bin height is of the dimension $\frac{\text{number of etch pits}}{\text{unit length}}$ and is directly proportional to the mean EPD.
The edge's center of the gettered samples has not been exposed to a net impurity flux, yet the bins at the center wafer depth show similar values as bins closer to the wafer surface. If a net impurity flux is causal to EPD reduction, the center bins in the gettered data (figure 5.28) are expected to show an EPD similar to the as-grown state, i.e. EPD reduction in the center bins should be suppressed. However, absolute EPD values (proportional to the bin height) show significant EPD reduction for all regions of the gettered wafer edge with no significant increase towards the center. This observation falsifies the hypothesis that a net flux of impurities and the resulting dislocation motion are causal to EPD reduction.

5.12. Interim conclusion

Candidate mechanisms that explain EPD reduction, as discussed in the beginning of this chapter, are:

1. Annihilation of dislocations, based on mechanisms that enhance dislocation motion at low temperatures
2. Reduction of the defect etch reaction rate in the presence of atomic species introduced during the gettering process, i.e. P, O, or silicon self interstitials
3. Reduction of the defect etch reaction rate, associated with the reduction of a dislocation's decoration with impurities

A gettering process that has been executed directly on the polished surface, maximizing the concentrations of P, O, and silicon self interstitials directly at the surface of EPD measurement has not increased but reduced the intensity of EPD reduction, therefore mechanism 2 is rejected (section 5.8.2). The observed reduction in gettering strength is in accordance with mechanism 1 as well as mechanism 3. However, the observed increase in EPD between a RTP processed temperature reference sample and an as-grown reference (section 5.8.2) would, according to mechanism 1, require a mechanism that creates new dislocations specifically in the (contaminated) environment of the RTP furnace, yet not in the (clean) environment of the diffusion furnace. Mechanism 3, on the other hand, offers a straightforward explanation for these observations.
Variation of the gettering strength, achieved by repeating a certain gettering process multiple times (section 5.6) shows increased EPD reduction for stronger gettering. This is easily understood in terms of mechanism 3, whereas for mechanism 1, every repetition of a gettering step should result in a progressively smaller net flux of impurities compared to the previous gettering step. With every additional gettering step, the force that is hypothesized to move dislocations is diminished, therefore it is hard to understand how those dislocations that survive the first gettering step, are annihilated in later gettering steps, for which the net impurity flux should be less. The specific mechanism for enhancement of dislocation motion that has been suggested in [19] could be falsified by etch pit density measurements on the wafer edge in a symmetric gettering system (section 5.11): By symmetric gettering, the net impurity flux that is hypothesized to cause dislocation motion [19], is suppressed - yet it has been shown that EPD reduction occurs nevertheless. Consequently, instances of mechanism 1 that require asymmetric gettering conditions can be rejected.
Further evidence against mechanism 1 is the observation of one-sided EPD reduction after one-sided gettering. This phenomenon that has been studied on the wafer surface (section 5.7) as well as on the wafer edge (section 5.8.1) is strong evidence against the notion of dislocations becoming mobile during gettering.
The observation that EPD reduction can be reversed is strong evidence against the notion that dislocations are removed from the material during gettering. Of special significance is the observation that regions of both, mid and low EPD, can

be reduced to an EPD of practically zero over extended regions, while the reversal of EPD reduction re-creates defect densities of the as-grown state, seemingly remembering the as-grown EPD (section 5.9). This remembering is understood most easily as the continued existence of dislocations throughout the process of EPD reduction and EPD reduction reversal. EPD reduction reversal has been observed after contamination with metallic impurities at high temperatures (section 5.9) as well as on one-sided gettered wafers when an additional high temperature step is performed after the gettering process(section 5.9.1). The latter effect has been observed on the wafer surface as well as on the wafer edge. A mechanism of EPD reduction that is reversible can hardly be reconciled with the view that EPD reduction is caused by annihilation of dislocations. Mechanism 1 is rejected on the basis of the evidence summarized so far. Mechanism 3, on the other hand, is in agreement with all of the above observations.
This mechanism is also supported by observations that can be interpreted as immediate effects of a reduction of the defect etch reaction rate: A drastic increase in etch time reveals some of the etch pits that have vanished due to EPD reduction (section 5.4). Dislocations that survive EPD reduction have been shown to result in shallower etch pits after the P-gettering step than corresponding etch pits on the opposite, ungettered wafer side (section 5.7.3). Similarly shallow etch pits have been observed after contamination and EPD reduction reversal (section 5.9.2). Finally, a similar increase of etch pit size with increasing distance from the gettering sink is observed on the wafer edge: Etch pits of reduced depth have been shown to appear with smaller size in the optical microscope (section 5.7.3) and a corresponding gradual reduction in etch pit size is observed on the wafer edge of one-sided gettered wafers towards the gettered wafer side (section 5.8.1). For mechanism 3, these observations are an expected consequence of the gradual reduction in the chemical reaction rate with a gradual reduction in impurity concentration.

So far, direct measurements of the EPD with the tool for EPD analysis on mc-Si that has been developed in the context of this thesis (section 3.3.4) have been used to investigate the phenomenon of EPD reduction. The presented evidence points unambiguously towards mechanism 3, i.e. the dislocation geometry remains unchanged during EPD reduction and the phenomenon itself is best explained by an inability of the defect etch to enter a reaction with dislocations whose decoration state with impurities is below a certain level.
In the following sections, experimental evidence for this EPD reduction mechanism is presented, that relies not on EPD measurements but on measurements of the impurity concentration or the immediate effect of the presence of impurities.

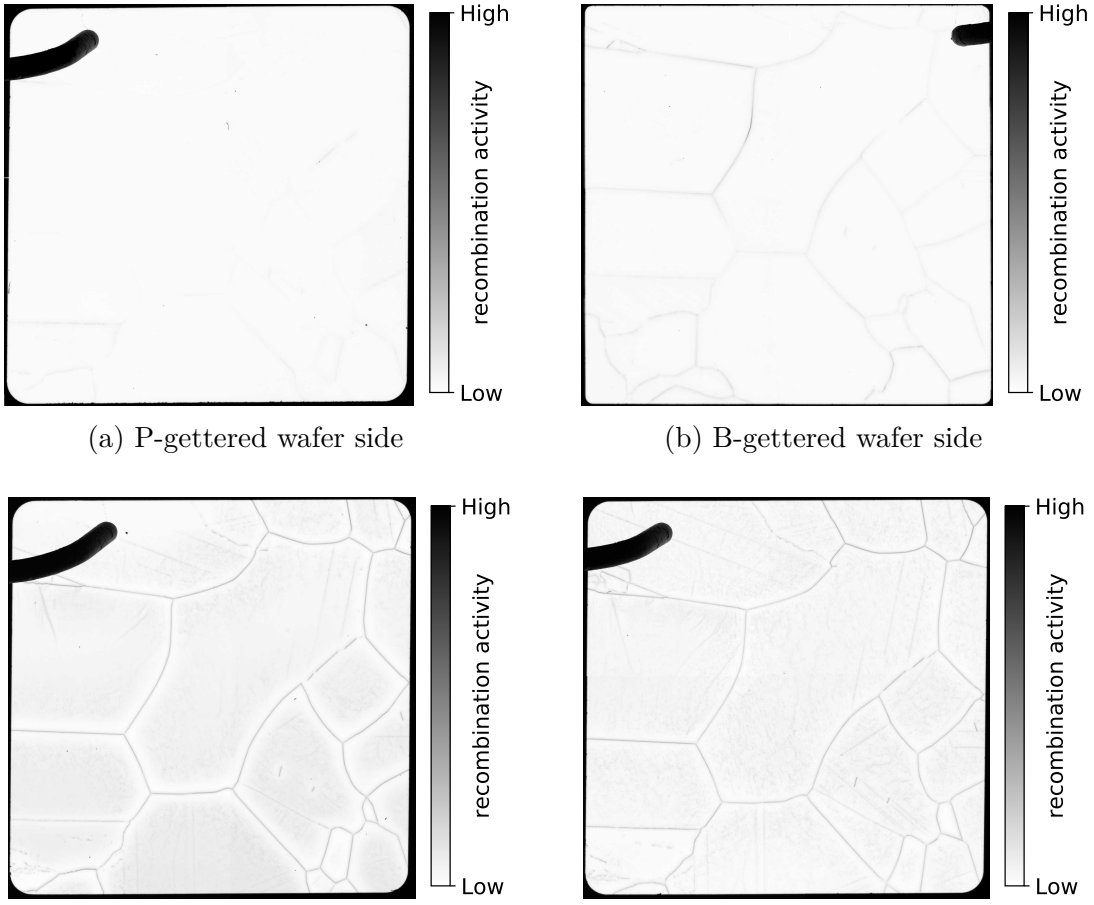
5.13. Surface-close recombination activity of both sides of co-gettered wafers

The view that EPD reduction is caused by impurities influencing the defect etch reaction rate predicts that one-sided gettering must lead to a different concentration of impurities on the gettered and ungettered wafer side. This difference in impurity concentrations could in principle be measured via PL imaging of both sides of a one-sided gettered wafer, since charge carriers are excited in surface-close regions [39]. However, assuming the limit of diffusion lengths that far exceed the wafer thickness, a difference in the PL signal is expected only due to the initial distribution of charge carriers at the moment of photoabsorption. Sufficient diffusion lengths lead to an equal distribution of charge carriers on both wafer sides, thereby reducing the relative signal from the illuminated wafer side. In practice, however, the differences in PL measurements of both wafer sides are dominated by the passivation and anti-reflex coating layer of SiN:H_x. Therefore, as long as no means of passivation is available for which both wafer sides exhibit identical passivation and optical properties, the PL can not be used to resolve these differences.
A better suited method for measuring possible differences in impurity concentration on opposing wafer sides of one-sided gettered wafers is the EBIC technique. EBIC measurements of the recombination activity are strongly biased towards surface-close defects (section 3.4). One-sided P-gettered samples have been prepared to measure this effect. However, at the time of sample preparation the interplay of hydrogen passivation and gettering on the EBIC signal (chapter 4.3) has not been clear and not enough samples have been prepared that feature the combination of gettering, hydrogenation via SiN:H_x deposition and fast firing for which the most significant effects on the EBIC signal have been observed. Therefore, an alternative sample set of co-gettered wafers has been used to study differences in the EBIC signal on both wafer sides.

While co-diffusion conditions are not identical to one-sided P-gettering, it can be argued in several ways why the B-diffused back side is well suited to identify a difference in impurity concentrations on both wafer sides: 1. EPD reduction on co-gettered wafers has been shown to only occur on the P-gettered wafer side (section 5.7.1) 2. The EBIC measurements presented in chapter 4.3 have shown that there is some influence of boron diffusion gettering on the recombination activity, but effects are less pronounced than what is observed after phosphorous-based diffusion gettering. Therefore, differences in impurity concentrations on both wafer sides are expected for one-sided P gettered samples as well as for samples of this co-gettering process. The difference on co-gettered samples is expected to be smaller than for an untreated sample back side, so this experiment is a conservative test. Yet, the observation of one-sided EPD reduction on co-gettered wafers, together with the here presented interpretation, suggests that the specific impurity responsible for the formation of etch pits is still present after boron diffusion gettering. EBIC results of chapter 4.3 have used the same BSG and the same diffusion process as is used for the co-diffusion samples that are presented here. 3. Any direct influence

of boron atoms can be excluded, as for all lifetime samples prepared here, 10 µm of surface material is removed after the diffusion step, far exceeding the diffusion range of B and P doping atoms in the silicon bulk.

Similar to the results presented in chapter 4.3, the EBIC measurement of the B-gettered wafer surface exhibits a recombination activity that lies in between the P-gettered and as-grown state (figure 5.29). Note, that the aluminum pad on the B-gettered sample (figure 5.29b) has sharper corners and is 9 mm wide, compared to 8.5 mm for the other measurements. These changes were made due to an exchange of the existing thermal evaporation machine for a new device. EBIC measurement results from front and back side of the co-gettered and hydrogenated ($SiN:H_x$ deposition and subsequent fast firing) sample show a reduction of the recombination activity on the P-gettered side that exceeds that of the B-gettered side (figure 5.29). This demonstrates a difference in impurity concentrations on the two wafer sides and is evidence in accordance with the interpretation that EPD reduction is due to a suppression of the defect etch reaction rate on impurity-lean dislocations.



(a) P-gettered wafer side

(b) B-gettered wafer side

(c) As-grown

(d) Temperature reference

Figure 5.29.: EBIC measurements of front and back side of two separate co-gettered sister samples (a and b). Additionally displayed is a sister sample in the as-grown state (c) as well as a reference sample that was exposed to the temperature load of the co-gettering process (d). All samples have been hydrogenated by SiN:H_x deposition and fast firing. The dark structure in the top left corner (top right for figure (b), because the image has been flipped) is the tip of the EBIC current probe. On the P-gettered wafer side most structures of enhanced recombination have vanished completely, when compared to the temperature reference sample, while the B-gettered wafer side has retained significantly more recombination active structures. This indicates a difference in impurity concentration on both wafer surfaces, as is predicted by the mechanism of EPD reduction (section 5.12). The measured areas are about 8.5 mm wide, except for image (b) that shows a slightly larger region (9.0 mm width) with differently shaped edges, as is explained in the text.

5.14. Impurity concentration measurements via synchrotron radiation x-ray fluorescence

X-ray fluorescence (XRF) measurements using synchrotron radiation from the MAX IV synchrotron via the NanoMAX beamline have been used to investigate, whether one-sided gettered samples exhibit different concentrations of certain impurities on opposing wafer sides. Additionally it has been studied, whether higher impurity concentrations can be found for any impurity species close to etch pit sites. Synchrotron-based XRF measurements have proven to be a useful tool for analysing impurity contents in silicon materials [83] [84] [85] [86]. The measurements presented in this section have been performed by Markus Rinio, which is gratefully acknowledged.

For this study, the sample depicted in figure 5.10 has been used, a sample that has been polished and Secco etched on both wafer sides. In addition, the sample that has been contaminated in the RTP process (figure 5.22b) is analysed in the hope to identify contaminating elements. Polished and Secco-etched samples like these have been used for this study, since the etch structures allow to identify regions of interest and to find corresponding regions on the opposing wafer sides. Samples have been cleaned two times using a Piranha solution and a subsequent HF dip before packaging and shipping to the beamline.

A monochromatic beam of 14 keV primary photons and a full-width-half-maximum (FWHM) diameter of about 90 nm is used to remove electrons from the innermost orbitals of atoms in the sample. Measuring the characteristic energy of the secondary photons that are released when these electron states are re-populated (figure 5.30) allows for identification and, after calibration and background subtraction, quantification of the amount of a certain atomic species that is present in the sample [87]. Significant peaks in the XRF spectrum have been labeled with the corresponding element names in figure 5.30. Unfortunately, the L lines of molybdenum, which has been speculated to be responsible for the observed increase in EPD after RTP contamination, are located in the range of 2.52 keV to 2.87 keV, at the same position as the dominant argon K line.
The one-sided gettered sample presented in section 5.7 has been used to make a comparison of impurity concentrations on both wafer sides. By changing the position of the sample relative to the primary beam, an energy spectrum can be recorded for various positions on the sample surface. The resulting matrix of XRF spectra can be reduced to spatial maps of element concentrations. For scanning large regions, the sample has been moved out of the focus position of the primary beam such that the FWHM diameter of the primary beam is increased to about 1 µm. The step width between each pixel is set to 1 µm, too. Such maps of the silicon K_α channel reveal structural properties of the surface and are therefore useful for orientation on the sample surface (figure 5.31).

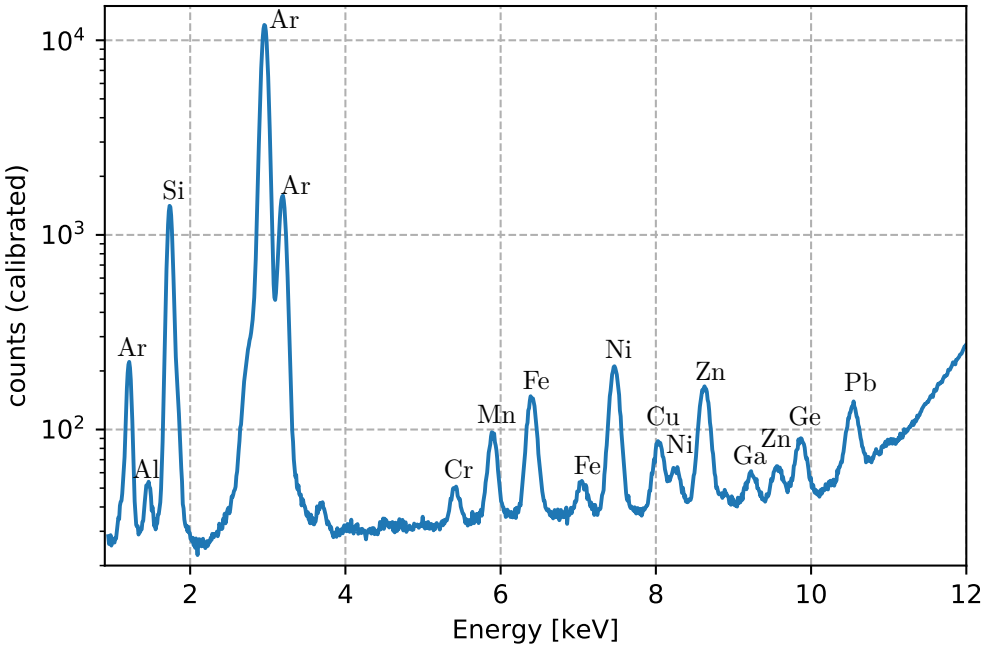
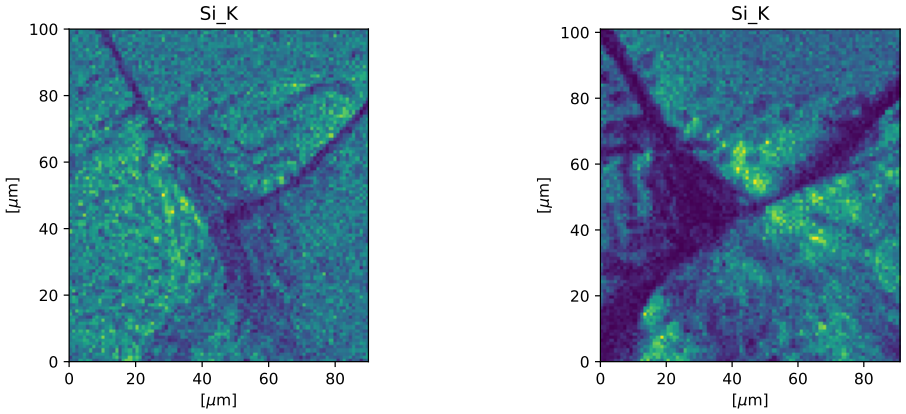


Figure 5.30.: Exemplary x-ray fluorescence spectrum measured on the ungettered side of the sample. Measurements and background correction executed by Markus Rinio.



(a) ungettered wafer side (b) gettered wafer side

Figure 5.31.: X-ray fluorescence maps of the silicon K_α channel (arbitrary units) reveal the surface structure of Secco etched grain boundaries and etch pits. The two images show corresponding regions on the opposing wafer sides on which the measurements depicted in figure 5.32 and 5.33 have been taken. Measurements and background correction executed by Markus Rinio.

Concentration maps of Zn, Mn, Cu and Fe show a distinct spatial distribution that seems to be similar for the various elements (figure 5.32) whereas no structure is visible on the gettered wafer side (figure 5.33). This is evidence in favor of the presented explanation for EPD reduction (section 5.12). However, no correlation between the spatial distribution of etch pits and impurities could be observed on any of the recorded maps.
Two methods to quantify the difference in impurity concentration on both wafer sides have been carried out. An essential part of quantitative XRF measurements is to subtract the background signal, i.e. all XRF photon contributions that originate from the material that surrounds the sample (sample holder, measurement chamber, etc). For this purpose, the XRF signal measured on the empty sample holder is recorded as background spectrum, that can later be subtracted from the measured spectra to obtain a background-free signal of the sample. However, a per-pixel background subtraction leads to negative peaks in some cases. This problem can be avoided when the background is subtracted from the sum of all spectra of each pixel belonging to a map, i.e. a single background correction for the sum of a map. This is the first method that has been used to determine the relative impurity concentrations between gettered and ungettered wafer side (figure 5.34). The relative fit-uncertainty of the peak area is used here as a lower limit to the uncertainty of the measured concentration. No information is available for estimating additional contributions to the uncertainty that arise due to the calibration process and beam parameters. In the scanned region, most elements are equally concentrated on both wafer sides, with the exception of zinc and possibly chromium (figure 5.34). While the significantly higher concentration of zinc on the gettered side is evidence for the EPD reduction mechanism as discussed in section 5.12, the inverse trend of chromium has to be explained (figure 5.32): The literature reports that after treatment in chromium-based preferential etch solutions (such as the here used Secco etch), adsorption layers of chromium have been measured before [82]. It is possible that this effect is more pronounced or present only on one of the two wafer sides.
For the second method for quantification of relative differences of the impurity concentration on both wafer sides, simply the sum of concentration maps (such as figures 5.32 and 5.33) are obtained and the ratio between both wafer sides is calculated (figure 5.35). Pixels of negative concentrations have been set to zero in the depicted case. However, results change by less than 2 % if negative concentration values are used unaltered. Overall, both methods give a similar impression of the relative impurity concentrations on both wafer sides. The excess of zinc and especially the behavior of chromium, however, are less significant for the second method. These analyses have been performed with PyMca [88]. Unfortunately, fit uncertainties for the per-pixel spectra could not be accessed, therefore figure 5.35 does not contain error bars.

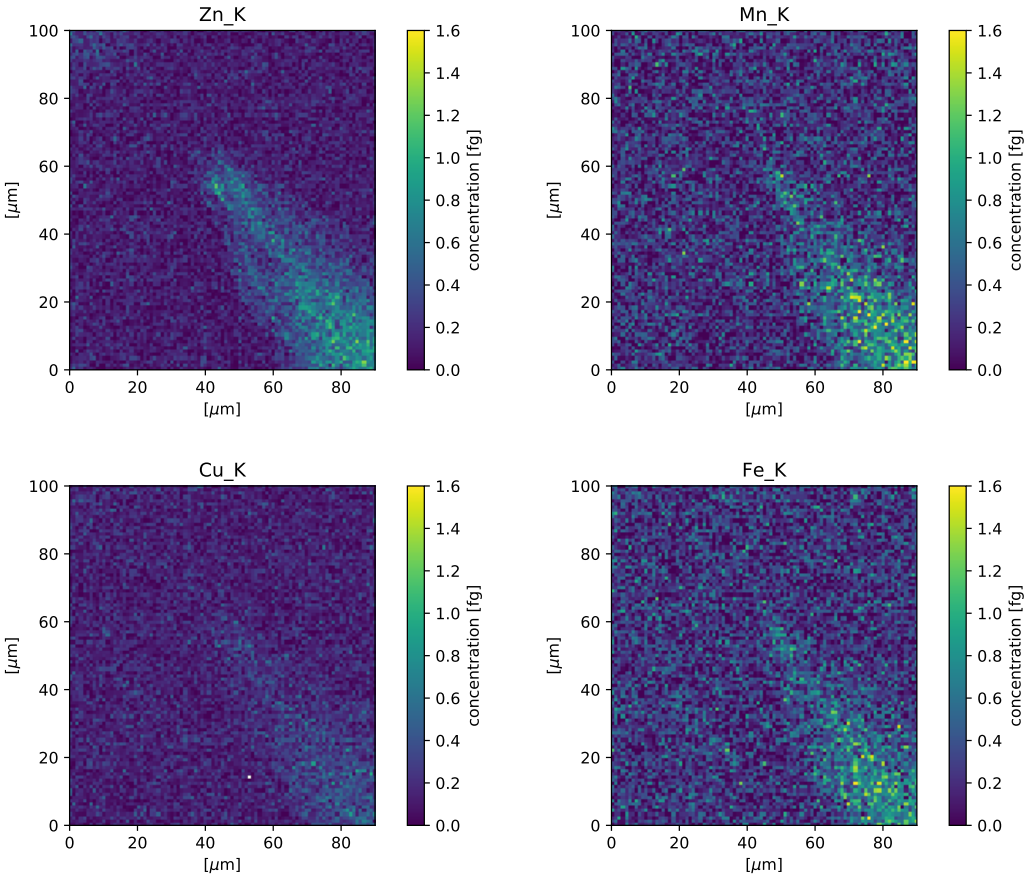


Figure 5.32.: X-ray fluorescence maps of the zinc, manganese copper and iron K_α channels show enhanced concentrations and a comparable spatial distribution of those contaminants on the ungettered wafer side. Measurements and background correction executed by Markus Rinio.

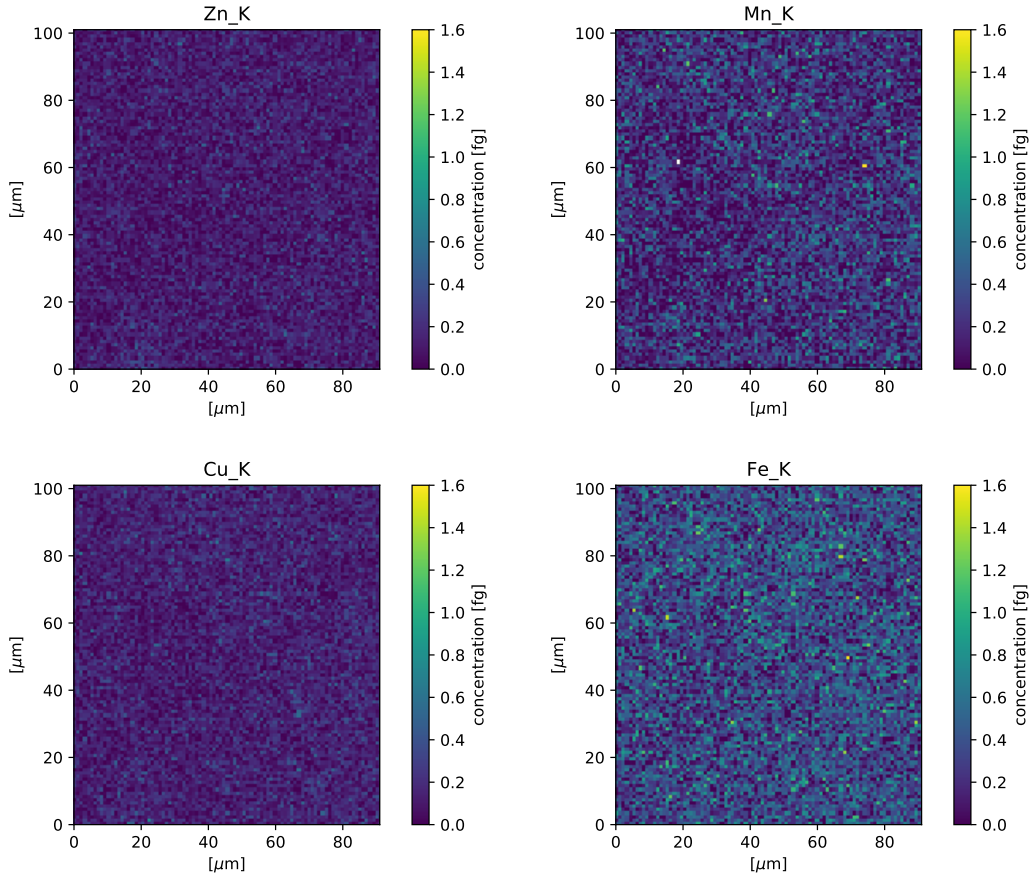


Figure 5.33.: X-ray fluorescence maps of the gettered wafer side exhibit no spatial structure in impurity concentrations. Measurements and background correction executed by Markus Rinio.

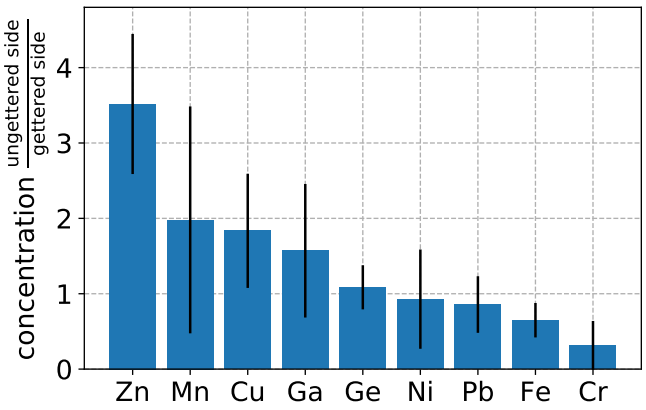


Figure 5.34.: Mean concentration of the ungettered wafer side relative to the gettered wafer side. For this measurement, the background is subtracted from the sum of all spectra belonging to each element's map. Only elements that show significant peaks in the XRF spectrum (figure 5.30) are depicted. Based on measurements executed by Markus Rinio.

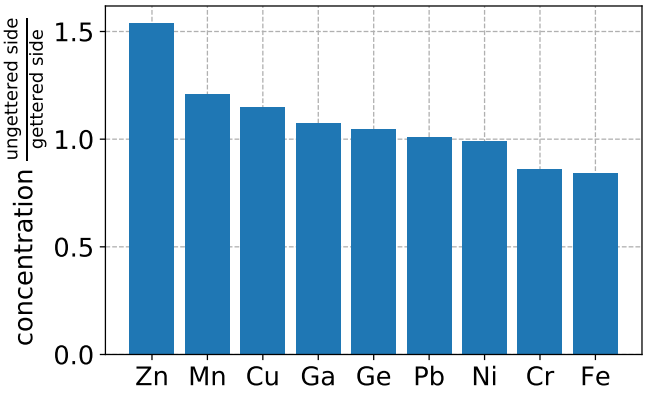


Figure 5.35.: Results of a second method for obtaining the mean concentration of the ungettered wafer side relative to the gettered wafer side: Here, simply the ratio of the sum of each concentration map (such as shown in figures 5.32 and 5.33) is used. Possible negative concentration values of single pixels are set to zero. However, if negative pixel values are kept as such, results differ by less than 2 %. Based on measurements executed by Markus Rinio.

The sample that has experienced EPD reduction reversal due to contamination in the RTP furnace (section 5.9) has been analysed for impurities. However, no general excess of a certain impurity relative to the gettered material nor a spatial correlation of impurities with etch pit structures could be observed.

As predicted by the EPD reduction mechanism discerned in section 5.12, evidence for increased impurity concentrations on the ungettered wafer side of a one-sided gettered wafer has been measured in two independent experiments: Synchrotron-based XRF measurements exhibit impurity structures and excess impurity concentrations only on the ungettered (high EPD) wafer side. Similarly, the recombination activity as measured by EBIC shows that the phosphorous gettered wafer side contains less recombination active impurities (section 5.13). These findings serve as evidence that, independently from the direct EPD studies presented in this chapter, supports the proposed mechanism for EPD reduction.

6. Conclusion and outlook

Etch pit density (EPD) measurements after defect etching are widely used to estimate the density of dislocations in crystalline materials. Ensuing from observations that for multicrystalline silicon, P-gettering can cause a reduction of the density of etch pits, it has been studied whether this phenomenon is caused by a reduction in the number of dislocations.

The mechanism that facilitates EPD reduction after P-gettering has been identified as a reduced reaction rate of the defect etch at dislocations that exhibit low impurity decoration. This interpretation has been distinguished from other candidate mechanisms by both, direct measurements of changes in the EPD after appropriate preparation states of the observed system, as well as by direct and indirect measurements of the impurity concentration. Furthermore, the idea of a reduced reaction rate in P-gettered dislocations is supported by observed changes in the etch pit depth and size for systems in various preparation states as well as by the observation of increased EPD after P gettering when etch times are increased drastically.

Other mechanisms, explaining EPD reduction with the influence of atomic species that are introduced by the P-glass, such as phosphorous, oxygen or silicon self interstitials, or mechanisms explaining EPD reduction as the consequence of annihilating dislocations could be ruled out by empirical evidence.
The prevalent assumption that EPD reduction is caused by annihilation of mobile dislocations has been shown to be in conflict with several experiments: Wafers could be prepared that exhibit EPD reduction only on one of the two wafer sides - an observation that is hard to reconcile with the notion that dislocations are removed from the material. Observations of EPD reduction in symmetric gettering systems have disproven a causal link between the phenomenon of EPD reduction and certain mechanisms that have been hypothesized to facilitate dislocation motion.
Several independent experiments have shown that EPD reduction is a reversible phenomenon, and moreover, that EPD reduction reversal seems to lead back to a similar spatial EPD distribution as measured on untreated sister wafers: Regions that revert to mid-EPD levels appear with mid-EPD in the as-grown state while likewise behavior is observed for low-EPD regions. This seeming memory of the spatial distribution of the as-grown EPD throughout the process of EPD reduction and EPD reduction reversal is strong evidence for the continued and unaltered existence of dislocations during all of these steps.

Wafers that exhibit one-sided EPD reduction show enhanced surface-close charge carrier recombination rates on the wafer side with higher EPD, from which a

relative difference in the presence of impurities on both wafer sides can be inferred. Direct observation of impurity elements with synchrotron radiation based x-ray fluorescence spectroscopy (XRF) has resulted in some evidence, that an enhanced concentration of zinc is found on the side of high EPD. Spatially resolved XRF maps show structures of various metallic impurities only on the high EPD side.

All these results support the notion, that EPD reduction is caused by a reduction of the defect etch reaction rate at dislocations that exhibit low impurity decoration. The models that so far have been used to explain the phenomenon of EPD reduction could be falsified: Dislocation motion is not causal to EPD reduction. The model proposed here offers a simple explanation by providing novel insights into the mechanism of defect etching.

Taking these results seriously, i.e. taking seriously that impurity lean dislocations exhibit a reduced reaction rate in defect etching, it must be considered whether dislocations densities in high purity silicon materials could be different from what is inferred by defect etching techniques. Applying a reliable technique for EPD reduction reversal on high purity float-zone or Czochralski grown silicon wafers, material that is currently considered to be dislocation free, it is possible that dislocations in these materials could be discovered, thereby paving the way towards further refinement of crystal growth procedures.

A. Appendix

A.1. The Wright etch and mc-Si

The Wright-etched as-grown sample features regions with hardly any etch pits, where the sister samples etched with the other etchants exhibit low or mid EPD (figure A.1). Unsurprisingly, those regions for which the Wright etch shows a lower EPD when compared to other etchants, exhibit a lower EPD after gettering, too (figure A.1). This effect turns out to be systematic to individual grains (figure A.2). Plotting a map of the size of those etch pits that do not belong to a cluster (figure A.4), reveals that regions of low etch pit density systematically exhibit smaller etch pits than what is observed in other regions. The size of etch pits, too, is clearly changing from grain to grain (figure A.2). This observation, as well as the observations of stronger EPD reduction and reduced EPD in the as-grown state, when comparing with the other etchants, indicates a reduced etch rate of the Wright etch in these regions. This is likely explained by grain orientations that deviate strongly from the (100) and (111) directions, for which the Wright etch is intended [48].
Conversely, the cluster of grains in the lower right corner of the gettered Wright-etched sample shows considerably higher EPD than for the other etchants (figure A.1). A systematically higher EPD for the same grains of the Wright-etched as-grown wafer is noticeable, too. This increase in apparent EPD must not be ascribed to an increased number of etch pits but originates from false positive events in the algorithmic etch pit detection, caused by grains that appear with dark background on Wright-etched samples (figure A.2). While the other etchants sporadically exhibit such dark grains or inter-grain contrast, too, the Wright etch does so with much higher intensity and probability. These two features, frequent and intense dark grains and selectively less etching for some grains, render the Wright etch ill-suited for EPD studies on mc-Si material.
SEM images show that high contrast (dark) grains exhibit higher surface roughness: dark grains feature surface structures of µm size, while other grains only contain features on the scale of 100 nm to 200 nm, well below the wavelengths of the visible spectrum (figure A.3). Therefore, these grains appear as reflective surfaces in the optical microscope. At the same time, there is a clear correlation between the dark grains and etch pit size (A.4): The effect is clearly systematic to specific grains, i.e. when dark surfaces occur, always the same corresponding grains of a set of sister wafers is affected.
However, there is evidence against the straightforward interpretation that dark

grains feature crystal orientations such that silicon atoms at the surface plane are bound less strong and therefore can be more easily attacked by the defect etch: a defect etch experiment with three as-grown sister wafers that were simultaneously processed in the same Secco solution resulted in dark grains on only two out of the three wafers. However, if the orientation of a grain's surface is the sole reason for whether or not the polished surface is attacked by a defect etch, all wafers should exhibit dark grains.
The idea was studied whether a local enrichment of the defect etch solution between two wafers could modify the etching behavior, thereby causing dark grains in only those sample surfaces, that during the defect etch are located close to other silicon wafers. However, despite various steps to avoid local concentration changes in the defect etch, still occasionally dark grains occur. Defect etching in a solution that due to heavy previous usage exhibits a high concentration of the reaction products, did not lead to a higher probability for the observation of dark grains. Since the intensity of dark grains with etchants other than the Wright etch is low enough that they hardly interfere with algorithmic etch pit detection (and the probability of dark grains occurring is much less than for the Wright etch), no more studies to explain this effect have been carried out. It could be shown that dark grains are originating from a change in the surface roughness after defect etching and that etch pits on dark grains increase in size the darker a grain surface (figure A.4). Important in the scope of this thesis, however, is that EPD reduction is observable on Wright-etched material, too.

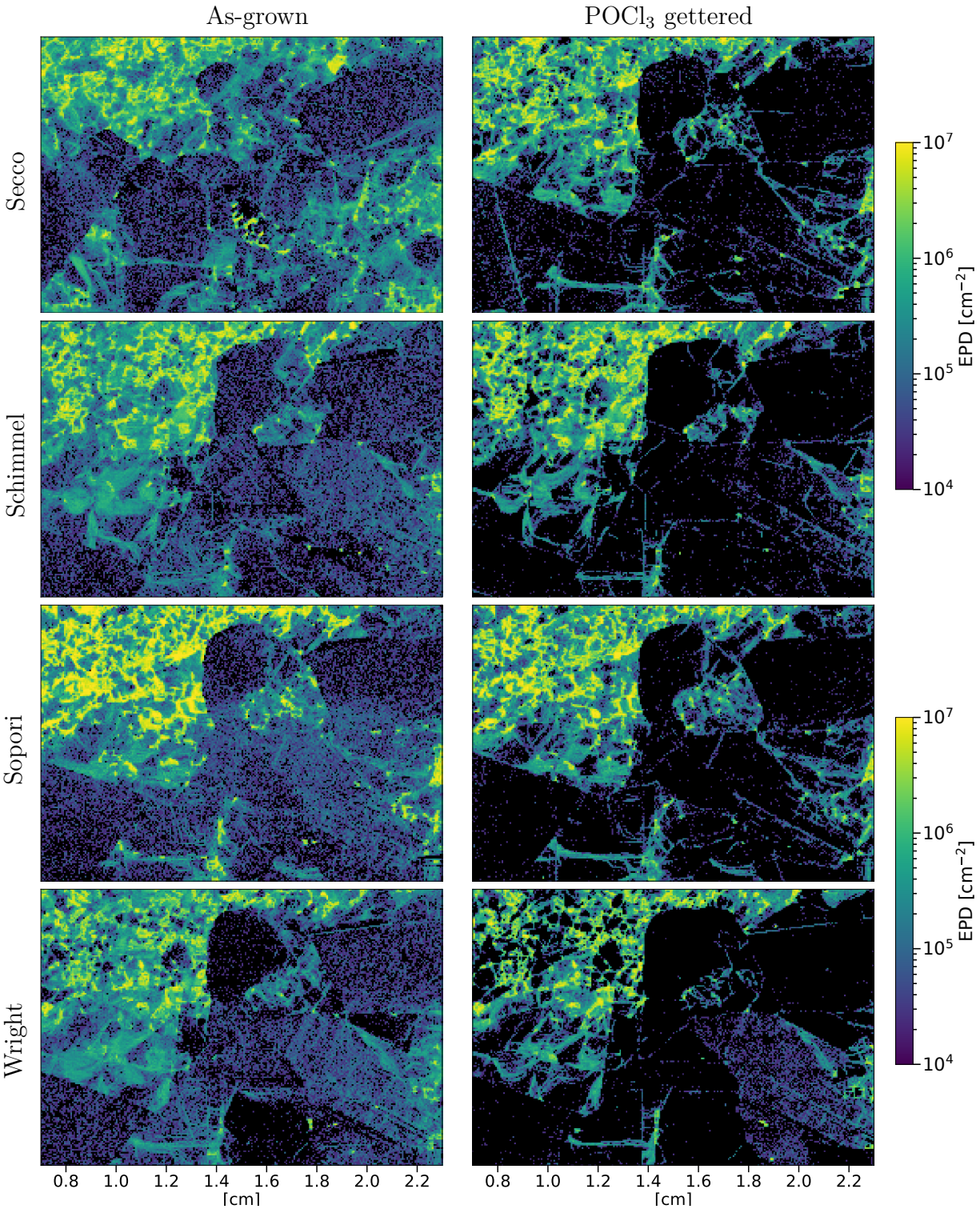
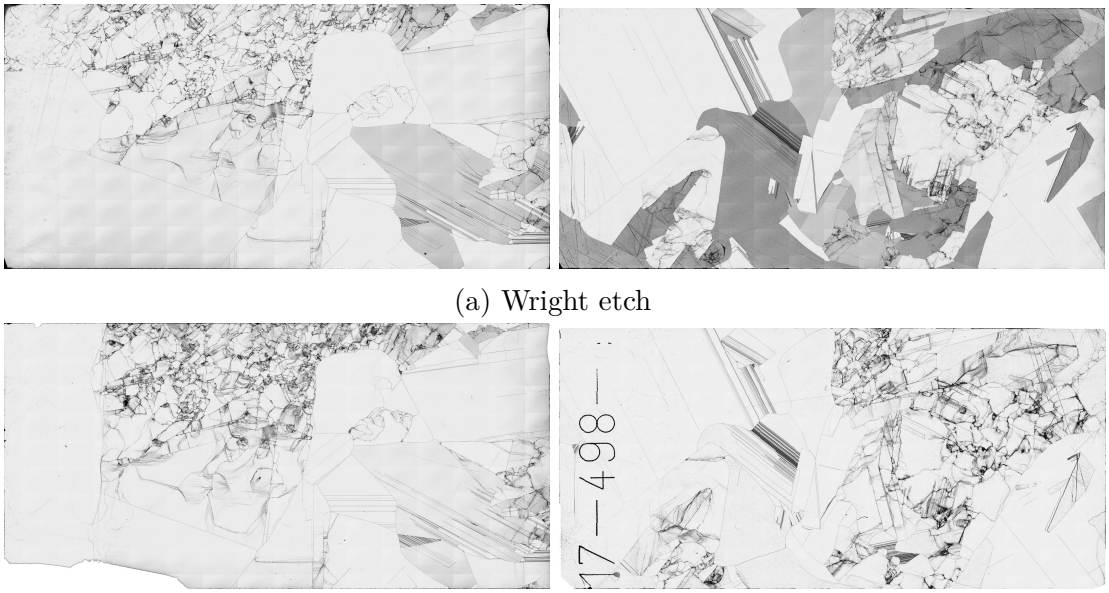


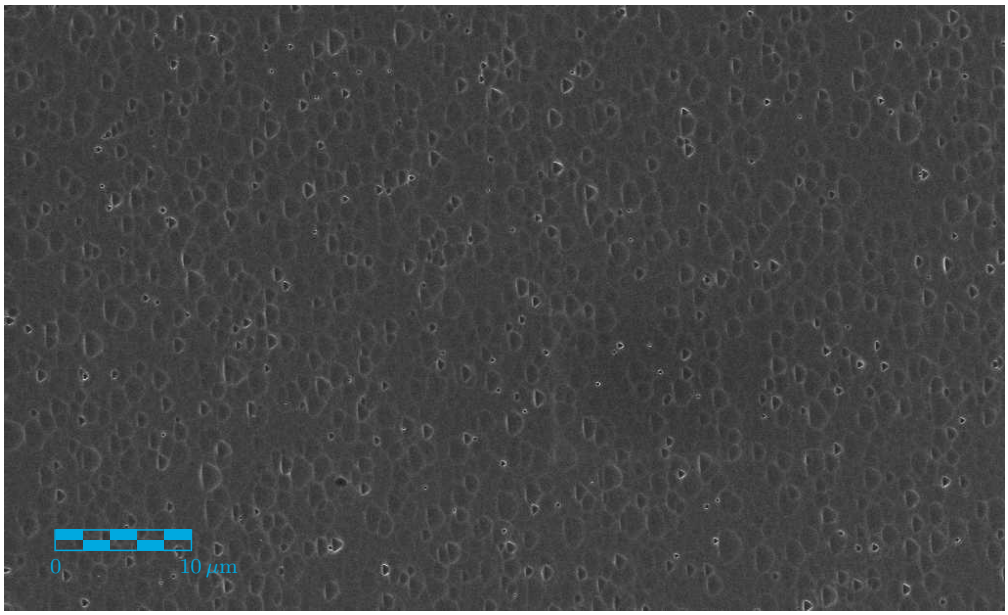
Figure A.1.: EPD of as-grown (left) and $POCl_3$ gettered (right) sister samples after defect etching with various etchants. The overall EPD in the as-grown state is comparable among the samples shown. The number of etch pits in low and mid EPD regions is reduced by about one third in the gettered samples, while clustered EPD regions remain unchanged. EPD reduction occurs in all observed samples, regardless whether the oxidizing agent is chromium based or chromium-free, therefore it can be excluded that EPD reduction is an artifact specific to certain etch solutions.



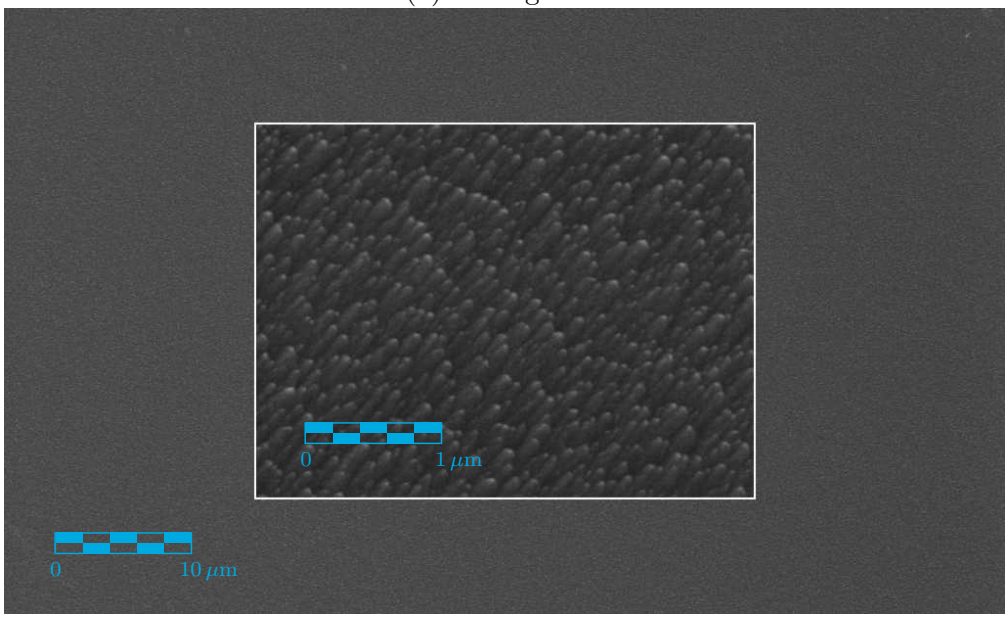
(a) Wright etch

(b) Schimmel etch

Figure A.2.: Two examples of inter-grain contrast as recorded by the optical microscope on Wright-etched samples (top row), compared to sister samples etched with the Schimmel solution (bottom row). Dark grains for the Wright etch are significantly stronger than for the other etchants. Comparing grains with dark and light background with the SEM shows that grains with dark background feature rougher surface structures (figure A.3). Threshold-based algorithmic detection of etch pits, as used in this thesis, is prone to false positive detection for these dark grains. The Wright etch is hence considered ill-suited for automated etch pit analyses on mc-Si material.

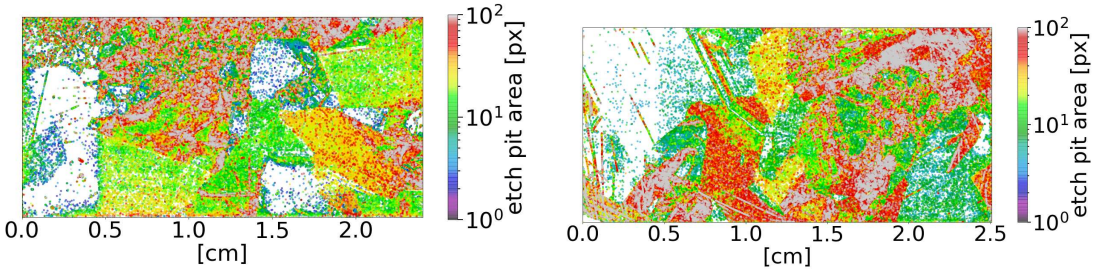


(a) Dark grain



(b) Normal grain

Figure A.3.: SEM image of the wafer surface after polishing and subsequent 240 s Wright etch. The surface structures on the grain that appears dark in the optical microscope (a) exhibits structures of micrometer size, while surface structures on other grains are considerably below the wavelength of the optical spectrum (b).



(a) Etch pit size

(b) Microscope image

Figure A.4.: Scatter plots of Wright-etched as-grown samples, where every marker corresponds to a single etch pit in a color corresponding to the etch pit size (a). Because in scatter plots makers close to each other will overlap, markers are drawn in ascending sequence such that the largest etch pits are drawn last. This allows to see the spatial distribution of the largest etch pits while suppressing noise in dark grains. A comparison with microscope images of the wafer surface reveals that the maximum etch pit size is systematically changing with grains (b). Furthermore, a clear correlation between large etch pits and dark grains is observed. This systematic change in the etch pit size from one grain to another is observed for all studied defect etchants with the exception of the Sopori etch and is observable regardless whether dark grains appear or not.

A.2. Chemo-mechanical polishing of surfaces

This section contains practical information about each step of the polishing procedure. Since polishing is a time consuming process and since results can not be judged immediately but only after defect etching, it takes a long time to isolate mistakes and improve the procedure. Hopefully, this section can help to achieve good results quickly.
The process can be divided into four steps:

1. Glueing the sample onto the sample holder
2. Flattening the sample
3. Polishing the sample
4. Removing polishing wax and preparation for defect etch

Glueing the sample onto the sample holder

It is crucial to glue the sample plane-parallel to the jig surface, otherwise the flattening process results in a wedge-shaped sample. Use a hot-plate to heat the metal jig head and apply a moderate amount of wax. Too little wax will result in chipped edges or breaking of the wafer during polishing.
The glued sample is placed into a clamping device such that the sample (and the wax) is cooled under mechanical pressure. Use a small piece of thin (here 100 µm) Teflon foil for separating the stack of jig head, wax and sample from the clamping device. This foil is very cheap, heat resistant and easily removed after the wax has cooled. A proper Teflon foil will not cause wafer breakage!
Viscosity of the wax changes drastically with temperature. Use temperatures as high as possible without disintegrating the wax (look for fumes). Initially set the hot-plate to 220 °C for a fast heat-up. The temperature can be reduced to about 120 °C to 150 °C. The low viscosity of hotter wax results in better plane-parallel attachment under pressure. Keep in mind that the jig head's temperature lags behind the hotplate temperature, therefore the wax temperature will not reach the hot-plate temperature if you work fast.
If wafer edges are chipping during polishing, it could be that too little wax is used. Chipping edges can be reduced, too, by moving the sample over the molten wax, accumulating wax at the edges. This, however, also results in an slight curvature of the sample, leading to more material removal close to the wafer edges. I therefore recommend that any movement of the sample in the molten wax is avoided.
Cool the combination of the hot jig head, Teflon foil, wax and sample in the clamping device until the jig head is cold enough to be touched (i.e. a minute or two). Only then you may use cold water to harden the wax.
Let excess wax be connected to the jig, such that the wafer edges are protected during polishing.

Flattening the sample

Wet polishing for flattening the sample is done at 20 rotations per minute, using the pressure of about 1/3 kg weight force per cm^2.
Flattening is complete when the whole surface is evenly scratched. If individual grains can be identified that appear to have significantly different surface scratching, the process is not finished yet. Using a fresh sand paper of 10 µm grain size, this step takes about 3 min to 6 min.
Regarding different types and batches of sand papers: Some sand papers with a grain size of 5 µm have been successfully used for flattening wafers in about 5 min, while with another type of 5 µm sand paper, it was impossible to remove enough material.

Polishing the sample

Most importantly: Avoid to carry over any polishing particles from the flattening process to the polishing process: A single sand-paper grain can be the difference between countless and zero scratches. Therefore, diligently rinse and wipe the jig and sample.
Polishing is done using an alkaline colloid solution of SiO_2 of 0.032 µm grain size (LOGITECH Syton Typ SF1) on a wet aluminium-oxide foam plate. With a drop rate of about 1 drop every 3 to 5 seconds and similar rotation and pressure settings as before, a good mirror polish is achieved after 90 min. Beware that not all surface damage (scratches) can be detected visibly, even under the microscope. A surface that seems perfectly devoid of scratches and marks under the optical microscope can still reveal scratches after the defect etching process. An SF1 polishing step of 90 min should be regarded as the minimum time when flattening has been carried out with 10 µm sand paper. Using the workable 5 µm grain size sand paper, 60 min SF1 polishing have been sufficient.

Removing polishing wax and preparation for defect etch

The wafer can be removed from the jig head after melting the wax with the hot plate. Consider removing excess wax from the jig head before heating. Wax from the back side of the wafer has to be removed before defect etching to avoid artifacts. Two cascades of hot piranha solution (10 min each) followed by a dip in diluted HF have been used to reliably free the samples of wax residue.
The last HF dip should be done immediately before the defect etch step.

Zusammenfassung

Messungen der räumlichen Dichte von Ätzgruben (EPD, „etch pit density“), die durch chemisches Defektätzen erzeugt werden können, sind weit verbreitet als Methode zur Bestimmung der Dichte von Kristallversetzungen. Ausgehend von der Beobachtung, dass phosphorbasiertes Diffusionsgettern (ein in der Photovoltaik etablierter Schritt zur Verbesserung der Materialqualität) eine Reduktion der beobachtbaren Ätzgrubendichte auf multikristallinem Silizium bewirken kann, wurde die Frage untersucht, ob die schwindende Anzahl von Ätzgruben gleichbedeutend mit dem Verschwinden von Versetzungen ist.

Ein in diesem Zusammenhang entwickelter Algorithmus, der aus Bilddaten geätzter Siliziumoberflächen, unter gezielter Auslassung von Korngrenzen, die Ätzgrubendichte bestimmt, wurde in einer Python Implementation als quelloffene Software unter freier Lizenz veröffentlicht.

Im Rahmen dieser Arbeit wurde, unter anderem mit Hilfe der genannten Software, der Mechanismus, der dem Phänomen der EPD Reduktion zugrunde liegt, erkannt und beschrieben: Die Reaktionsrate der Defektätzreaktion hängt entscheidend davon ab, ob Kristallversetzungen mit Fremdatomen verunreinigt sind oder nicht. Versetzungen, die arm an Verunreinigungen sind, reagieren signifikant langsamer mit Defektätzlösungen.
Es wurde gezeigt, dass diese Interpretation, im Gegensatz zu den übrigen bekannten Erklärungsmodellen, durch eine Reihe experimenteller Beobachtungen gestützt wird, die sowohl auf direkter Messung der Ätzgrubendichte an geeignet präparierten Kristallproben als auch auf direkten und indirekten Messungen der Verunreinigungskonzentration basieren.
Des Weiteren wird die Hypothese, dass der Phosphorgetterschritt die Defektätzrate reduziert, durch die Beobachtungen bekräftigt, dass einerseits Größe und Tiefe von Ätzgruben in Abhängigkeit des präparierten Zustandes variieren und dass andererseits die Anzahl der Ätzgruben nach EPD Reduktion durch drastisches Verlängern der Ätzzeit wieder ansteigt.

Es konnte explizit ausgeschlossen werden, dass die durch die Phosphordiffusion bedingte Präsenz von Phosphor-, Sauerstoff- und interstitiellen Siliziumatomen ursächlich für EPD Reduktion ist. Ebenfalls wurde durch mehrere Experimente die etablierte Annahme falsifiziert, dass EPD Reduktion durch die Bewegung und paarweise Vernichtung von Versetzungen verursacht wird: Es konnten Wafer hergestellt werden, die EPD Reduktion nur auf einer Waferseite aufweisen - eine Beobachtung, die kaum mit der Hypothese in Einklang gebracht werden kann, dass

Versetzungen aus dem Material verschwinden. Einzelne konkrete Mechanismen, die als ursächlich für die Bewegung von Versetzungen vermutet wurden, konnten durch Beobachtung von EPD Reduktion bei räumlich symmetrischer Anordnung der Gettersenken widerlegt werden.
Mit mehreren voneinander unabhängigen Experimenten konnte gezeigt werden, dass es sich bei der EPD Reduktion um ein reversibles Phänomen handelt. Dabei ist insbesondere hervorzuheben, dass eine solche Umkehr der EPD Reduktion zur ursprünglichen räumlichen Verteilung der Ätzgrubendichte zurückführt. Eine solche Speicherung der räumlichen EPD Information, ausgehend vom Ursprungszustand, über den Zustand der EPD Reduktion hin zum Zustand nach der Umkehrung der EPD Reduktion, ist ein starkes Indiz für die unveränderte Existenz von Versetzungen während aller dieser Phasen.

An Material, das EPD Reduktion nur auf einer Waferseite aufweist, deuten Messungen der oberflächennahen Ladungsträgerrekombinationsrate darauf hin, dass die beiden Seiten des Wafers, der Hypothese entsprechend, verschiedene Verunreinigungskonzentrationen aufweisen. Ein Versuch mittels synchrotronbasierter Röntgenfluoreszenz Unterschiede in der Verunreinigungskonzentration beider Waferseiten direkt nachzuweisen, zeigt einerseits Strukturen von Verunreinigungen, die nur auf der Waferseite mit hoher EPD nachgewiesen werden konnten. Andererseits ergaben gemittelte Messungen eine erhöhte Konzentration von Zink auf der Waferseite mit hoher EPD.

All diese Resultate sind positive Indizien für die Hypothese, dass Versetzungen, die arm an Verunreinigungen sind, eine geringere Reaktionsrate mit den Defektätzlösungen aufweisen als solche Versetzungen, die stark mit Verunreinigungen dekoriert sind. Bisherige Modelle zur Erklärung von EPD Reduktion, insbesondere solche, die EPD Reduktion mit der Auslöschung von Versetzungen erklären, sind nicht mehr haltbar.

Nimmt man diese Resultate ernst, d.h. nimmt man ernst, dass Versetzungen, die arm an Verunreinigungen sind, tatsächlich nicht durch Defektätzen sichtbar gemacht werden können, muss auch in Betracht gezogen werden, ob Versetzungsdichten in hochreinem Silizium von jenen Werten abweichen, die durch Defektätzen ermittelt werden. Es besteht die Möglichkeit, dass mit einer zuverlässigen Methode zur Umkehr der EPD Reduktion Versetzungen in hochreinem Czochralski oder Float-Zone Silizium nachgewiesen werden können. Gelingt ein solcher Nachweis, sind weitere Verbesserungen dieser Kristallzuchtverfahren denkbar.

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