High-Efficiency Multicrystalline Silicon Solar Cells

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1 Introduction

1.1 Thesis motivation

Photovoltaics, the conversion of sunlight into electricity, is a very promising technology for satisfying current and future energy demands in a sustainable and environmentally friendly way. There is a rapidly expanding market calling for advanced technologies and devices capable of yielding higher performance at lower cost. The typical cost distribution of a photovoltaic module is presented in Fig. 1.1.

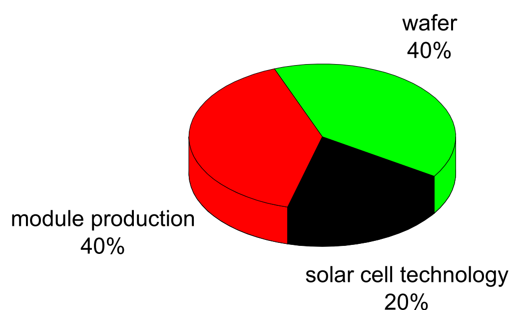

Fig. 1.1: Cost distribution of a photovoltaic module. The wafer accounts for about 40 % of the total module price [1].

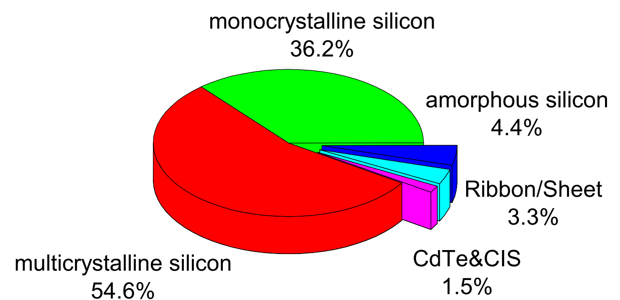

Fig. 1.2: Shares of different solar cell technology options of the total global market volume 2004 [2].

The wafer material contributes to about 40 % to the total cost. Thus, it is attractive to use low-cost material and at the same time achieve a high conversion efficiency. Silicon has shown itself able to fulfil these demands (Fig. 1.2). Nevertheless, the production of silicon from the raw material silica sand is complicated and requires many purification processes. Once comparatively pure silicon is obtained, it is necessary to convert it into the form of thin sheets/wafers of good crystalline quality.

One cost-effective way is the production of multicrystalline silicon. It is cast from molten silicon and solidifies inside a crucible made of graphite or quartz. The result is a multicrystalline silicon block with comparatively large grains

(millimetres to centimetres) of different crystal orientation. The solidification proceeds from bottom to top. Since impurities have a higher solubility in molten silicon than in the solid crystal, the impurity concentration is increased in the top layer. The crystallographic quality at the surfaces is rather poor and impurities from the crucible can diffuse into the silicon. Therefore the outer parts of the block are usually cut away before the block is sawn into several ingots.

A higher crystallographic quality is achieved with the Czochralski method (Cz). A small single-crystal is used as a seed and the ingot is pulled from the molten silicon. This results in monocrystalline silicon ingots but impurities like oxygen are introduced from the quartz crucible. This contamination is avoided with the floating zone method (FZ) where a single-crystal seed is placed at the bottom of a polycrystalline ingot of clean silicon. A melting zone slowly moves upwards from bottom to top. The silicon solidifies as a monocrystalline ingot and the impurities agglomerate in the top which can be cut away. This method produces silicon of the highest quality but also of high cost.

All these methods bear the drawback that the wafers have to be sliced from the ingot. About half the silicon is lost during this sawing process. The limitations of the ingot approach can be overcome if the silicon is formed directly into sheets or ribbons. The most prominent examples are edge-defined film-fed growth (EFG) or string-ribbon (SR). Slicing losses are avoided but the ratio of surface/volume during crystallisation is very high. This leads to relatively poor crystallographic quality and high impurity levels. In this case the top and bottom layers cannot be cut away for the whole ingot but may be etched away on every individual slice.

Thus, multicrystalline silicon is the dominant material for solar cell production because it constitutes a good compromise of quality and price and decent solar cell efficiencies of 14 - 15 % are achieved in commercial production. In order to attain further cost reduction, thinner wafers need to be used. This approach in turn increases the ratio of diffusion length to thickness. It enhances the importance of the surface and requires new cell concepts with well passivated surfaces in order to obtain higher efficiencies. Therefore sophisticated technologies like passivation and texturing of the surface become important for the future development of cell structures.

Since multicrystalline silicon suffers from crystal defects and impurities and their interaction can change the material quality during solar cell processing, a

deeper understanding of the process-induced changes needs to be acquired. This allows for the purposeful optimisation of process parameters and the development of new production processes. This is accomplished within this thesis.

1.2 Thesis outline

In **chapter 2** the operation principle of solar cells based on semiconductors is described. The basic equations of solar cell physics which are used throughout this thesis are introduced. The importance of a high effective minority carrier diffusion length for a maximised conversion efficiency is highlighted. This requires a cell structure with very well passivated surfaces and small electrical losses. At the same time a high material quality is indispensable. The established ways to fabricate high-efficiency silicon solar cells are described. They incorporate many oxidations at elevated temperatures and it is shown that these high temperatures degrade the defect-rich multicrystalline silicon. This obstructs the successful application of the standard processes on this material.

In **chapter 3** the effect of oxidations and diffusions on the minority carrier lifetime in multicrystalline silicon is investigated. This is performed with area-averaged measurements in order to optimise process parameters for thermal oxidation and impurity gettering. For a more detailed investigation locally resolved measurements of the minority carrier lifetime and the dislocation density of the crystals are compared. A clear correlation between these two parameters is established and the limitation of carrier lifetime by crystal defects is quantitatively described. A microscopic model is discussed which explains the impact of temperature on the degradation of multicrystalline silicon during oxidation and the gettering efficiency of phosphorus diffusions. The results of this chapter allow to draw conclusions for the process parameters and the process sequence during solar cell production.

In **chapter 4** methods for structuring the front surface are described. A texturing process for multicrystalline silicon has to be independent of the differing crystal orientations of the grains. A plasma-etching process working at low temperature is developed and characterised.

Texturing changes the surface structure and increases the surface area. In **chapter 5** the emitter diffusion is adjusted to this new front structure. Emitter dark saturation currents are measured, and the optimisation also accounts for the effect of the emitter diffusion on the multicrystalline material quality. The contact quality in combination with the metal grid is measured and one emitter is chosen to produce the solar cells.

In **chapter 6** the oxidation of the silicon surface at the rear, one of the most important processes for a high solar cell efficiency, is investigated in more detail. The growth rate is significantly increased by the addition of water vapour to the oxidation ambience. This is called wet oxidation and allows for the reduction of the process temperature from 1050 °C to 800 °C avoiding the material degradation of multicrystalline silicon. The quality of the wet oxide applied as rear surface passivation in solar cells is investigated by carrier lifetime measurements. The developed processes, which were described in the previous chapters, are combined to a production sequence for high-efficiency multicrystalline silicon solar cells.

In **chapter 7** these cells, which are almost entirely dominated by the material quality, are used to investigate the influence of the inhomogeneous minority carrier lifetime on the solar cell parameters. Spatially resolved minority carrier density measurements of emitter-diffused and oxidised samples are used to model the solar cell parameters. Such sample preparation is preferred because these wafers were exposed to the same critical processes which can change the material quality, as the corresponding solar cells. However, the emitter enables the flow of carriers from grains of high lifetime to regions of low lifetime during the measurement. An analytical procedure to calculate the real material quality from these blurred measurements is presented and the open-circuit voltage and the short-circuit current density are predicted from the carrier density measurement.

In the **Appendix** the lifetime measurement methods of photoconductance decay (PCD), quasi steady-state photoconductance (QssPC) and carrier density imaging (CDI), which were used throughout this work, are briefly described.

2 Crystalline silicon solar cells

2.1 Introduction

Solar cells are devices constructed to convert sunlight into electricity. The operating principle of solar cells based on semiconductors is described in section 2.2. The basic equations used throughout this work are introduced and the necessity of a high minority carrier lifetime for good solar cell performance is highlighted. In section 2.3 the loss mechanisms present in crystalline silicon solar cells are discussed; ways of their reduction by the design of the cell structure are presented in section 2.4. This includes texturing, highly doped regions under the metal contacts and surface passivation by thermal oxidation. Those measures were originally introduced for monocrystalline silicon solar cells. In section 2.5 their direct application to multicrystalline silicon is shown to fail because of the high temperatures which are applied during the processes. They drastically reduce the minority carrier lifetime, the key parameter for high-efficiency crystalline silicon solar cells.

2.2 Operation principle and basic equations of device physics

A simple cell concept for a *p*-type crystalline silicon solar cell is presented in Fig. 2-1. It is not only the base for most solar cells in industrial production but also for the best high-efficiency silicon solar cells produced to date. Such a solar cell can be regarded as a large-area diode with a relatively thin emitter (*n*-type, thickness $d \approx 0.2$ - $2\ \mu m$) and a thick base (*p*-type, $d \approx 50$ - $500\ \mu m$). The emitter is on the front surface where the incident light is coupled into the cell to create electron-hole pairs by absorbing photons of sufficient energy. The carriers diffuse to the space charge region of the *p/n*-junction where they are separated and are converted from minority carriers to majority carriers. Those can be extracted at the metal contacts on the front and rear to deliver electrical power. In the following subsections the *I-V* curve as well as some equations used throughout this work are

introduced based on thermodynamical considerations as well as the fundamental equations of semiconductor device physics. More detailed descriptions of silicon solar cells can be found in the corresponding literature [3-5].

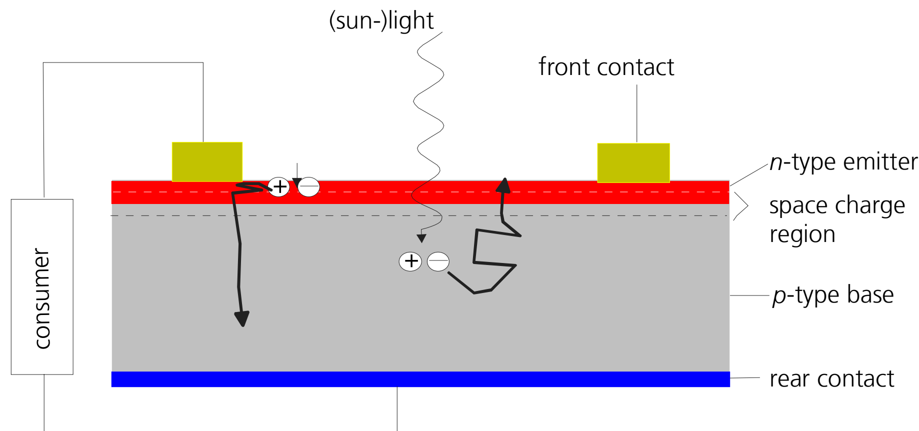

Fig. 2-1: Schematic drawing of a simple solar cell. The absorbed light creates electron-hole pairs. The carriers need to diffuse to the *p*/*n*-junction where they are separated before being extracted at the metal contacts.

2.2.1 Carrier density and the electrochemical potential

At absolute zero T = 0 K, electrons in a crystal occupy the lowest possible energy states. A fundamental physical theorem, Pauli's exclusion principle, implies that each allowed energy level can only be occupied by not more than two electrons (each of opposite spin). Thus, all available states below a certain energy in the crystal will be occupied by two electrons. This energy level is known as the Fermi level ε_F. With increasing temperature, some electrons gain energy in excess of the Fermi level. The probability of occupation of an allowed state of any given energy ε can be calculated from statistical considerations taking into account the constraints imposed by Pauli's exclusion principle. The resulting Fermi distribution $F(\varepsilon)$ is given by

$$F(\varepsilon) = \frac{1}{1 + \exp\left(\frac{\varepsilon - \varepsilon_F}{kT}\right)} \qquad \text{2-1}$$

where k is Boltzmann's constant and T the absolute temperature. The Fermi energy can be identified with the electrochemical potential η_e which is derived from the chemical potential μ_e and the electric potential φ via

$$\varepsilon_F = \eta_e = \mu_e - q\varphi \qquad 2\text{-}2$$

with q being the elementary charge. Knowing the density of allowed states $D(\varepsilon)$ and the probability of occupation of these states, the density of free electrons n can be calculated by integration from the conduction band edge ε_C:

$$n = \int_{\varepsilon_C}^{\infty} D(\varepsilon) F(\varepsilon) d\varepsilon . \qquad 2\text{-}3$$

Since ε_C is at least $3 \cdot kT$ larger than ε_F, $F(\varepsilon)$ can be approximated by the Boltzmann distribution:

$$F(\varepsilon) \approx \frac{1}{\exp\left(\frac{\varepsilon - \varepsilon_F}{kT}\right)} . \qquad 2\text{-}4$$

Introducing the effective density of states in the conduction band N_C, a constant at a fixed temperature T, n can be expressed as

$$n = N_C \exp\left(\frac{\varepsilon_F - \varepsilon_C}{kT}\right) . \qquad 2\text{-}5$$

Using equation 2-2, the electrochemical potential for electrons is derived as

$$\eta_e = kT \ln\left(\frac{n}{N_C}\right) + \varepsilon_C . \qquad 2\text{-}6$$

The chemical potential can be split into a concentration-independent part μ_{e0}, which depends on the chemical surroundings of the electron, and a part depending on concentration. Thus the energy of the conduction band edge ε_C can be identified as

$$\varepsilon_C = \mu_{e0} - q\varphi \qquad 2\text{-}7$$

which results in

$$\eta_e = \mu_{e0} + kT \ln\left(\frac{n}{N_C}\right) - q\varphi \qquad 2\text{-}8$$

and

$$\mu_e = \mu_{e0} + kT \ln\left(\frac{n}{N_C}\right) . \qquad 2\text{-}9$$

Similarly, the density of holes in the valence band is given by

$$p = N_V \exp\left(\frac{\varepsilon_V - \varepsilon_F}{kT}\right) \qquad 2\text{-}10$$

where N_V is the effective density of states for holes and ε_V is the upper band edge of the valence band. Thus the product of the density of electrons and holes in equilibrium can be calculated as

$$np = N_C N_V \exp\left(\frac{\varepsilon_F - \varepsilon_C + \varepsilon_V - \varepsilon_F}{kT}\right) = N_C N_V \exp\left(\frac{\varepsilon_G}{kT}\right) \equiv n_i^2 . \qquad 2\text{-}11$$

The electron and hole concentration equals n_i in an intrinsic, i.e. undoped semiconductor: $np = n_i^2$ with $n_i \approx 1 \cdot 10^{10}$ cm^3 in silicon [6].

In the case of doping with donors of concentration N_D the semiconductor becomes n-type and $n \approx N_D$. Doping with acceptors of concentration N_A results in p-type silicon and $p \approx N_A$. Therefore it is

$$p = \frac{n_i^2}{N_D} \quad \text{and} \quad n = \frac{n_i^2}{N_A} . \qquad 2\text{-}12$$

The carriers in higher concentration are denoted as majority carriers and the ones in lower concentration as minority carriers.

The generation of carriers in excess of thermal generation increases the concentrations of electrons and holes. An analogous description to equilibrium conditions can be obtained by introducing separate Fermi energy levels for electrons and holes, the quasi-Fermi levels ε_{FC} and ε_{FV}. These are defined in a way that replacement of the single Fermi level ε_F in the equilibrium expressions of equation 2-5 and 2-10 by the quasi-Fermi levels ε_{FC} and ε_{FV} yields the non-equilibrium carrier densities

$$n = N_C \exp\left(\frac{\varepsilon_{FC} - \varepsilon_C}{kT}\right) \quad \text{and} \quad p = N_V \exp\left(\frac{\varepsilon_V - \varepsilon_{FV}}{kT}\right). \qquad 2\text{-}13$$

In the case of gradients in the quasi-Fermi level, the carriers start flowing to balance the difference. The current density j_e of electrons is

$$j_e = \frac{\sigma_e}{q} grad(\varepsilon_{FC}) \qquad 2\text{-}14$$

with σ_e being the conductivity of the semiconductor for electrons and q the elementary charge.

2.2.2 Minority carrier lifetime and recombination

In a semiconductor in the dark electrons and holes are constantly generated by thermal generation G_{th}. However, the concentration of free electrons is constant since they recombine with holes with the rate R_{th} and under steady state conditions $G_{th} = R_{th}$. Having an additional generation of electrons and holes G_L, e.g. by absorption of light, the concentration of electrons increases. The two types of carriers are not in equilibrium anymore and the recombination also increases in a way that the equilibrium values are reached again when the additional generation is switched off.

For electrons (and similarly for holes) the continuity equation links the current density j_e, the generation G and the recombination R with the carrier concentration n:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\, j_e - R + G \,. \qquad \text{2-15}$$

Without current flow this equation simplifies to

$$\frac{\partial n}{\partial t} = G - R = G_L + G_{th} - R \qquad \text{2-16}$$

when the generation is split into the contributions caused by thermal generation and illumination $G = G_{th}+G_L$. The net recombination rate U is defined as

$$U \equiv R - G_{th} \qquad \text{2-17}$$

(because of $R_{th} = G_{th}$) and equation 2-16 is simplified to

$$\frac{\partial n}{\partial t} = G_L - U \,. \qquad \text{2-18}$$

The recombination activity $1/\tau$, or the carrier lifetime τ, is defined as

$$\frac{1}{\tau} \equiv \frac{U}{n - n_0} = \frac{U}{\Delta n} \qquad \text{2-19}$$

where n_0 is the carrier concentration in equilibrium and Δn the excess carrier density. Under steady state conditions the carrier concentration is constant and using equations 2-18 and 2-19 the basic equation

$$\tau = \frac{\Delta n}{G_L} \qquad \text{2-20}$$

is derived. With the diffusion constant of electrons D_e the lifetime can be converted into the diffusion length L:

$$L = \sqrt{D_e \tau} \,. \tag{2-21}$$

The diffusion length is the average distance an electron with lifetime τ can migrate through the cell before recombining with a hole.

The generation of carriers by the absorption of photons is, in most practical cases, orders of magnitude larger than the thermal generation, thus $G \approx G_L$. The continuity equation 2-15 under steady-state conditions can therefore be written as

$$\frac{1}{q} div\, j_e - \frac{\Delta n}{\tau} + G = 0 \,. \tag{2-22}$$

2.2.3 Solar cells under operating conditions

Solar cells are devices designed to convert sunlight into electrical energy. The absorption of photons in the semiconductor creates free electrons in the conduction band and holes in the valence band. The distribution of electrons and holes can be described by quasi-Fermi levels, and holes and electrons have their own electrochemical potential. The sum of the electrochemical potentials of one created electron-hole-pair is the sum of the chemical potentials:

$$\eta_e + \eta_h = \mu_e - q\varphi + \mu_h + q\varphi = \mu_e + \mu_h \,. \tag{2-23}$$

Therefore the energy of the photons is converted to chemical energy. The electrons and holes need to be separated to be extracted at the contacts. The junction of a *p*-type and a *n*-type semiconductor, a *p/n* junction, can be used to separate the electrons and holes.

The carriers can flow between the two regions until the gradient of the electrochemical potential becomes zero, i.e. $\eta_e^p = \eta_e^n$ with the upper indices denoting the *n*-type and *p*-type regions, respectively. This creates a gradient in the electric potential between the two regions and thus a band bending. Using equation 2-8 it follows

$$\mu_{e0}^p + kT \ln\left(\frac{n^p}{N_C}\right) - q\varphi^p = \mu_{e0}^n + kT \ln\left(\frac{n^n}{N_C}\right) - q\varphi^n \,. \tag{2-24}$$

The doping atoms hardly change the chemical surroundings and therefore it is

$$\mu_{e0}^p = \mu_{e0}^n \tag{2-25}$$

and

$$\varphi^n - \varphi^p = \frac{kT}{q}\ln\left(\frac{n^n}{n^p}\right). \tag{2-26}$$

Using

$$n^n = N_D \text{ and } n^p = \frac{n_i^2}{N_A} \tag{2-27}$$

where N_D are the donors in the *n*-type and N_A are the acceptors in the *p*-type region, the difference in the potential, called the built-in potential V_{bi}, is

$$V_{bi} = \varphi^n - \varphi^p = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right). \tag{2-28}$$

Under illumination the carrier densities are described by the quasi-Fermi levels. By contacting such a *p/n*-junction at the physical surfaces, a simple solar cell is constructed. At the metal contacts recombination is so high that equilibrium between electrons and holes exists. As in the dark, one Fermi level is sufficient to describe the carrier densities. But since the two contacts are located at differently doped layers (*p*- and *n*-type), different carrier concentrations arise. The gradient in the electrochemical potential is equal to the product of the elementary charge q and the voltage V_{OC}, which can be measured between the contacts of a solar cell under open-circuit conditions (see Fig. 2-2). Under short-circuit conditions, the energy levels split due to the generation of carriers by photon absorption, and high gradients in the quasi-Fermi levels arise. This induces a high current density and the electrons flow to the contact of the *n*-type and the holes to the contact of the *p*-type region (see Fig. 2-3).

Under open-circuit conditions the gradient between the electrochemical potentials is maximum but no carriers are extracted from the solar cell. Under short-circuit conditions the maximum amount of carriers is extracted but at no difference in the potential. Therefore in both cases the delivered power is zero. The maximum power extraction is reached between open-circuit and short-circuit conditions and can be regulated by external consumers. It is called maximum power point (mpp) and comprises a high potential and a high current density between the contacts.

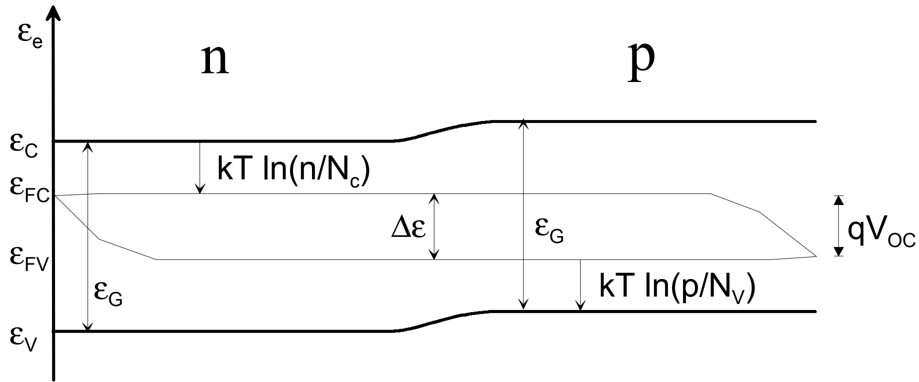

Fig. 2-2: Illustration of the energy levels of an illuminated *p/n*-junction with surface recombination under open-circuit conditions.

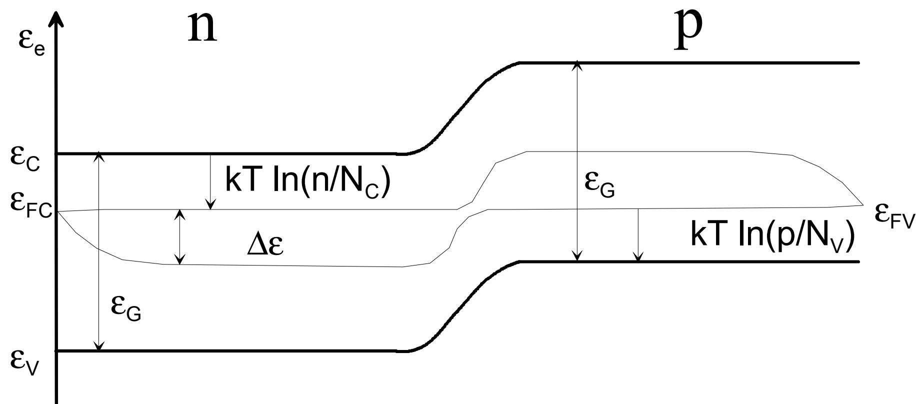

Fig. 2-3: Illustration of the energy levels of an illuminated *p/n*-junction with surface recombination under short-circuit conditions.

The quality of a solar cell can be assessed via its current flow $I = -j_e \cdot A$ (where A is the active area of the cell) as a function of the voltage V at the contacts. This is called the *I-V* curve. It can be derived from the idea that only the minority carriers generated within one diffusion length from the *p/n*-junction live long enough (their minority carrier lifetime) to migrate towards it and to be "saved" as majority carriers on the other side. Thus for the electrical current density $j = I/A$ it follows

$$j = -\int_{-L_h}^{L_e} div\, j_e\, dx \qquad 2\text{-}29$$

Where L_e and L_h are the diffusion length of electrons and holes. The continuity equation for steady state conditions is

$$\frac{1}{q} div\, j_e = G - R = G_L + G_{th} - R \,. \qquad \text{2-30}$$

The recombination rate R is given by

$$R = R_{th} \frac{np}{n_i^2} \,. \qquad \text{2-31}$$

Using equations 2-11 and 2-12, the recombination rate R can be written as

$$R = R_{th} \exp\left(\frac{\varepsilon_{FC} - \varepsilon_{FV}}{kT}\right). \qquad \text{2-32}$$

When this is inserted into equation 2-29 and 2-30 the current is described by

$$j = -q \int_{-L_h}^{L_e} \left\{ G_{th}\left[1 - \exp\left(\frac{\varepsilon_{FC} - \varepsilon_{FV}}{kT}\right)\right] + G_L \right\} dx \,. \qquad \text{2-33}$$

The difference in the quasi-Fermi levels equals the elementary charge multiplied with the voltage at the contacts ε_{FC}-$\varepsilon_{FV} = qV$ and the I-V curve is derived:

$$j(V) = qG_{th}(L_e + L_h)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] - q\int_{-L_h}^{L_e} G_L dx \,. \qquad \text{2-34}$$

Under short circuit conditions the voltage is zero and the short-circuit current density j_{sc} is

$$j_{sc} = -q \int_{-L_h}^{L_e} G_L dx \,. \qquad \text{2-35}$$

Applying a high negative voltage in the dark ($G_L = 0$) leads to the flow of the dark saturation current j_0. Since exp $(qV/kT) \ll 1$, this results in

$$j_0 = qG_{th}(L_e + L_h) \,. \qquad \text{2-36}$$

The generation of carriers in the dark G_{th} can also be expressed by

$$G_{th} = R_{th} = \frac{n^p}{\tau_e} = \frac{p^n}{\tau_h} \qquad \text{2-37}$$

and combination with equations 2-21 and 2-27 leads to

$$j_0 = qn_i^2\left(\frac{D_e}{N_A L_e} + \frac{D_h}{N_D L_h}\right). \qquad \text{2-38}$$

The doping concentration N_D in the emitter is much higher than the doping concentration in the base and therefore this equation can be approximated as

$$j_0 = \frac{qn_i^2 D_e}{N_A L_e} \,. \qquad \text{2-39}$$

Additional to recombination in the base, recombination at the surfaces and in the emitter contribute to the dark saturation current. Recombination in the base and at the rear of a solar cell can be described by

$$j_{0B} = \frac{qn_i^2 D_e}{N_A L_e} \frac{\sinh\left(\frac{W}{L_e}\right) + \frac{SL_e}{D}\cosh\left(\frac{W}{L_e}\right)}{\cosh\left(\frac{W}{L_e}\right) + \frac{SL_e}{D}\sinh\left(\frac{W}{L_e}\right)} \qquad 2\text{-}40$$

where W is the wafer thickness, S the surface recombination velocity and L_e the diffusion length in the base. The front surface and the emitter can be described as one surface with an effective recombination velocity S_{eff}. This results in the emitter dark saturation current density

$$j_{0E} = \frac{qn_i^2 S_{eff}}{N_A}. \qquad 2\text{-}41$$

The total dark saturation current j_0 is the sum of the base current and the contribution of the emitter

$$j_0 = j_{0B} + j_{0E}. \qquad 2\text{-}42$$

Using the expressions for the dark saturation current and short-circuit current the *I-V* curve can also be written as

$$j(V) = j_0\left[\exp\left(\frac{qV}{kT}\right) - 1\right] + j_{sc} \qquad 2\text{-}43$$

which is the ideal diode equation. For open-circuit conditions this results in the expression for V_{OC}

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{j_{sc}}{j_0} + 1\right) \qquad 2\text{-}44$$

because $j(V_{oc}) = 0$. The complete *I-V* curve is illustrated in Fig. 2-4 and the power at maximum power point is described by the product of open-circuit voltage and short-circuit current multiplied by the fill factor (*FF*):

$$P_{mpp} = j_{sc} V_{oc} FF. \qquad 2\text{-}45$$

The efficiency η is defined as the ratio of P_{mpp} and the incident power of photons $P_{photons}$ and is usually measured under standard testing conditions (25 °C, 1000 W/m^2, spectrum AM1.5g[1])

$$\eta = \frac{P_{mpp}}{P_{photons}} = \frac{j_{sc} V_{oc} FF}{1000\, W/m^2} . \quad \text{2-46}$$

Fig. 2-4 illustrates a typical *I-V* curve and the most important solar cell parameters.

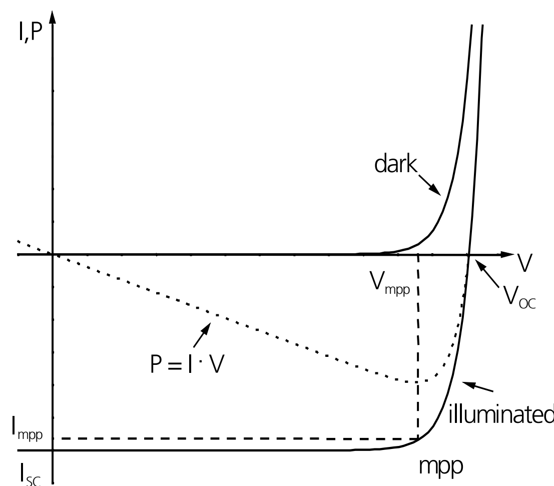

Fig. 2-4: *I-V* curve and power extracted at the contacts of a solar cell. The fill factor can be described as the rectangular area with the largest area inside the *I-V* curve.

Though the ideal diode equation 2-43 takes into account the basic physical principles of charge carrier transport which take place in real devices, silicon solar cells in general can exhibit strong deviations from these ideal characteristics. In a real device a series resistance R_S and a shunt (or parallel) resistance R_P may be present. This is accounted for with the more realistic model shown in Fig. 2-5 where an additional second diode is connected in parallel. This diode models recombination within the space-charge region under the assumption of a single recombination centre in the middle of the forbidden gap and a constant recombination rate across the space-charge region.

[1] AM1.5g is the standard solar spectrum for terrestrial application where the light has passed an air mass of 1.5 times the distance when the sun was overhead. The "g" denotes the "global" spectrum which takes into account direct and diffuse radiation.

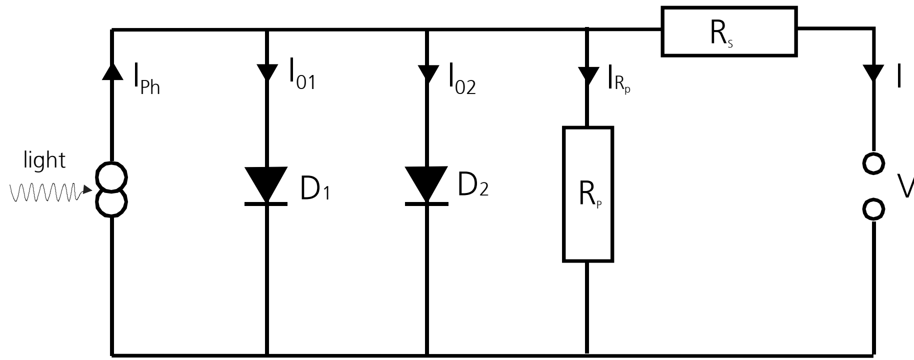

Fig. 2-5: The equivalent circuit of equation 2-47. The second diode models recombination within the space charge region, the series resistance and a shunt resistance account for electrical losses.

The equation for the *I-V* curve is modified to

$$j(V) = j_{01}\left[\exp\left(\frac{q(V - j(V)R_s)}{n_1 kT}\right) - 1\right] + j_{02}\left[\exp\left(\frac{q(V - j(V)R_s)}{n_2 kT}\right) - 1\right] + \frac{V - j(V)R_S}{R_P} + j_L \qquad \text{2-47}$$

where j_L is the current generated by the incident light and $n_1 = 1$ and $n_2 = 2$ represent the diode ideality factors. High values for j_{02} strongly influence the shape of the *I-V* curve (note that j_L is negative!) and can drastically reduce the fill factor. The influence of the series resistance and shunt resistance is plotted in Fig. 2-6. V_{OC} and j_{sc} are only affected for excessive values of R_S and R_P, but the fill factor (and thus the efficiency) is strongly reduced by a high R_S or a low R_P.

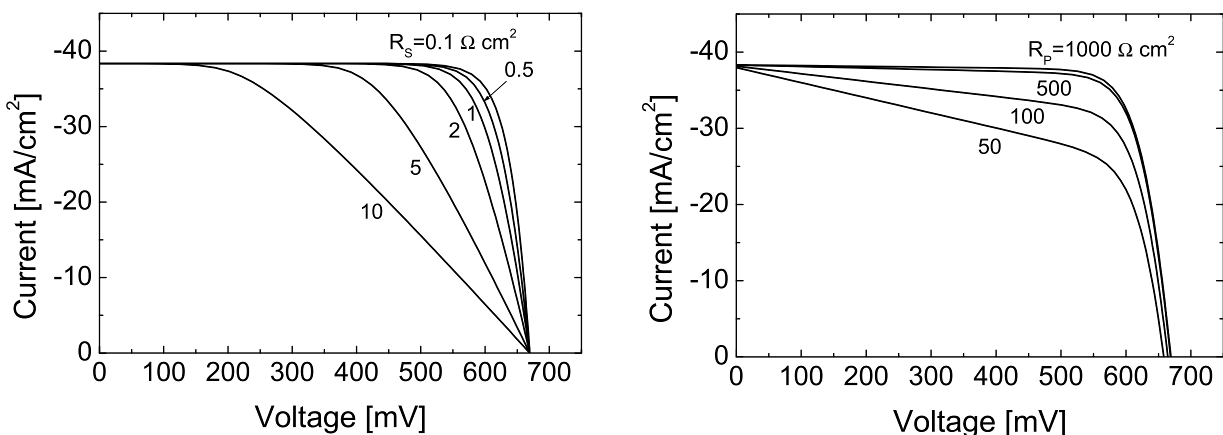

Fig. 2-6: Effect of series resistance (left-hand) and shunt resistance (right-hand) on *I-V* curve. V_{OC} and j_{sc} are only affected for excessive values of R_S and R_P but the fill factor (and thus efficiency) is easily reduced.

Empirically these factors can be fitted to *I-V* curves measured in the dark ($j_L = 0$) to obtain numerical values and to acquire detailed information about the major solar cell loss channels. However, different recombination components may be lumped in numerical fit values of the model parameters j_{01}, j_{02}, n_1, n_2, R_S and R_P. A unique assignment of fit results corresponding to the physical origin of one recombination mechanism is generally difficult.

From the equations discussed above, some important conclusions can be drawn with respect to a maximised solar cell efficiency:

- To maximise the fill factor of a solar cell, the series resistance R_S should be as low as possible whereas the shunt resistance R_P should be as high as possible. Furthermore the dark saturation current j_0 needs to be low.
- The minority carrier diffusion length should be maximised. This requires not only well passivated surfaces but also a high minority carrier lifetime in the bulk (compare 2-40). The result is a low dark saturation current and high values for V_{OC} and j_{sc} (compare equations 2-39, 2-43 and 2-44).

In other words: Not only the cell structure needs to be optimised with respect to optical properties, metallisation and surface passivation. At the same time a high carrier lifetime in the bulk has to be maintained in order to achieve the high effective diffusion lengths necessary for high-efficiency solar cells.

2.3 Loss mechanisms

2.3.1 Optical losses

For a high conversion efficiency, the current which can be extracted from the contacts of a solar cell should be maximised. This requires a high generation rate of electron-hole pairs G_L (see equation 2-34). The necessity of making electrical contact to both *p*- and *n*-type regions of the solar cell usually leads to a contact grid on the side which is exposed to the sunlight (except back contact cells). Since the metal contacts are opaque, this results in shading losses of several percent, independent from wavelength. Light which was not reflected at the contacts strikes the silicon surface. Bare silicon is quite reflective (about 36 % reflectance weighted with the AM1.5g spectrum). A texturing of the surface changes the

geometry of the surface and reflection at a tilted plane towards the cells can enable a second or third chance of an incoming photon to enter the cell. A coverage with one or more dielectric layers can further decrease the reflection losses. Incident light which was not lost via reflection or shading can be absorbed in the bulk. The absorption strongly depends on the wavelength and since silicon is an indirect-gap semiconductor, the absorption probability for low energy photons ($\lambda \geq 1000$ nm) is weak (see Fig. 2-7). Light which was not absorbed within the wafer's thickness, can leave the bulk at the rear or even at the front after internal reflection (Fig. 2-8).

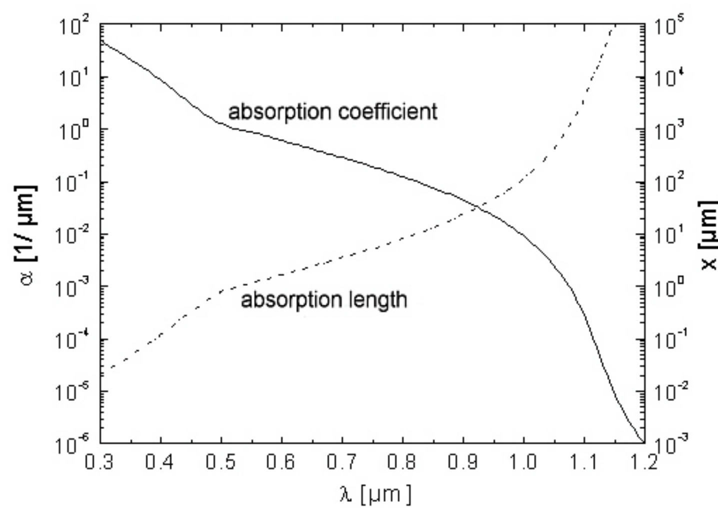

Fig. 2-7: Absorption coefficient and absorption length in silicon. By definition the absorption length is the distance at which the intensity of the incident light is reduced to 37 % of the original power. Short wavelength photons are absorbed within several tenths of micrometers but long wavelength photons ($\lambda \geq 1000$ nm) need several internal reflections before being absorbed within cell thickness [7].

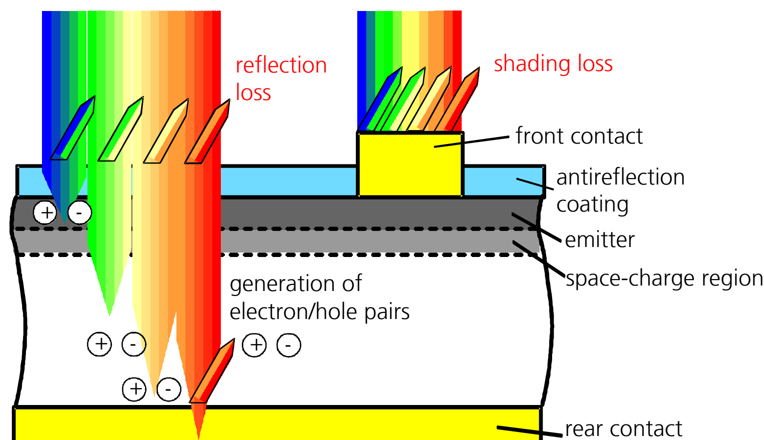

Fig. 2-8: Schematic drawing of a solar cell. The major optical losses are illustrated. Long wavelength photons are reflected at the rear and need internal light-trapping to be absorbed [7].

The described losses mainly influence the short-circuit current density j_{sc} (and V_{OC} via equation 2-44).

2.3.2 Recombination losses

Once the electron-hole pairs are generated by absorption in the silicon, they are exposed to several recombination mechanisms. These processes occur in parallel and the recombination rate is the sum of those for the individual processes.

Radiative Recombination

Radiative recombination is the inverse process of optical absorption. This process is of minor importance in silicon since energy and momentum conservation require the additional participation of a phonon. For the usual doping concentration of about $N_A \approx 1 \cdot 10^{16}$ cm^{-3} radiative recombination is negligible and cannot be influenced by the solar cell design and processing.

Auger Recombination

Auger recombination is described by an electron recombining with a hole which gives the excess energy to a second electron or hole instead of emitting light. This third particle then relaxes back to its original energy by emission of phonons. The characteristic lifetime associated with the Auger process is in general inversely proportional to the square of carrier concentration. In low level injection it is described by:

$$\tau_{Auger} = \frac{1}{C_n N_D^{\;2}} \quad \text{or} \quad \tau_{Auger} = \frac{1}{C_p N_A^{\;2}}. \qquad \text{2-48}$$

Lower doping levels lead to higher limits of the Auger recombination. Therefore the minority carrier lifetime can be influenced by the design of the emitter diffusion and the doping of the base material.

Recombination through traps

Impurities and defects in semiconductors can give rise to allowed energy levels within the forbidden gap. These defect levels create very efficient two-step recombination processes whereby electrons relax from the conduction band to the

defect level and then relax to the valence band, recombining with a hole. The dynamics of this recombination process were calculated by Shockley, Read [8] and Hall [9]. The recombination rate, U_{SRH} for a single defect is given by

$$U_{SRH} = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \qquad 2\text{-}49$$

where τ_{n0} and τ_{p0} are the fundamental hole and electron lifetimes. These are related to the thermal velocity of charge carriers $v_{th} \approx 10^7$ cm/s, the density of recombination defects N_t and the capture cross sections σ_n and σ_p for the specific defect:

$$\tau_{p0} \equiv \frac{1}{\sigma_p v_{th} N_t} \quad \text{and} \quad \tau_{n0} \equiv \frac{1}{\sigma_n v_{th} N_t} \qquad 2\text{-}50$$

n_1 and p_1 are statistical factors defined as follows:

$$n_1 \equiv N_C \exp\left(\frac{\varepsilon_T - \varepsilon_C}{kT}\right) \quad \text{and} \quad p_1 \equiv N_V \exp\left(\frac{\varepsilon_V - \varepsilon_t}{kT}\right) \qquad 2\text{-}51$$

where N_C and N_V are the effective density of states at the conduction band edges, ε_C and ε_G are the conduction band and bandgap energies and ε_t is the energy level of the defect.

The recombination lifetime τ_{SRH} follows from equation 2-20

$$\tau_{SRH} = \frac{\tau_{n0}(p + p_1 + \Delta n) + \tau_{p0}(n + n_1 + \Delta n)}{n_0 + p_0 + \Delta n} \qquad 2\text{-}52$$

with n_0 and p_0 being the equilibrium electron and hole concentrations. The SRH lifetime is a function of the injection level and the doping density as well as the specific defect parameters such as the concentration of traps, their energy level and their capture cross sections. Deep levels with energies close to the middle of the gap are more detrimental recombination centres than shallow levels near the band edges. Technological ways to reduce recombination following the Shockley-Read-Hall mechanism are the avoidance of contamination of the material, the removal of impurities by gettering or the passivation of defect levels.

Recombination at surfaces

Surfaces are rather severe defects in the crystal structure and produce a continuum of allowed states within the forbidden gap. Recombination can therefore occur very effectively via the Shockley-Read-Hall mechanism. The

analysis needs to be reformulated in terms of recombination per unit surface area (rather than unit volume). For a single defect the recombination rate U_S is given by

$$U_S = \frac{n_s p_s - n_i^2}{\dfrac{n_s + n_1}{S_{p0}} + \dfrac{p_s + p_1}{S_{n0}}} \qquad \text{2-53}$$

where n_S and p_S are the concentrations of electrons and holes at the surface. S_{n0} and S_{p0} are related to the density of surface states per unit area N_{tS}. Using the capture cross sections σ_n and σ_p for electrons and holes, S_{n0} and S_{p0} can be written as:

$$S_{n0} \equiv \sigma_{n0} v_{th} N_{ts} \quad \text{and} \quad S_{p0} \equiv \sigma_{p0} v_{th} N_{ts}\,. \qquad \text{2-54}$$

The defect levels at the surface are so numerous that a continuous distribution throughout the bandgap is assumed. Using the interface density of states $D_{it}(\varepsilon)$ and integrating over the entire bandgap results in

$$U_S = \int_{\varepsilon_V}^{\varepsilon_C} \frac{v_{th}\left(n_s p_s - n_i^2\right)}{\dfrac{n_s + n_1}{\sigma_p(\varepsilon)} + \dfrac{p_s + p_1}{\sigma_n(\varepsilon)}} D_{it}(\varepsilon) d\varepsilon\,. \qquad \text{2-55}$$

Similar to the definition of the lifetime, the surface recombination velocity is defined via

$$U_S \equiv S \Delta n_S \qquad \text{2-56}$$

which is typically used for quantifying surface recombination processes.

The two fundamental possibilities to reduce surface recombination are:

- Reduction of the density of interface states. This can be achieved by growing an appropriate dielectric layer like SiO_2 which passivates many of the dangling bonds with oxygen or hydrogen atoms and reduces $D_{it}(\varepsilon)$.
- Reduction of the surface concentration of electrons and holes. Equation 2-53 shows that a reduction of one carrier type can strongly reduce carrier recombination. Minimisation of these therefore reduces recombination. This can be achieved by doping the surface to reduce the minority carrier concentration like in a back-surface-field (BSF). Alternatively, fixed charges in an overlying dielectric layer can be used to hold off either the minority carriers (for a *p*-type wafer negative charges repel free electrons) or in the extreme case invert the surface (large amounts of fixed positive charge invert the surface of a *p*-type silicon wafer). This is also known as field effect passivation, since an electric field is established near the surface.

In reality the methods for reducing surface recombination in actual devices rely on both mechanisms to some extent. The most prominent dielectric layers used to passivate the surfaces in silicon solar cells are thermal oxidation of the silicon surface and a deposited silicon nitride layer. Silicon oxide drastically reduces the interface state density (and additionally contains some fixed charges), silicon nitride mainly passivates via the field effect (in addition to a reduction of interface states). Gradients in the dopant concentration are commonly realised with highly doped regions of phosphorus or boron underneath local contacts or, on an industrial scale, via alloyed aluminium back-surface-fields.

2.3.3 Resistance and shunt losses

Generated carriers which did not recombine and have been separated by the *p*/*n*-junction need to be extracted at the contacts. Non-zero contact resistance and ohmic losses in the metallisation layer lead to power dissipation due to series resistance (see Fig. 2-9).

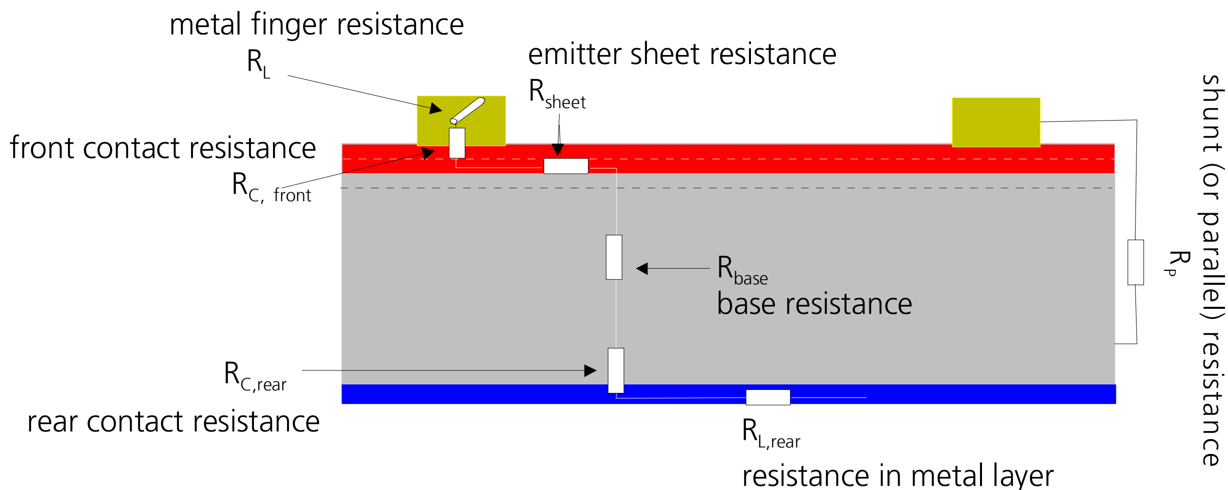

Fig. 2-9: Schematic drawing of a solar cell. To minimise the electrical losses, the series resistance should be as small as possible whereas the shunt resistance should be maximised.

Thus large contact areas and therefore broad contact lines are desirable but this would increase recombination and also the shadowing. The series resistance of the emitter should be low to enable a good current flow towards the contacts. But this requires a highly doped emitter, which in turn increases Auger recombination and surface recombination. The contribution of the bulk resistivity to the series

resistance can be minimised by a higher base doping, which decreases the minority carrier lifetime (Auger recombination) or by a thinner substrate, which decreases the absorption probability for low energy photons. A good compromise between the different loss mechanisms has to be found in a well designed cell structure to find the optimum. The shunting of *n*- and *p*-type regions, for example by excess metallisation around the cell edges should, should be minimised.

A large series resistance decreases the fill factor and even can, if excessive, reduce the short-circuit current. Since under open-circuit conditions the current flow is zero, V_{OC} is not affected. A small value for the shunt resistance also decreases the fill factor and can reduce V_{OC} (see Fig. 2-6).

2.4 Design and processing of high-efficiency silicon solar cells

High-efficiency solar cells can basically be regarded as devices of which the losses are minimised to a very great extent. The PERL (passivated emitter, rear locally-diffused) cell design [10] realises most of the technological possibilities known to date and is sketched in Fig. 2-10.

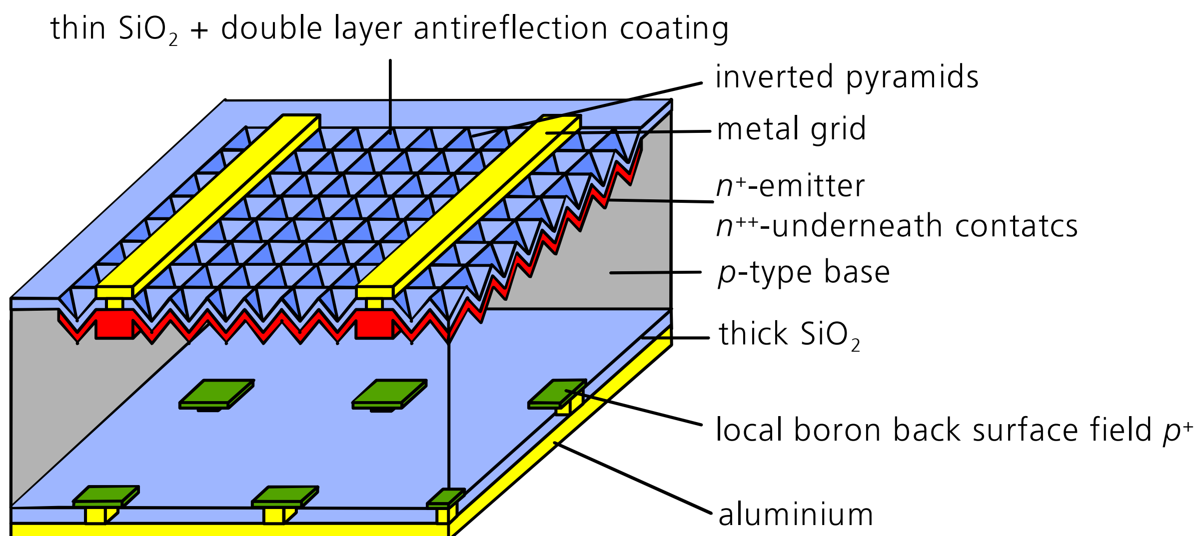

Fig. 2-10: High-efficiency cells structure for monocrystalline silicon solar cells of high material quality.

The features (from front to rear) are:

- Evaporated contacts with a high aspect ratio. The front metal contact is built from an evaporated stack system of titanium, palladium and silver (Ti/Pd/Ag). This thin layer gives a low contact resistivity. For a high grid conductivity the metallisation lines are thickened by electroplating of silver. Usually the lines broaden as they increase in thickness. This can be avoided by guidance of the growth with a structured photoresist layer which allows plating in height only [11]. A high aspect ratio of height/width is achieved and shading losses are minimised.
- Double layer antireflection coating. The use of a double layer coating significantly reduces the primary reflection losses in comparison to a single layer by adjusting thickness and refractive indices to the whole solar spectrum.
- Thin silicon oxide for surface passivation. A thin silicon oxide is thermally grown on top of the emitter. To improve the passivation quality, a thin layer of evaporated aluminium is deposited onto the oxide and annealed at a moderate temperature (≈ 400 °C for about 30 min). It reacts with residual water molecules and atomic hydrogen is released, which migrates to the Si/SiO_2 interface and passivates defects such as dangling bonds. The process is called Al-neal (aluminium anneal) and after the reaction the aluminium layer is etched away in phosphoric acid [10,12,13].
- Inverted pyramid front surface. The surface consists of intersecting <111> planes which were etched using a cross-hatched photolithographically defined mask of silicon oxide. Perpendicularly incident light experiences at least two reflections, i.e. two possibilities to be coupled into the cell. Furthermore the tilted surface leads to a refracted ray path from normal and increases the distance to the rear surface. This improves the absorption probability.
- High dopant concentration under the front contacts. A selective emitter structure is formed in which in the emitter is usually only lightly doped (n^+) to allow for a good surface passivation. Directly underneath the contacts the phosphorus doping is extremely high (n^{++}) in order to minimise contact resistance and recombination at the contacts [14].
- Thick base of high-quality material. A thick wafer (300-500 µm) increases the absorption probability for long wavelength photons. This directly demands a very high minority carrier lifetime to benefit from the increased carrier generation since the carriers need to migrate to the *p*/*n*-junction within their lifetime.

- High dopant concentration under the rear contacts. A local boron diffusion (p^+) underneath the rear contacts minimises the contact resistance and decreases recombination at the contacts [14-16].
- Silicon oxide passivated rear surface. The rear surface is excellently passivated with an Al-nealed oxide. This reduces the rear surface recombination velocity and increases the diffusion length [17].
- Aluminium evaporated onto the silicon oxide. This works as a nearly perfect mirror. Long wavelength photons which were not absorbed so far are reflected and pass the whole wafer for a second time. Together with the textured front this is a very good light-trapping scheme and enables several internal reflections.

For the realisation of such a cell structure, not only many photolithography processes are necessary, but also many high-temperature processes are involved, because usually a silicon oxide mask is required to pattern the surface and mask the local diffusions. Very high efficiencies of $\eta = 24$ % were achieved on this cell structure [10]. A measure to further reduce the shading losses of the front metallisation is a grid design, where the busbars collecting the currents from the grid fingers are laid outside the illuminated area. This measurement condition is denoted as “designated area” measurement and leads to a considerable efficiency gain. Solar cells with essentially the same structure as described above resulted in $\eta = 24.7$ %, the highest efficiency reported to date for a silicon solar cell under one-sun illumination [18,19].

2.5 Application of a standard process sequence to multicrystalline silicon

The features of the cell structure for a high-efficiency device on monocrystalline silicon are well known (see previous section). When trying to produce a high-efficiency solar cell on multicrystalline silicon, one of the first ideas is to apply the processes described in the previous section. This cannot work for the pyramid texture since every grain has a different crystal orientation and thus anisotropic etching methods will not work. A very effective texturing method for

multicrystalline using plasma etching was developed by the author and is described in section 4.3.

With the exception of texturing, all other processes in principle are applicable on multicrystalline silicon. Thus a batch of solar cells with a standard high-efficiency process and a similar solar cell structure as in Fig. 2-10 with many high-temperature oxidations was produced. The minority carrier lifetime of consecutive multicrystalline silicon wafers was monitored on standard wafers of $\rho \approx 1.5\ \Omega$ cm produced by the company ScanWafer. Starting with seven lifetime monitoring wafers after each high-temperature process one wafer was removed from the batch and all diffused or oxidised layers were etched away. After surface passivation with silicon nitride quasi-steady state photoconductance (QssPC, see Appendix A2) was measured on four spots on every wafer and arithmetically averaged. The results are shown in Fig. 2-11. The minority carrier lifetime which started on a high average level of $\tau \approx 50$ µs (which corresponds to a diffusion length of $L_e \approx 380$ µm), was strongly reduced by an oxidation at 1050 °C for two hours.

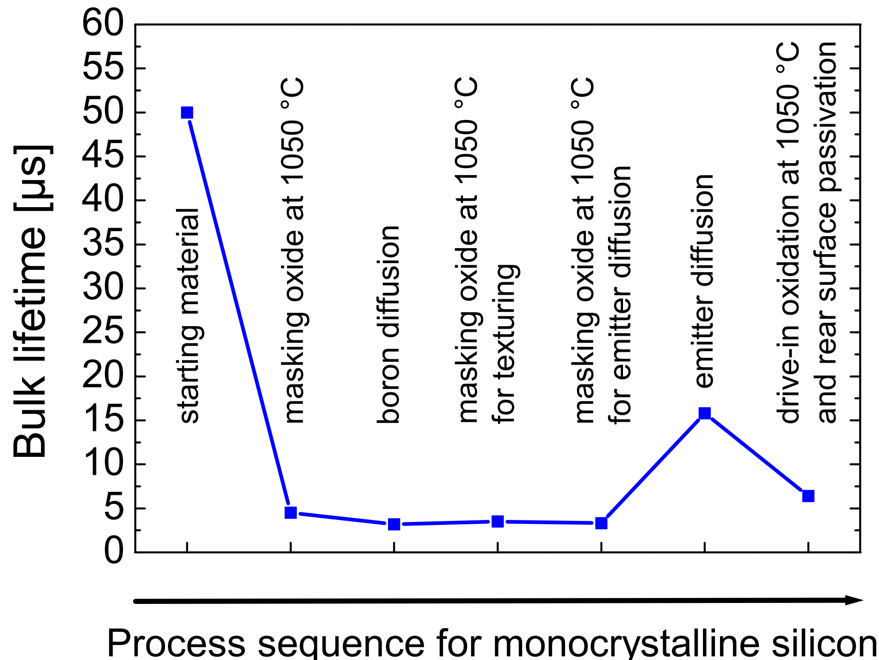

Fig. 2-11: Minority carrier bulk lifetime of multicrystalline silicon wafers in a standard high-temperature process sequence designed for monocrystalline silicon. All diffused or oxidised layers were etched away and the surfaces were passivated with silicon nitride. The measurements were taken on four spots on every wafer with the QssPC method at $\Delta n = 1 \cdot 10^{15}$ cm^{-3} and arithmetically averaged. Oxidation at 1050 °C led to a severe degradation which was only partly recovered by the emitter diffusion.

During further high-temperature processes, the material did not recover, with the exception of the emitter diffusion. This phosphorus diffusion at 790 °C improved the carrier lifetime, but not to the initial value. The last oxidation for emitter drive-in and surface passivation again degraded the material to very low values. Additionally multicrystalline wafers were processed which were only exposed to one high-temperature process or a short sequence. The results are displayed in Fig. 2-12.

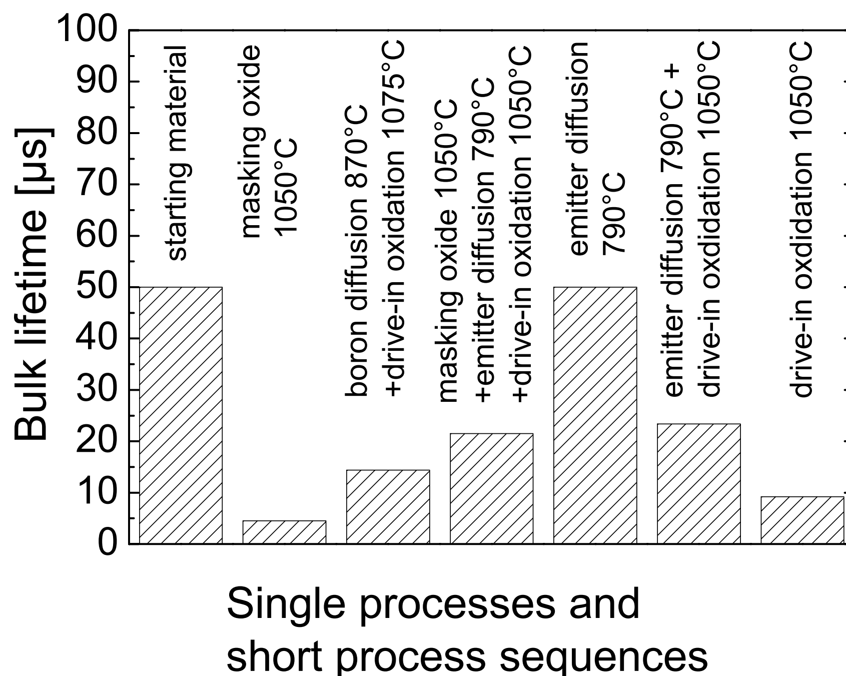

Fig. 2-12: Minority carrier bulk lifetime of multicrystalline silicon wafers after different high-temperature processes and short process sequences. All diffused or oxidised layers were etched away and the surfaces were passivated by silicon nitride. The measurements were taken on four spots on every wafer with the QssPC method at $\Delta n = 1 \cdot 10^{15}$ cm^{-3} and arithmetically averaged. Every single high-temperature process except for the emitter diffusion led to a significant lifetime degradation in multicrystalline silicon. When a diffused layer was present during drive-in oxidation, the degradation was reduced.

Also every single high-temperature oxidation is harmful and significantly decreases the material quality. When diffused layers are present on the wafer during drive-in oxidations, the degradation is reduced, probably due to in-situ gettering.

The observed minority carrier lifetime degradation by high-temperature processes was reported in literature by several authors [20-24]. However, one exceptional result was presented by Zhao et al. [25,26] who applied the PERL

process sequence (compare section 2.4) with several oxidations at temperatures of about 1050 °C and an adjusted isotropically etched front surface on very clean material from the company Eurosolare. On an area of 1 cm^2 an efficiency of $\eta = 19.8$ % was published. It was reported by Green [27] that after completed processing the material consisted of regions of very good and very poor quality areas and that scatter of cell performance was large. Similar results were observed by the author of this thesis with locally resolved lifetime measurements taken with the Carrier Density Imaging technique (CDI, see Appendix A4) as shown in Fig. 2-13. The image on the left-hand exhibits many areas of high material quality. A neighbouring wafer with the same crystal structure was oxidised for one hour at 1050 °C. It revealed a severe degradation in most areas, only some small regions could maintain their high minority carrier lifetimes. This explains why it is possible to produce solar cells with high efficiencies on small areas with the standard high-temperature processing. But in principle the material quality is severely degraded.

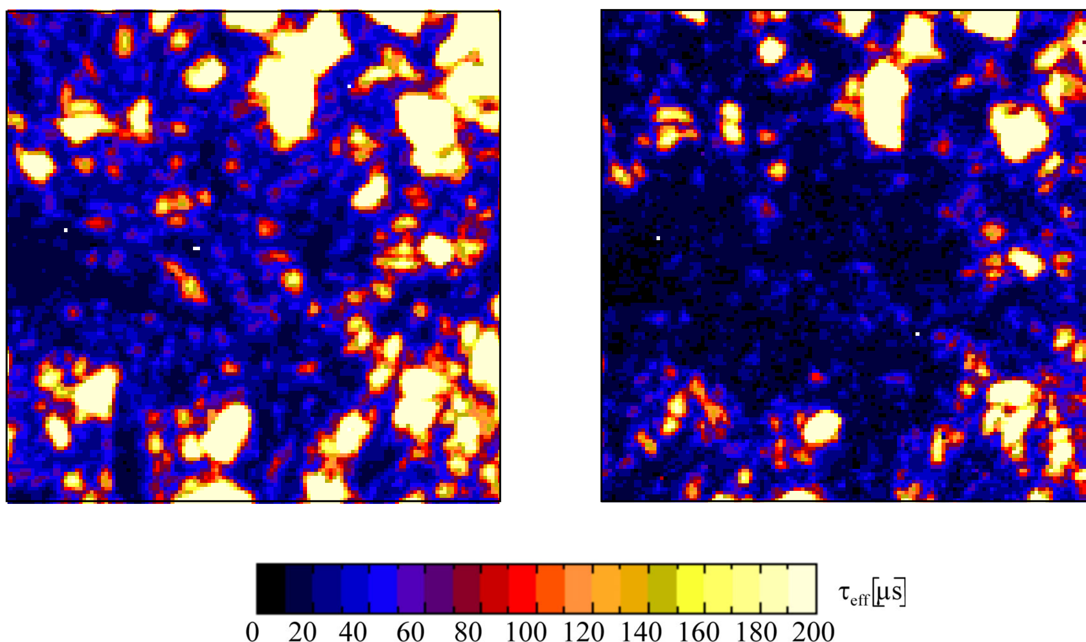

Fig. 2-13: Bulk lifetime of multicrystalline silicon wafers passivated with silicon nitride. The starting material (left-hand) has many areas of high lifetime and some medium quality areas. Even one oxidation for one hour at 1050 °C led to severe degradation on a neighbouring wafer in most regions, only some grains could preserve a high minority carrier lifetime (right-hand).

Solar cells were produced with nearly the same process sequence as described in Fig. 2-11 (using an additional n^{++}-diffusion underneath the front contacts). The results corresponded well to the lifetime measurements: The highest efficiency on a 1.5 Ω cm multicrystalline wafer of 4 cm^2 size was only 15.6 %. In a previous attempt 16.2 % had been achieved with a full process sequence for a PERL-cell by Knobloch [28]. These low efficiencies are explained by the strongly reduced material quality of the multicrystalline silicon after the oxidations at 1050 °C. Therefore this high-temperature route was not followed any further.

2.6 Chapter summary

The basic equations of solar cell physics clearly state a strong dependence of solar cell performance on the effective minority carrier diffusion length. In order to maximise this parameter and this way the cell efficiency, two conditions need to be fulfilled simultaneously: A high-quality cell structure with very well passivated surfaces and low electrical losses has to be produced without degrading the material quality. The best solar cells produced so far were exposed to many high-temperature processes during fabrication. This is no problem for high-quality monocrystalline material, but defect-rich multicrystalline silicon in general severely degrades at such high temperatures.

The challenge is the development of a cell structure which can be produced with processes which do not degrade multicrystalline silicon. At the same time the loss mechanisms need to be suppressed as much as possible. This topic is addressed in this thesis.

3 Gettering and thermal degradation of multi-crystalline silicon

3.1 Introduction

The efficiency of a solar cell is determined by many parameters, for example surface and bulk recombination, optical properties and electric contacts. This chapter deals with the minority carrier lifetime in the bulk of a solar cell. The first part is focussed on the increment of lifetime during phosphorus gettering and aluminium-phosphorus co-gettering. Furthermore the lifetime-degrading process of thermal oxidation is investigated for temperatures of 1050 °C and 800 °C. The relevant parameters are optimised with respect to a maximised minority carrier lifetime.

In the second part, a microscopic model is discussed to explain the results. This analysis concentrates on the lifetime improvement by phosphorus gettering and on the degradation during high-temperature oxidation at 1050 °C.

3.2 Optimisation of process parameters for gettering and oxidation

One important technology in connection with solar cells from multicrystalline silicon is the gettering of impurities. In general, gettering is a three-step process which removes unwanted impurities from the active regions of a device and traps them in defect-containing regions or in zones where their solubility is enhanced [29]:

1. Impurities must be released from their original state to become mobile.
2. The impurities need to diffuse through the crystal.
3. The impurities have to be captured at the gettering site.

Two basic classes of gettering processes are defined by their capture mechanism: relaxation and segregation. In a relaxation technique, precipitation sites are intentionally formed far away from the active device region. This process

works with an impurity supersaturation which occurs during cooling from high temperature and causes the precipitation of the impurities. In a segregation gettering process, a region of higher solubility is utilised to extract impurities from a region of lower solubility. Since no supersaturation is required, low impurity concentrations can be obtained, provided that the gettering layer has a sufficient capacity to absorb the impurities.

In a solar cell, the entire wafer is the active region. Carrier recombination in a highly doped layer is enhanced anyway resulting in a reduced sensitivity to impurities. Thus gettering into the front layer (emitter) or back layer (back surface field) of the solar cell is an appropriate technique. Furthermore this allows the gettering layer to be etched away if necessary. This would remove the impurities permanently. Phosphorus gettering and aluminium-phosphorus co-gettering are investigated as they can provide the emitter and a contact on a *p*-type base, both being vital necessities in a solar cell.

3.2.1 Phosphorus gettering

Gettering of impurities by heavy phosphorus diffusion is a well known measure to increase the carrier lifetime in contaminated silicon. Phosphorus gettering by $POCl_3$ is especially effective since it provides a number of potential mechanisms for gettering [29,30]. The very high phosphorus concentration at the surface ($\approx 10^{21}\text{cm}^{-3}$) leads to SiP precipitate formation. These precipitates create gettering sites and contribute to the injection of self-interstitials in excess which can enhance the mobility of impurities. However, the gettering mechanisms of phosphorus diffusions are still poorly understood and a subject of ongoing research [31,32].

An ideal phosphorus gettering process would yield a high carrier lifetime and a heavily doped layer for the contact region of a solar cell with selective emitter design. For these purposes emitter diffusions resulting in a sheet resistance of 10-20 Ω/sq. were optimised to obtain the highest possible minority carrier lifetime. Eight phosphorus diffusions were performed on standard multicrystalline material with a base resistivity of about 1.5 Ω cm produced by the company ScanWafer. The wafers were diffused in a tube furnace with a $POCl_3$ source with the temperature profiles given in Table 3.1. The phosphorus layers were etched away

and after a cleaning process the surfaces were passivated with silicon nitride to suppress surface recombination. The effective lifetimes were measured with the QssPC method on eight spots on every wafer of 125 mm·125 mm size. The arithmetically averaged results at an injection level of $\Delta n = 1 \cdot 10^{15}$ cm^{-3} are reported in Table 3.1.

Table 3.1: Gettering experiments with heavy phosphorus diffusion on both sides. The reference wafer without diffusion had an effective carrier lifetime of 39 µs. The reported lifetimes were measured at an excess carrier density of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}.

	900°C		880°C		860°C	
time [min]	R_{sheet} [Ω/sq]	τ_{eff} [µs]	R_{sheet} [Ω/sq]	τ_{eff} [µs]	R_{sheet} [Ω/sq]	τ_{eff} [µs]
60	16	110				
75	14	94				
90	13	107	17	104		
105			16	112		
120			16	110		
165			12	113		
300					14	135

The reference value of a neighbouring wafer without diffusion was 39 µs. The emitter sheet resistance was below 20 Ω/sq for all diffusions. The evaluation revealed that a big improvement in carrier lifetime from $\tau_{eff} = 39$ µs of the reference wafer to about $\tau_{eff} \approx 100$ µs was observed for all diffusions. However, no significant difference between the processes was observed in the case of 900 °C and 880 °C. For 860 °C there seems to be a slight advantage compared to the higher temperatures, but the applied process lasted for five hours. This time was considered to be too long. No further parameters were investigated, especially since the achieved level of more than 100 µs bulk lifetime was sufficient to produce high-efficiency solar cells. Spatially resolved measurements using the CDI

technique neither revealed any significant difference in the material under investigation. The same pattern of lifetime improvement (compare section 3.3) was observed for all wafers indicating that every applied process was sufficiently effective in removing impurities where possible. Special treatment like a prolonged waiting time at a low temperature during ramp-down, as successfully used by Härkönen et al. [33] (14 hours at 700 °C), was not applied because of the long process time. Furthermore the achieved minority carrier lifetimes in that experiment were still significantly below the results of the study presented here.

3.2.2 Aluminium-phosphorus co-gettering

Another approach to obtain a clean bulk for a solar cell is gettering with aluminium. The aluminium is deposited as a full area layer on the rear of a standard solar cell design by screen printing, pad printing, evaporation or sputtering. Afterwards it is annealed at a process temperature above the Al/Si eutectic temperature (577 °C). This produces a molten Al/Si layer in which the solubility of metallic impurities is much higher than in the wafer bulk[2]. Aluminium gettering is well understood in terms of segregation and is widely employed in silicon solar cell processing. However, it is often only a by-product of back-surface-field formation.

In this study, a technique was chosen in which a two micrometer thick layer of evaporated aluminium was deposited on the rear of a solar cell before phosphorus diffusion. Front phosphorus and rear aluminium diffusion happened simultaneously, therefore this process is called co-diffusion. Two time/temperature profiles were chosen (4 hours/880 °C and 1½ hours/900 °C) to achieve a highly doped emitter. At the same time an aluminium gettering layer at the rear was formed which passivates the surface.

Plekhanov et al. [34] modelled the gettering of precipitated iron. They found that the highest gettering efficiency should be achieved with a ramped process starting at a high temperature in order to dissolve the precipitates followed by a multiple step ramp-down process. The time at each gettering step has to be increased as the temperature decreases because of the reduced mobility of the impurities at lower

[2] Aluminium possesses a solubility of 1-10 at.% for many metals including Fe, Cu, Ni, and Au [29].

temperatures. In order to test whether the suggested method increases the effectiveness of the co-gettering process, loading and unloading of the tube was varied. It either took place at 700 °C (followed by a ramp-up and ramp-down to/from the plateau temperature at 2 K/min = slow) or directly at the diffusion temperature (ramps as fast as possible = fast).

After the diffusion, all layers were thoroughly etched away in a wet-chemical solution. After a further cleaning procedure a PECVD silicon nitride layer was deposited to passivate both surfaces. The measurement of the effective minority carrier density with the QssPC method revealed an increase of the carrier lifetime compared to the reference sample (Fig. 3.1).

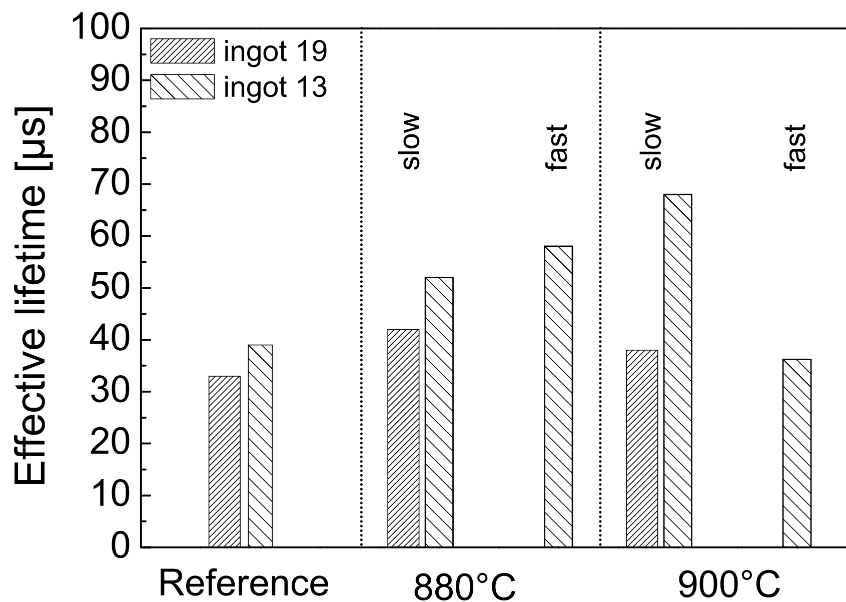

Fig. 3.1: Gettering experiment with a heavy phosphorus diffusion on one side and a two micrometer thick aluminium layer on the other. Effective lifetimes were measured with the QssPC method ($\Delta n = 1 \cdot 10^{15}$ cm^{-3}) after removal of the diffused layers and surface passivation with silicon nitride.

This was due to the successful removal of impurities. The impact of the diffusion temperature and of the different ramp-up and ramp-down profiles is not evident. For the wafers of ingot 13 the fast ramps with the 880 °C plateau temperature resulted in higher lifetimes than the slow ramps. At 900 °C it was the other way round. For the wafers of ingot 19 the co-gettering process at 900 °C with the slow ramps, which gave the best results for the wafers of ingot 13, was ineffective. More

data would be necessary to enable an explanation of the results. But the experimental investigation of the co-gettering technique is much more complicated than phosphorus diffusion gettering: The diffused aluminium layer and the aluminium silicide have to be completely etched away for reliable minority carrier lifetime measurements. This bears the risk of contamination of equipment with residual aluminium. As the beneficial effect even of the best of these gettering sequences was below the pure phosphorus gettering (see previous section), which is the much easier process, the aluminium-phosphorus co-geterring path was not followed any further.

Riepe et al. showed in [35] for vertical cut wafers, that the efficiency of the gettering treatment with a similar recipe was very effective especially in the bottom part of the investigated block cast material. This is explained by the material properties like the distribution of iron and oxygen [36] or the crystal quality [31] which vary within the height of the ingot. The material investigated in this study was already rather clean ($\tau_{bulk} \approx$ 30-40 µs) and therefore did not need a special gettering treatment, a fact greatly appreciated since this facilitates the manufacturing of high-efficiency solar cells.

3.2.3 Plateau temperature of oxidation

The competing effects of gettering, the dissolution of precipitated impurities and their spreading in the bulk, also need to be controlled by process design. Several authors have investigated thermal oxidation of multicrystalline silicon (e.g. [31,37,38]) and it is common opinion that a temperature of 1050 °C leads to a drastic degradation of minority carrier lifetime and therefore forbids the application of such a high-temperature process step (compare section 3.3). In most cases the upper limit, below which no degradation is observed, was found around 900 °C [37,38]. Nevertheless, at this temperature also degradation was reported, especially for low resistivity material [39].

In a study presented in section 5.4, multicrystalline silicon of 1.5 Ω cm was oxidised for emitter drive-in and simultaneous oxidation of the rear. Hardly any degradation of the bulk lifetime was observed for temperatures of 800 °C, 850 °C and 900 °C although the oxidation lasted for four hours. In those experiments a

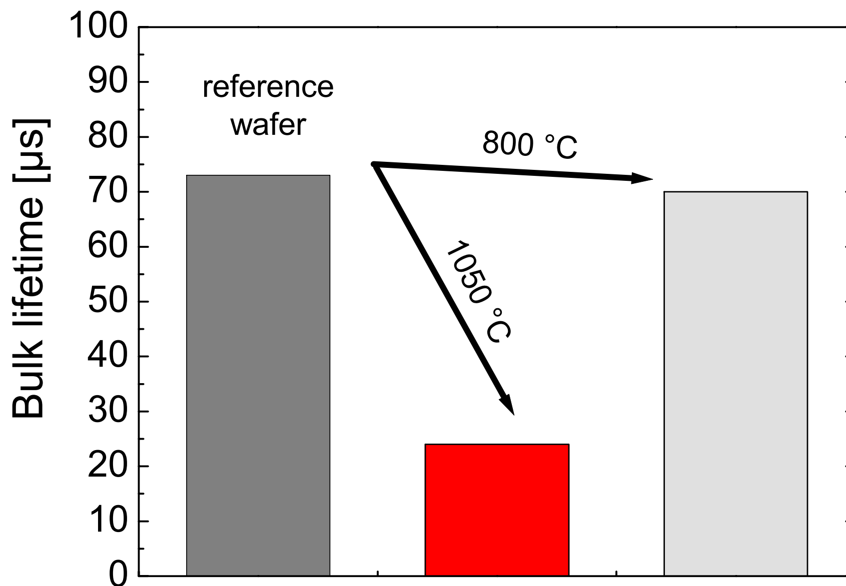

Fig. 3.2: Bulk lifetime of standard quality multicrystalline silicon of neighbouring wafers after thermal oxidation for one hour at 1050 °C and four hours at 800 °C respectively. Measurements were performed with the QssPC technique at an excess carrier density of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}.

phosphorus layer was present during the oxidations. In a different set of samples without prior emitter diffusion the bulk lifetime of neighbouring wafers was measured after an oxidation for four hours at 800 °C and one hour at 1050 °C (see Fig. 3.2). The oxide layers were etched away and the surfaces were passivated with silicon nitride. Again a severe degradation was observed in the case of the 1050 °C oxidation whereas at 800 °C no significant lifetime deterioration was observed. Although the oxidation temperature might be increased up to about 900 °C without degradation, bearing the benefit of a significantly reduced oxidation time (see section 6.2.1), for further experiments the process at 800 °C was applied. This choice was motivated by the exponential dependence of the reaction velocity on temperature. Thus, at low temperatures dissociation processes of metal clusters are expected not to be activated and a low mobility of impurities should limit their migration throughout the wafer. In other words: A prolonged time should be less harmful than an elevated temperature. Therefore higher impurity levels in the multicrystalline silicon might be tolerable. Furthermore low resistivity material can be used which allows the application of the same process to all kinds of multicrystalline silicon.

3.2.4 Heat-up and cool-down ramps of oxidation process

Apart from the maximum plateau temperature of a high-temperature process, the ramps to reach it and to cool down to room temperature can significantly influence the quality of the material. The explanation is the exponential dependence of the diffusivity and solubility of impurities on temperature which also causes the quick supersaturation when the sample cools down. Thus, the temperature profile during cooling (both during crystal growth and subsequent processing) has a strong impact on the final distribution and chemical state of the impurities in multicrystalline silicon [40] and can have a strong impact on the solar cell efficiency [41].

Two different processes were investigated which both have a high practical relevance: dry oxidation for one hour at 1050 °C and wet oxidation for four hours at 800 °C. Both result in oxide thickness on *p*-type material ($\rho = 0.5–10\ \Omega$ cm) of about 100-120 nm (depending on crystal orientation). Two ramping profiles were applied, one called “fast” (but no quench) and one called “slow” to cool down the samples to room temperature. Standard multicrystalline silicon produced by ScanWafer was used. The oxidised layer was etched away and the surfaces were passivated with silicon nitride. Effective lifetimes were measured with the QssPC method at an injection level of $\Delta n = 1 \cdot 10^{15}$ cm^{-3} and arithmetically averaged (see Fig. 3.3). Due to the excellent surface passivation [42], the effective lifetimes represent the bulk lifetime of the multicrystalline silicon in very good approximation. The plateau temperature had a decisive influence on the observed degradation (as already shown in 3.2.3) and the process temperature of 1050 °C was far too high. There was no significant difference for the two ramps which could be derived from the QssPC measurements. In the case of the 800 °C oxidation, the influence of the ramps was pronounced. The slow ramp could maintain the high lifetime whereas the fast ramp led to a significant reduction of the minority carrier lifetime.

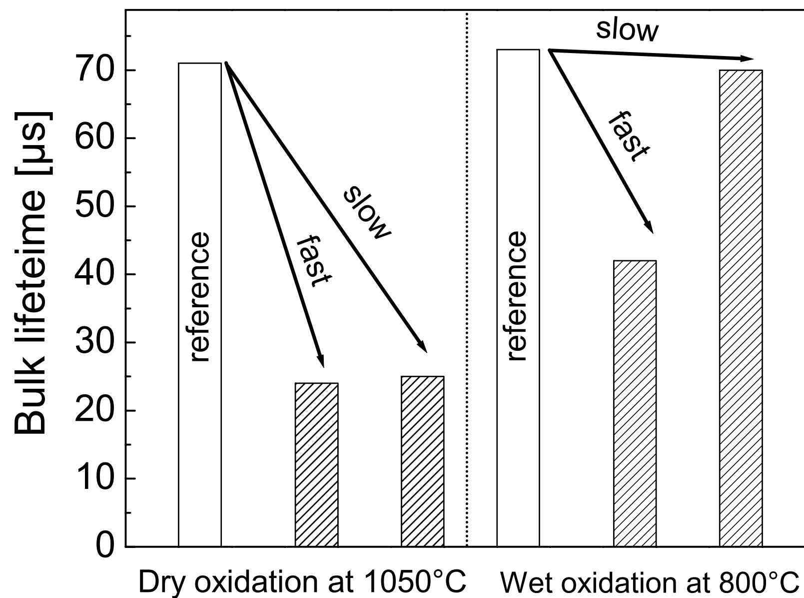

Fig. 3.3: Bulk lifetime measured with the QssPC method at an injection level of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}. The plateau temperature and the ramping profiles have a significant influence on the bulk lifetime.

For further investigation small areas of 14·14 mm^2 were measured with the CDI technique with a high spatial resolution (50·50 µm^2). The images are shown in Fig. 3.4. The areas were marked with a laser (eight points in the outer area, visible in the form of low lifetime spots due to the introduced surface damage) allowing the tracing of specific regions of interest throughout the neighbouring wafers. Two reference wafers were selected as close as possible to the wafers which were oxidised in order to have the same crystal structure. For the 1050 °C oxidation the fast ramp led to more homogeneous low lifetime regions than the slow ramps. One explanation would be a widespread nucleation of impurities during fast cooling because they could not diffuse to the preferred nucleation sites (highly dislocated areas and grain boundaries as suggested by Buonassisi [40]). However, after the 800 °C oxidation the opposite was be observed: the fast ramps led to a more coarse grained structure of high and low lifetime areas than the slow ramps. In the middle of the good grains the lifetime was even slightly increased. But: the slow ramps hardly showed any difference in lifetime compared to the reference sample, i.e. degradation was effectively suppressed.

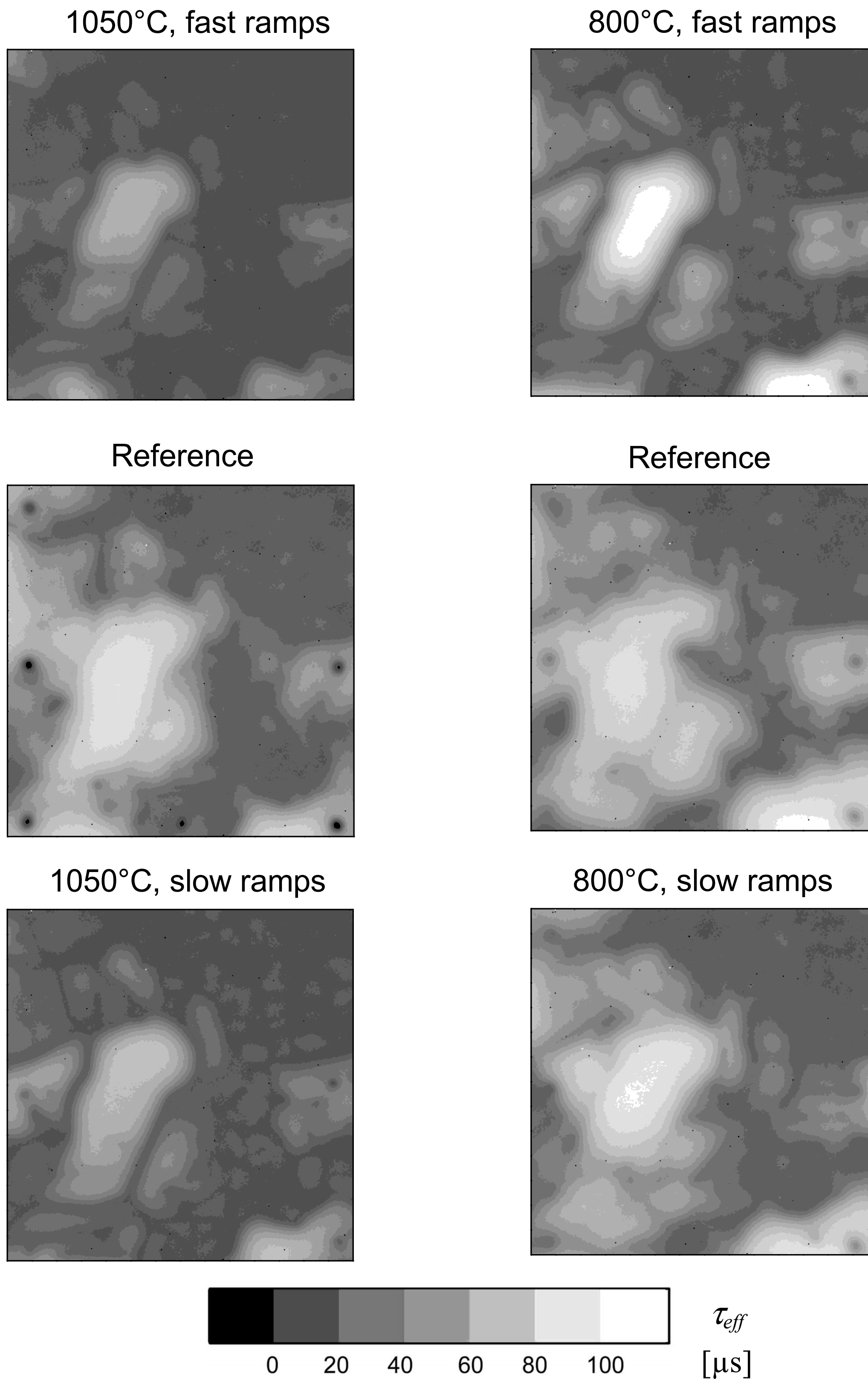

Fig. 3.4: CDI images of oxidised samples after 1050 °C dry oxidation (left column) and 800 °C wet oxidation (right column). The samples have a size of 14·14 mm^2. The row in the middle shows the carrier lifetime of reference samples without thermal treatment, the black dots at the edges are laser marks.

One explanation for the observed results would be a different amount and mobility of the impurities which are dissolved from the dislocations and grain boundaries during the time at the plateau temperature. In the case of 1050 °C much more impurities are expected to dissolve and even those with low mobility could diffuse throughout the bulk due to the high temperature. At 800 °C plateau temperature only a small fraction of impurities is dissolved and only those with high mobility can diffuse a significant distance at this temperature. If then the ramps are sufficiently slow the impurities have enough time to diffuse back to the preferred sites from which they were dissolved whereas for the fast ramps they precipitate at the place where they are when the cool-down starts. However, without a more detailed investigation using methods which can identify the chemical state and the type of impurities affecting the minority carrier lifetime (like μ-XRF and μ-XAS [40]) such explanations remain speculation although they fit well to existing knowledge. A more detailed study including the local dislocation density in the multicrystalline silicon is presented in the next section.

3.3 Reasons for the changes of carrier lifetime by high-temperature processes

High-temperature processes like oxidations and diffusions are state-of-the-art techniques for the production of high-efficiency silicon solar cells. They hardly have any influence on high-purity monocrystalline silicon, but strongly affect the carrier lifetime when applied to solar grade multicrystalline silicon. In the following the change of carrier lifetime after phosphorus diffusion at 790 °C and 880 °C and oxidations at 1050 °C is further investigated. The reason for the beneficial impact of the phosphorus diffusion is known to be the reduction of mobile impurities. However, it will be shown that the efficiency of this gettering process is not homogenous all over the wafer but particularly pronounced in areas of low dislocation densities. As seen above, in contrast to the beneficial effect of the phosphorus diffusion the oxidation at 1050 °C has a detrimental impact on minority carrier lifetime. This is suggested to be at least partly due to an increase in dislocation density. A microscopic model which explains the results is discussed. Combining oxidations and diffusions and analysing the change in minority carrier

lifetime, conclusions on the processing conditions suitable for high-efficiency solar cells made from solar-grade multicrystalline silicon are derived. The measurements on a "macroscopic" level were performed by injection-dependent lifetime spectroscopy (IDLS) [43] on spot sizes of about 11 cm^2 with the QssPC method (see Appendix A.2). For investigations on a "microscopic" level, a higher resolution of about 50·50 μm^2 was achieved with the Carrier Density Imaging (CDI) technique (see Appendix A.4). Additionally, spatially resolved measurements of dislocation density were performed for some samples [44].

3.3.1 Experimental procedure

All phosphorus diffusions discussed in this thesis were carried out in a tube furnace with a $POCl_3$ source. The first type of diffusion was performed at 790 °C for one hour to get a lightly doped emitter which, after subsequent drive-in oxidation, resulted in a sheet resistance of about 120 Ω/sq. This emitter was optimised for a solar cell design with homogeneous emitter and evaporated contacts and will be referred to as "emitter diffusion". The second type of diffusion was performed at 880 °C for two hours. One hour a deposition of P_2O_5 took place and the second hour was a drive-in diffusion. It resulted in a sheet resistance of about 16 Ω/sq. This is a good emitter for the contact region of a solar cell design with selective emitter. At the same time this procedure acts as a strong gettering process (see 3.2.1). Therefore it will be denoted "gettering diffusion" in the following. The thermal oxidations were carried out at an elevated temperature of 1050 °C for one hour with the addition of dichloroethylene (DCE). No external contamination was introduced during this process. This was monitored on high-purity monocrystalline FZ silicon reference samples whose minority carrier lifetime was not decreased.

The samples were selected from the centre region of a solar-grade multicrystalline silicon ingot of about 1.5 Ω cm resistivity. They were cut in consecutive order and the saw damage was removed with an acidic wet-chemical bright etch. Before all high-temperature processes, a cleaning procedure was applied to reduce the risk of external contamination. After the diffusion processes, all samples were etched again. This way all diffused layers were completely

removed and all samples had the same surface conditions. To enable the precise extraction of the bulk lifetime, the surfaces were again cleaned and passivated with a high quality silicon nitride layer using Plasma Enhanced Chemical Vapour Deposition (PECVD) at 350 °C [42]. The measured effective lifetime on the reference samples was in the range of one millisecond.

Dislocations in silicon are an important material property that can have a significant impact on the carrier lifetime and on the electrical properties of silicon devices. For dislocation density measurements areas of $15 \cdot 15\ mm^2$ were cut out and chemo-mechanically polished on the front side. Dislocations and grain boundaries cause a crystal defect and the lattice is distorted. Special etching solutions can be applied which preferentially attack the silicon at these sites.

In this study the crystal defects were revealed by treating the sample with a Secco etch [45] until the piercing points of the line dislocations with the plane resulted in etched moulds of about 0.4 µm diameter. Grain boundaries appeared as lines. Thus every dislocation line resulted in a small etch pit which were observable with an automated optical microscope (see Fig. 3.5).

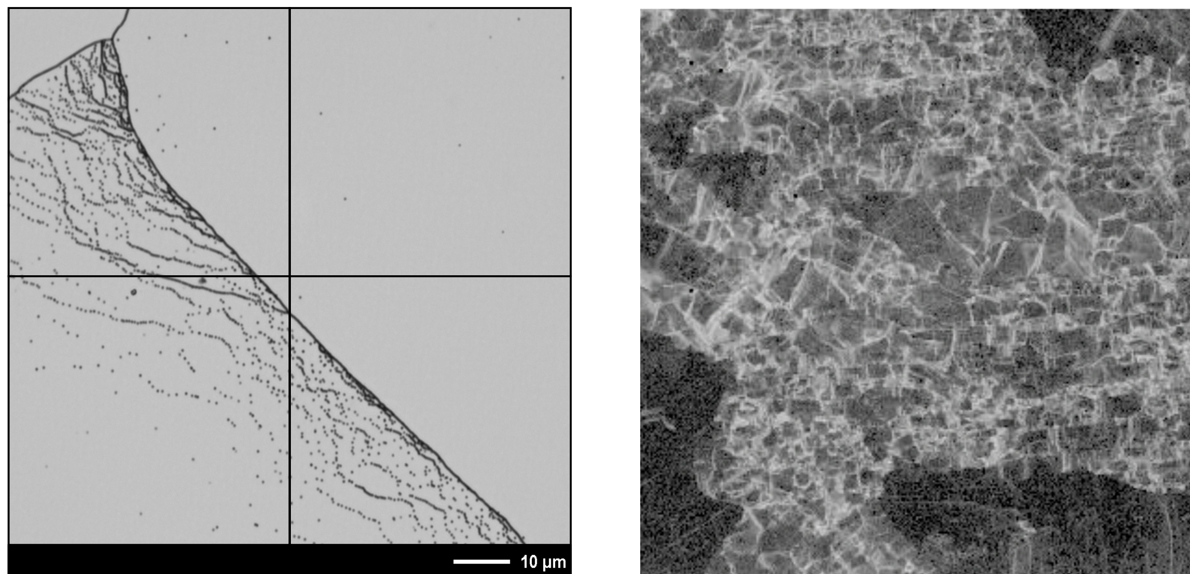

Fig. 3.5: An optical microscope picture of the wafer surface after Secco etch can be seen on the left-hand side. The etch pits are counted with an automated imaging analysis software and the etch pit density (EPD) is calculated for every region of $50 \cdot 50\ \mu m^2$ (solid lines). These local values of the EPD build the 300·300 pixel matrix for the image on the right-hand side.

For Etch Pit Density (EPD) analysis in $50 \cdot 50\ \mu m^2$ regions of interest objects were automatically counted and classified by using an image analysis software [44]. The

local EPD was calculated by taking into account all objects classified as "single etch pits" and "single etch pits in small clusters". Thus, the final EPD map consists of 300·300 pixels representing the dislocation density. Grain boundaries were not considered[3].

3.3.2 Average minority carrier lifetime measurements

Two areas A and B were chosen differing in grain size and lifetime. Area A consisted of large grains and showed an initial lifetime of about 52 µs, area B had comparatively small grains and an initial lifetime of 43 µs (see No. 1 in Table 3.2).

Table 3.2: Matrix of performed experiments and measured effective lifetimes in two areas for every wafer.

No.	processing sequence	area A	area B
1	Reference (no thermal treatment)	52 µs	43 µs
2	Emitter diffusion 790 °C	131 µs	87 µs
3	Gettering diffusion 880 °C	184 µs	104 µs
4	Oxidation 1050 °C	27 µs	22 µs
5	Emitter + Oxidation	39 µs	29 µs
6	Gettering + Oxidation	59 µs	35 µs
7	Oxidation + Emitter	93 µs	55 µs
8	Oxidation + Gettering	72 µs	48 µs
9	Oxidation + Emitter + Oxidation	25 µs	21 µs

The effective lifetime of the samples was measured in the two areas A and B at an injection level of $\Delta n = 1\cdot10^{14}$-$1\cdot10^{16}$ cm^{-3} for every wafer on an area of about 11 cm^2. Misalignment of the wafers was prevented by laser marking of the areas and the use of a ruler on the measurement table. The reported values were read out

[3] The dislocation density measurements were performed by Stephan Riepe from Fraunhofer ISE.

at $\Delta n = 1 \cdot 10^{15}$ cm^{-3} to ensure that the lifetime data was not affected by trapping effects. Unless stated, all reported lifetime values were measured after storage of the samples in the dark for at least 12 hours to ensure reproducible measurement conditions with respect to a possible iron contamination [46]. Due to the excellent surface passivation of the samples ($S \approx 10$ cm/s) the measured effective lifetimes represent the bulk lifetimes in very good approximation. The emitter diffusion (No. 2) has a beneficial impact and leads to a more than doubled minority carrier lifetime (see Table 3.2 and Fig. 3.6).

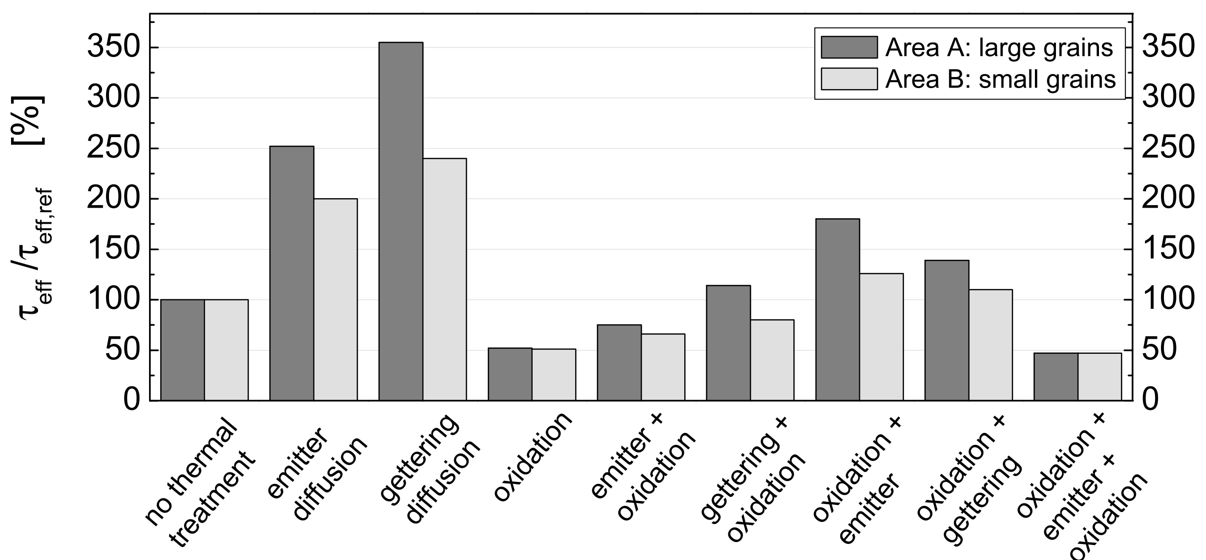

Fig. 3.6: Effect of high temperature processes on the recombination lifetime of the two distinct areas on every wafer. The values are normalised to the reference without thermal treatment.

This was observed for both investigated areas. The effect was stronger in area A, where the crystal structure contained larger grains. In the case of the gettering diffusion (No. 3) this was even more pronounced. The oxidation (No. 4) diminished the measured lifetime for both areas. This deteriorating effect was smaller when the wafers were emitter-diffused or gettered before the oxidation (No. 5 and 6). The phosphorus diffused layers were still present during oxidation, thus diffusions under extreme conditions (1050 °C) were performed. However, the obtained lifetime was always much smaller than the lifetime of the corresponding non-oxidised samples. For the inverted sequence, which was oxidising the samples before the phosphorus diffusions (No. 7 and 8), the lifetimes recovered to the reference value and even exceeded it.

In contrast to the application on non-oxidised wafers (No. 2 and 3) the gettering diffusion (No. 8) was less effective than the emitter diffusion (No. 7) when applied after oxidation. A subsequent oxidation after the emitter diffusion of oxidised samples (No. 9 and most right column in Fig. 3.6) annihilated the beneficial effect of the emitter diffusion. Both investigated areas show the same behaviour with the beneficial impact of diffusions being more pronounced in area A, the area with larger grains and higher initial lifetime.

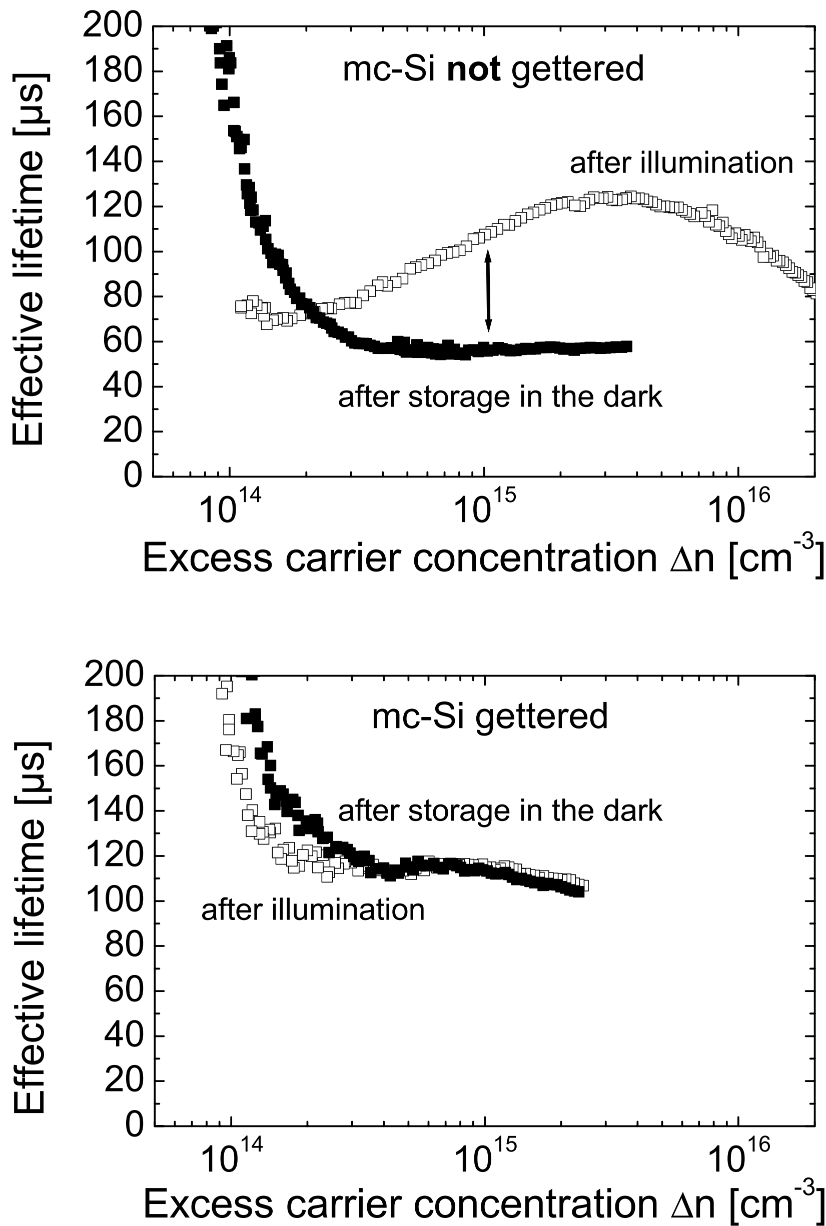

Fig. 3.7: Effective lifetime versus excess carrier concentration for the reference sample (upper graph) and a sample after gettering diffusion (lower graph) before and after illumination. The trapping at low excess carrier densities does not affect the analysis at $\Delta n = 1{\cdot}10^{15}$ cm^{-3}.

To obtain a deeper understanding of the observed differences in lifetime, the samples were measured after a long storage in the dark, illuminated under a sun simulator at an intensity of about 1000 W/m^2 and measured again. This procedure is a test for the presence of iron in boron-doped silicon [47]. Applying this procedure to the reference sample resulted in a significant increase of the lifetime after illumination (Fig. 3.7). This "light-soaking" was applied to both areas of all samples and repeated several times. The described increase of lifetime after illumination was also clearly detectable after the oxidation, but much less pronounced after any phosphorus diffusion involved. The results are listed in Table 3.3.

The observed behaviour has to be interpreted carefully. Apart from iron contamination there could be other reasons for a change in carrier lifetime after illumination. However, the crossover point of the lifetime curves was at about $2 \cdot 10^{14}$ cm^{-3}, which is characteristic for iron in boron-doped silicon of 1.5 Ω cm, supporting the idea that a significant iron contamination was detected [47].

Under the assumption that the observed change in lifetime is due to iron, the interstitial iron concentration can be directly calculated from the difference of the lifetimes before (τ_{dark}) and after illumination ($\tau_{illuminated}$) via

$$[Fe_i] = C \cdot \left(\frac{1}{\tau_{\text{illuminated}}} - \frac{1}{\tau_{dark}} \right). \qquad 3\text{-}1$$

The pre-factor C was calculated from the data published by Macdonald [47]. It is $C = -2.91 \cdot 10^{13}$ µs cm^{-3} for 1.5 Ω cm boron doped silicon at an excess carrier density of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}.

This results in iron concentrations in the order of 10^{11} cm^{-3} for the non-diffused samples. After phosphorus diffusion these values decreased to 10^{10} cm^{-3}. Most phosphorus-diffused samples did not show a significant rise in lifetime after illumination exceeding measurement uncertainty, thus the calculation was not performed for those samples.

Table 3.3: Matrix of performed experiments and measured effective lifetimes at $\Delta n = 1 \cdot 10^{15}$ cm^{-3} of two areas on every wafer. The measurements were taken after storage for at least twelve hours in the dark and directly after at least one hour illumination under a sun simulator. The corresponding concentration of interstitial iron is also listed. No values were calculated where the difference of the measured lifetimes was too small to be significant (marked with −).

		area A			area B		
No.	process sequence	τ_{dark} [µs]	$\tau_{illuminated}$ [µs]	Fe_i [cm^{-3}]	τ_{dark} [µs]	$\tau_{illuminated}$ [µs]	Fe_i [cm^{-3}]
1	reference	52	98	$26 \cdot 10^{10}$	43	79	$31 \cdot 10^{10}$
2	emitter diffusion	131	155	$3 \cdot 10^{10}$	87	99	$4 \cdot 10^{10}$
3	gettering diffusion	184	190	–	104	108	–
4	oxidation	27	51	$51 \cdot 10^{10}$	22	30	$35 \cdot 10^{10}$
5	emitter + oxidation	39	46	$11 \cdot 10^{10}$	29	30	–
6	gettering + oxidation	59	64	$4 \cdot 10^{10}$	35	32	–
7	oxidation + emitter	93	95	–	55	59	–
8	oxidation + gettering	72	69	–	48	49	–
9	oxidation + emitter + oxidation	25	25	–	21	20	–

The described effects of the diffusions were consistent with the removal of mobile impurities by phosphorus diffusion [39,48,49]. The different behaviour of the two selected areas A and B is not surprising since the minority carrier lifetime is affected by *all* recombination channels present (for example dislocations) and not only by impurities which can be gettered. As expected, phosphorus diffusion was more effective at a higher temperature. The detrimental influence of the

oxidation on the lifetime was present after all performed processes. It has been suggested that the dissociation of impurity precipitates at high temperatures enables their diffusion throughout the bulk [34]. This would explain the observed decrease in lifetime after the oxidation. The contamination of the bulk was less pronounced when the phosphorus layers were left on the wafers during oxidation which could have been an in-situ gettering while the precipitates dissolved. However, the beneficial effect of the phosphorus diffusion was clearly diminished and an increment of [Fe_i] was detected in area A (No. 5 and 6 compared to No. 2 and 3). This may have been caused by a limited solubility when the concentration of contaminating species became excessive. Macdonald et al. [23] proposed that the observed behaviour could be due to re-injection of the gettered impurities from the phosphorus layer into the bulk, a theory which would well explain the results of this study.

3.3.3 Correlation between local minority carrier lifetime and dislocation density

Since the QssPC set-up does not give a good spatial resolution, the CDI technique was applied to have a closer look at the lifetime distribution of a small area of 14·14 mm^2 size which is situated inside area B. The area-averaged results in comparison to the QssPC measurements are shown in Fig. 3.8.

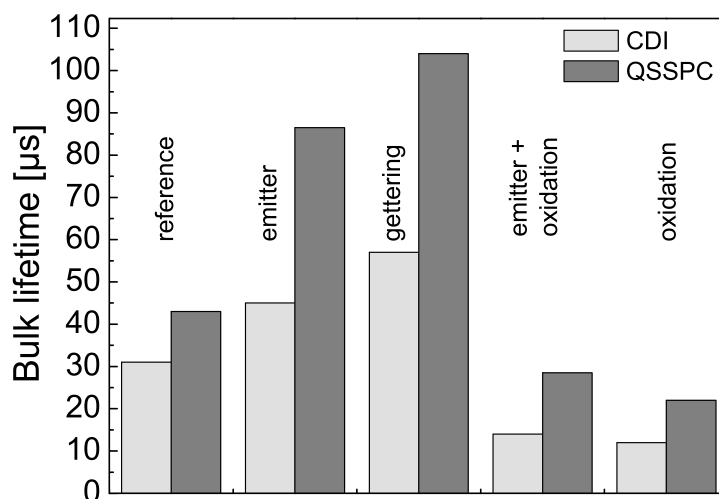

Fig. 3.8: Bulk lifetime measurements with QssPC and CDI technique in area B.

Both CDI and QssPC data reveal the same trends. The quantitative deviation is explained by the different injection levels (CDI measures under constant illumination whereas QssPC data was read out at $\Delta n = 10^{15}$ cm^{-3}). The dislocation density was determined with microscopic images of polished wafer surfaces after a Secco etch treatment[4]. In the following the correlation between these two measurements is investigated.

In Fig. 3.9 the dislocation density of the reference sample, i.e. the sample without high-temperature treatment, is shown. In the upper image of Fig. 3.10 the measured minority carrier lifetime of the same wafer can be seen. Areas with low dislocation density (dark) corresponded to regions of high lifetime and areas with high dislocation density (white) corresponded to regions of low lifetime. Furthermore the CDI measurements of wafers with the same crystal structure are shown after phosphorus diffusion at 790 °C and 880 °C. The increase of lifetime as it was found in both the CDI and the QssPC data (Fig. 3.8) after the emitter diffusion at 790 °C was mainly located in areas with initial high lifetimes.

These were the sites with a low dislocation density. In the areas with high dislocation density, there was hardly any increase in lifetime. For the gettering diffusion at 880 °C, the correlation between high lifetime/low dislocation density and low lifetime/high dislocation density was even more pronounced.

In Fig. 3.11 the EPD measurement after emitter diffusion at 790 °C and drive-in oxidation at 1050 °C is shown. In comparison to the EPD measurements of the reference wafer (no thermal treatment), the structure had a smaller contrast and shows a grey haze representing a higher background level of dislocation density. The CDI measurement of the solely oxidised sample (i.e. no emitter diffusion before oxidation) is shown in the upper image of Fig. 3.12. It revealed nearly the same lifetime distribution as the oxidised wafer with emitter diffusion before oxidation (image in the middle). The only difference was an even reduced carrier lifetime in the “high-lifetime” areas. The lifetimes for a wafer which was gettered after oxidation is displayed in the lower picture. The minority carrier lifetime recovered but after gettering the value was much smaller than it was after gettering without prior oxidation. The lifetime recovery mainly occurred in areas with low

[4] The measurements of the etch pit densities evaluated in this study were performed by Stephan Riepe.

dislocation density whereas at the highly dislocated sites hardly any improvement was detected. The results demonstrate a clear correlation between dislocation density, minority carrier lifetime and gettering efficiency. They will be quantitatively analysed in the following section.

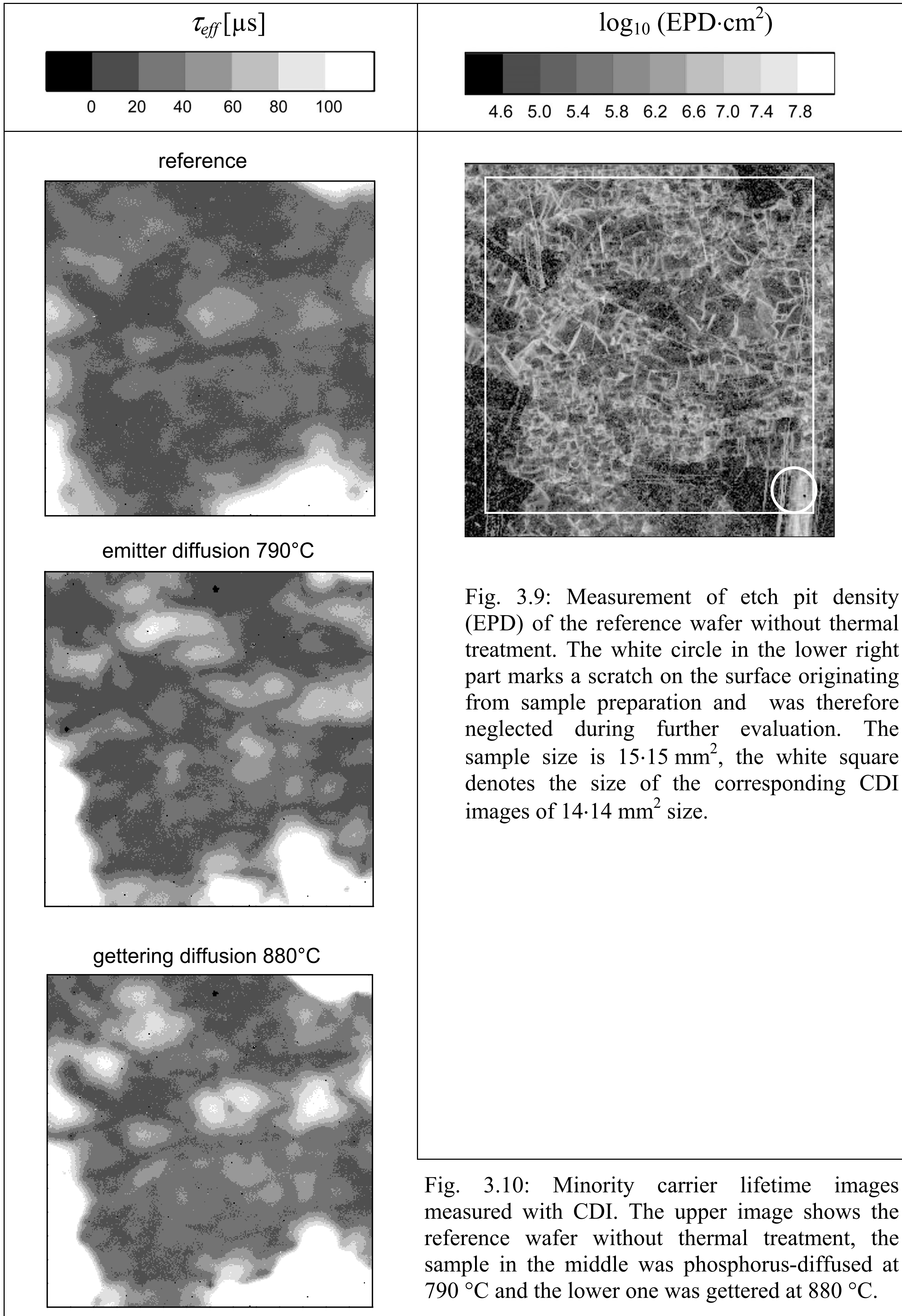

Fig. 3.9: Measurement of etch pit density (EPD) of the reference wafer without thermal treatment. The white circle in the lower right part marks a scratch on the surface originating from sample preparation and was therefore neglected during further evaluation. The sample size is $15 \cdot 15\ mm^2$, the white square denotes the size of the corresponding CDI images of $14 \cdot 14\ mm^2$ size.

Fig. 3.10: Minority carrier lifetime images measured with CDI. The upper image shows the reference wafer without thermal treatment, the sample in the middle was phosphorus-diffused at 790 °C and the lower one was gettered at 880 °C.

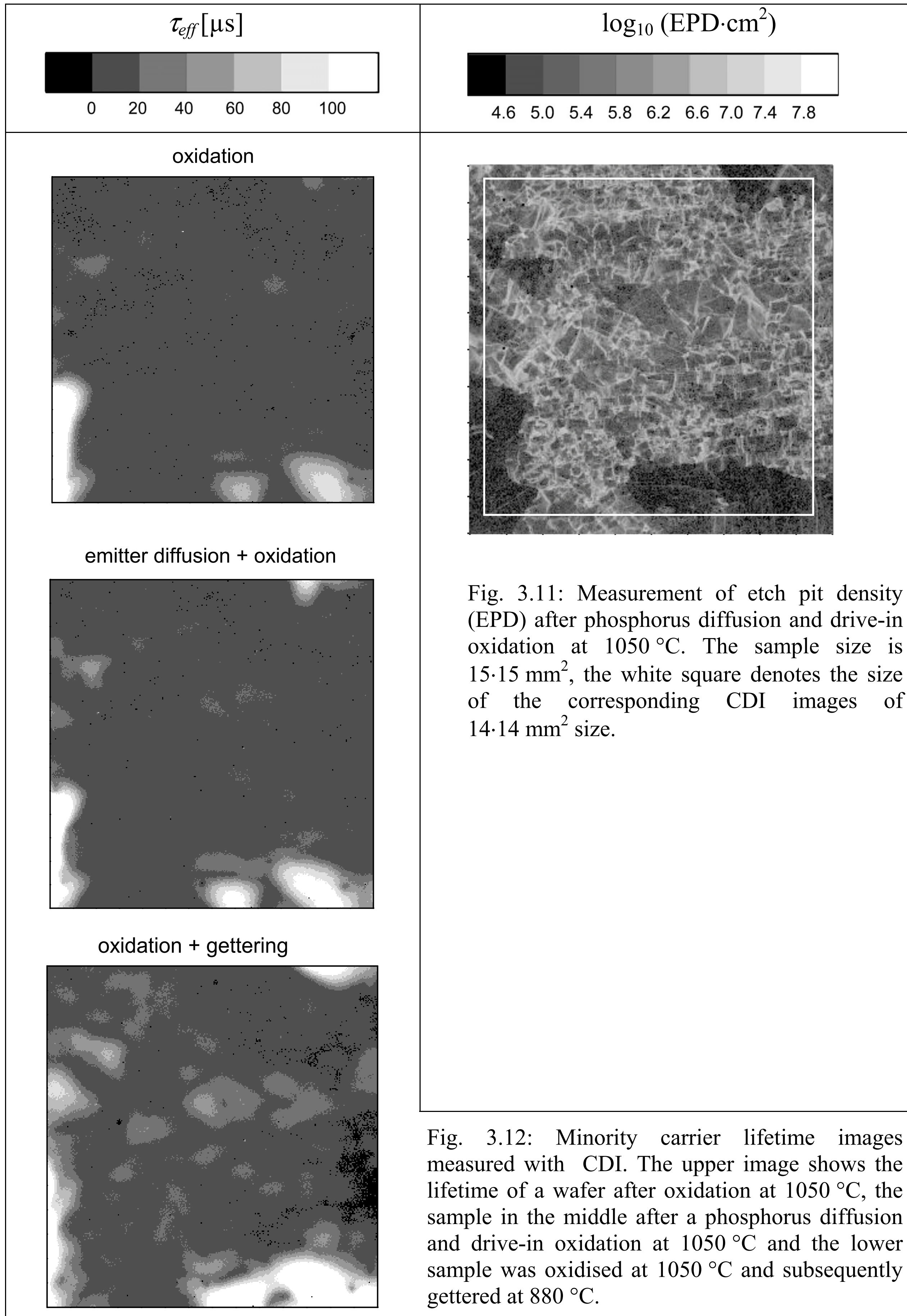

Fig. 3.11: Measurement of etch pit density (EPD) after phosphorus diffusion and drive-in oxidation at 1050 °C. The sample size is 15·15 mm^2, the white square denotes the size of the corresponding CDI images of 14·14 mm^2 size.

Fig. 3.12: Minority carrier lifetime images measured with CDI. The upper image shows the lifetime of a wafer after oxidation at 1050 °C, the sample in the middle after a phosphorus diffusion and drive-in oxidation at 1050 °C and the lower sample was oxidised at 1050 °C and subsequently gettered at 880 °C.

3.3.4 Microscopic model

After phosphorus diffusion the minority carrier lifetime was considerably increased. A detailed investigation exhibited that this increment is strongly inhomogeneous and particularly pronounced in areas with low dislocation densities. This limitation in multicrystalline silicon was previously described by Sopori et al. [50]. Kittler and Seifert [51] investigated the influence of dislocation density on the effectiveness of gettering in a similar experiment on intentionally dislocated and contaminated monocrystalline silicon. To explain their results they proposed a model in which impurities are accommodated at dislocations in two areas (see Fig. 3.13):

- Impurities in the core region around the dislocation are tightly bound and cannot be gettered from this site.
- Impurities in the strain field of a dislocation are weakly bound and can be gettered or their defect levels can be passivated.

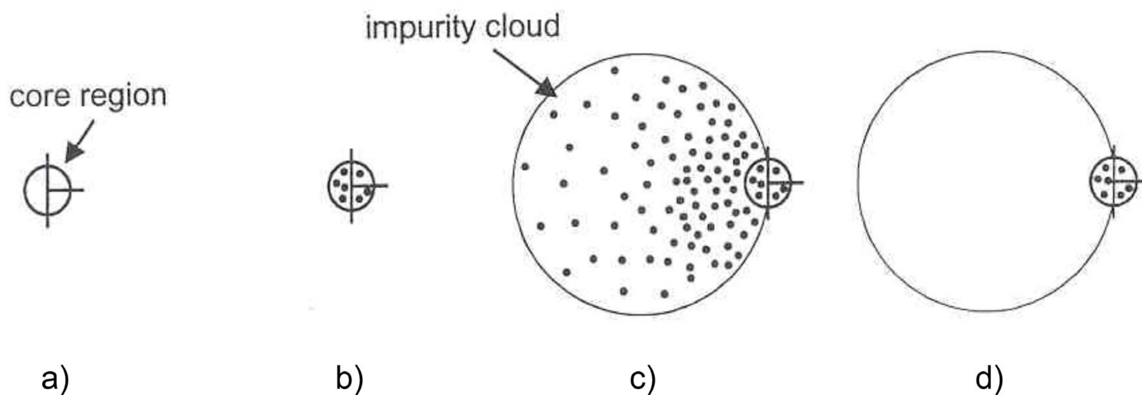

Fig. 3.13: Suggested impurity accommodation and effect of gettering on impurity states at a dislocation [51].
a) Clean dislocation.
b) Impurities in the core.
c) Impurities in the cloud formed by the dislocation strain field.
d) Dislocation after gettering process. The impurities in the cloud are removed.

Since a dislocation will always maintain a certain amount of active defects, this results in a minimum recombination strength Γ_{min} of a dislocation decorated by impurities. Once a dislocation gets contaminated, which in the case of multi-crystalline silicon takes place already during the growth of the crystal, even a very efficient gettering treatment is not capable of removing the impurities from the

dislocation. The minimum recombination strength of dislocations decorated by impurities sets an upper limit to the obtainable diffusion length. In [44] Riepe et al. developed a two-dimensional model adjusted to CDI measurement conditions.

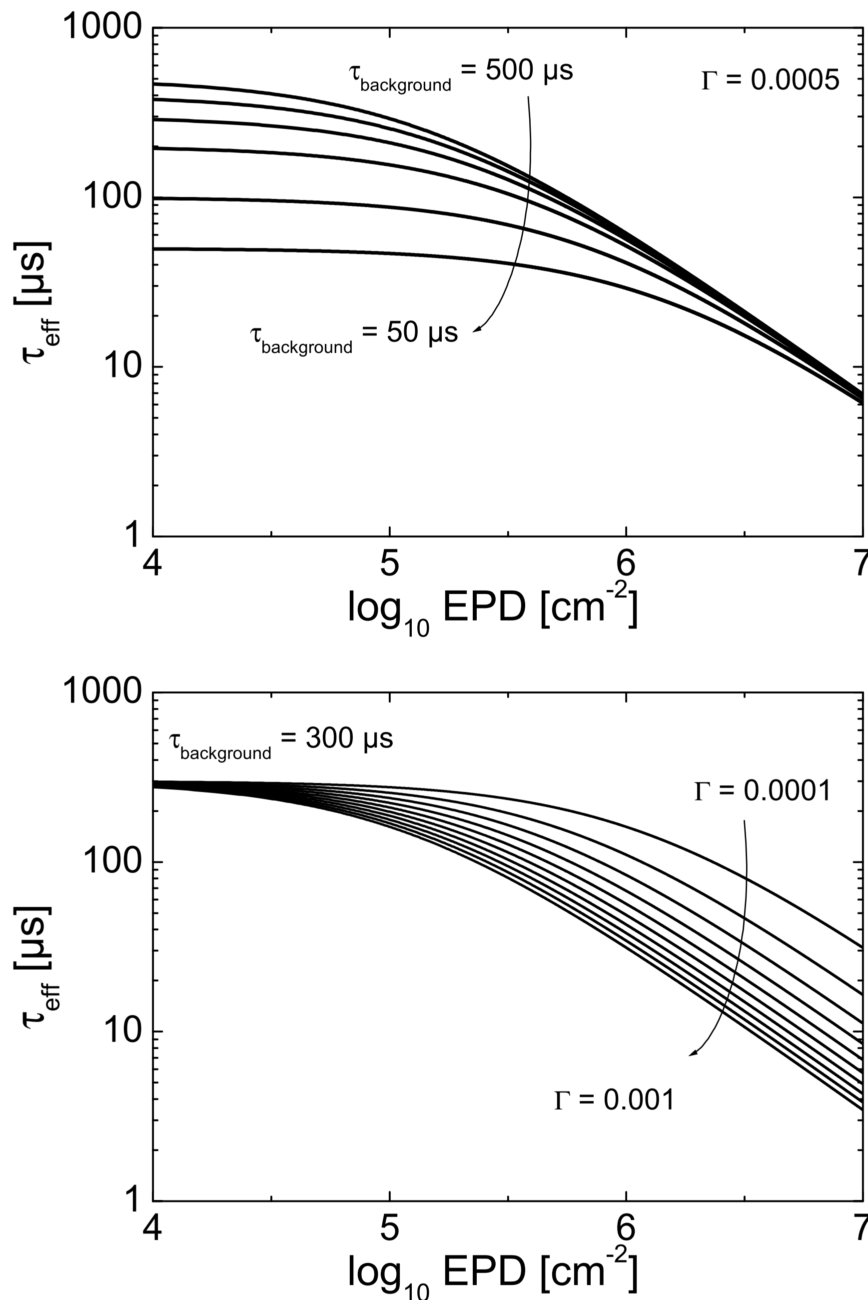

Fig. 3.14: Dependence of bulk lifetime on dislocation density and "background lifetime" according to the model of Riepe et al [44]. The graphs show that a varying background lifetime mainly determines the maximum achievable lifetime for low dislocation densities (upper graph) whereas the recombination strength has a big impact for higher dislocation strengths (lower graph).

In this model, dislocations are embedded in material of high lifetime $\tau_{background}$, and the minimum recombination strength Γ_{min} of the dislocations leads to a maximum achievable minority carrier lifetime depending on dislocation density. The dependence of the bulk lifetime on dislocation density is shown in Fig. 3.14. The background lifetime $\tau_{background}$ determines mainly the maximum achievable lifetime in low dislocation areas whereas in highly dislocated regions the lifetime is mainly sensitive to the recombination strength Γ. This enables the fitting of the data with just two varying parameters which are most sensitive in the two opposing limiting cases. The minority carrier lifetime and the measured dislocation density were compared for

- a reference sample,
- a wafer after a gettering diffusion,
- a wafer after an oxidation,
- and a wafer after oxidation and subsequent gettering diffusion.

To minimise the impact of a lateral misalignment of the two measurements and to account for the diffusion of the minority carriers, an array of 12·12 pixels ($\approx 0.34\ mm^2$) was arithmetically averaged for both, CDI and EPD measurement data. This resulted in plots of 576 measurement points (see Fig. 3.15). According to the model the envelope line (dashed line) should describe the data if no other defects than the dislocations are present. Since other defects (e.g. grain boundaries and surfaces) can contribute to recombination as well, in addition to the upper bound also the mean value of the "data clouds" (for $N_{dis} \geq 10^{5.5}\ cm^{-3}$) was modelled (solid line). This led to an estimate of the minimum values for the recombination strength Γ_{min}, the average Γ_{av} and the background lifetime $\tau_{background}$. For the reference sample (upper image) most data points were located at a dislocation density of $N_{dis} \approx 10^5$-$10^6\ cm^{-2}$ and all lifetimes were well above 10 µs. The highest achieved lifetimes led to a simulation of dislocations with a minimum recombination strength of $\Gamma_{min} = 0.0002$ embedded in rather clean silicon with a lifetime of $\tau_{background} \approx 200$ µs ($\Gamma_{av} \approx 0.001$). After oxidation at 1050 °C the carrier lifetime was drastically reduced (lower graph). This reduction took place all over the investigated area, but relatively high lifetimes were maintained in areas of low dislocation densities. Most data points moved to higher dislocation densities ($N_{dis} = 10^{5.5\ -\ 6.5}$) and lower lifetimes (below 10 µs).

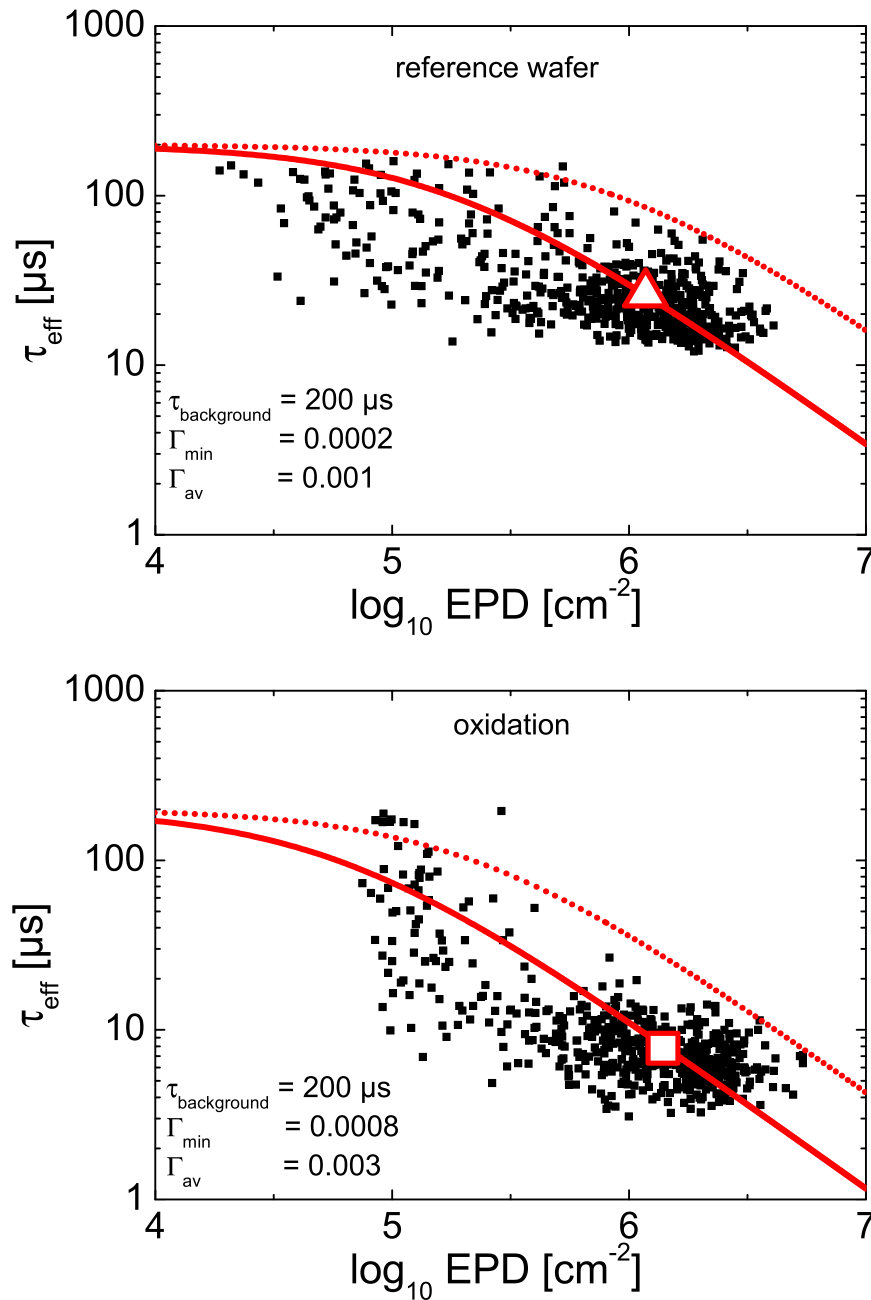

Fig. 3.15: Correlation of measured etch pit density and minority carrier lifetime. The EPD measurement of the emitter diffused and oxidised wafer was also used for the oxidised sample shown in the lower graph. The dotted line represents a calculation for the lifetime dependence on dislocation density using the model described in [44]. This determines the maximum achievable lifetime when no other defects are present. The hollow symbols represent the arithmetic average for the data points of $N_{dis} \geq 10^{5.5}$ cm^{-3}, the solid line is the corresponding fit.

The number of dislocations was higher in the oxidised sample but this alone was too small to explain the shift in lifetime. The modelled background lifetime did not change either (≈ 200 µs), it was the recombination strength of the dislocation which had to be increased to obtain a good fit ($\Gamma_{min} \approx 0.0008$ by a factor of four

and $\Gamma_{av} \approx 0.003$ by a factor of three). The same results were obtained for the sample which received an emitter diffusion before oxidation. The beneficial effect of the emitter diffusion was annihilated by the subsequent drive-in oxidation. Similar observations were previously made by Macdonald et al. [23,39]. The degradation of the lifetime was attributed to the dissolution of precipitated impurities. The annihilation of the gettering effect of phosphorus diffusion at very high temperatures was explained with the re-injection of the contaminants from the gettering layer into the bulk. Furthermore the EPD measurement revealed a higher dislocation density in the oxidised multicrystalline silicon sample in comparison with the reference wafer. Such increment was also observed by Franke [52] for tricrystalline silicon. Both data groups are plotted in one graph in Fig. 3.16.

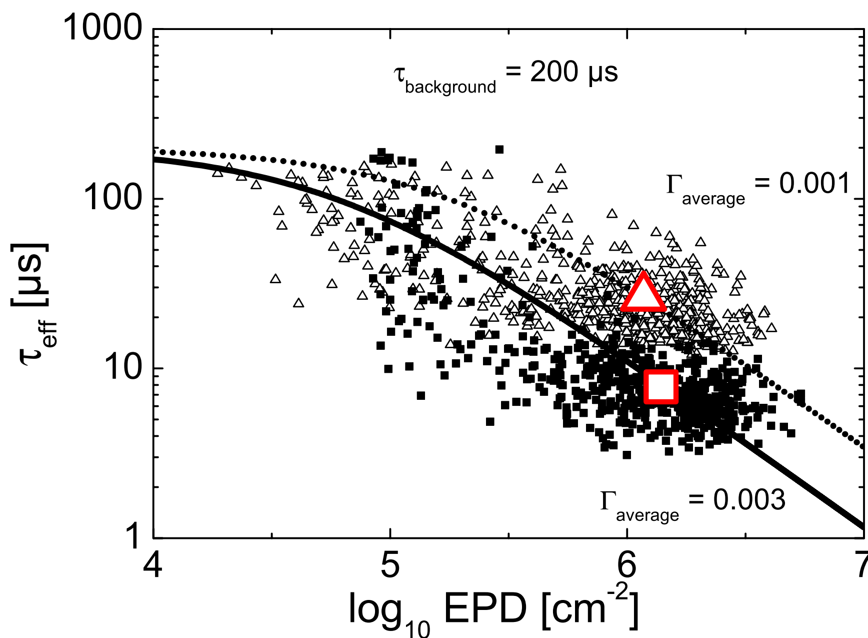

Fig. 3.16: Carrier lifetime versus etch pit density for neighbouring wafers before and after oxidation at 1050 °C. The increment of dislocation density N_{dis} alone did not explain the carrier lifetime degradation, additionally an increased recombination strength Γ was needed to explain the results.

The average dislocation density of the oxidised sample $N_{dis,ox} = 10^{6.14}$ (taken as arithmetic average of the data points of $N_{dis} \geq 10^{5.5}$) was only slightly higher than the reference value $N_{dis,ref} = 10^{6.07}$ (shift from Δ to □). The higher number of dislocations alone could therefore not satisfactorily describe the degradation of

minority carrier lifetime. The enhanced recombination strength Γ can be explained with the dissolution of precipitated impurities in regions with many crystal defects whereas the lowly dislocated sites were hardly affected (see also Fig. 3.12). Microscopically dislocations are the centres of recombination-active species and the high-temperature oxidation leads to a release of impurities into the bulk material. These agglomerate in the surroundings of dislocations, probably in the strain field.

Applying the gettering diffusion to an already oxidised wafer (upper graph in Fig. 3.17) recovered the average lifetime, but to a significantly minor degree as if the wafers were not oxidised prior to gettering (lower graph in Fig. 3.17). For the gettered wafer without prior oxidation, the background lifetime was increased from 200 µs (reference wafer) to about 700 µs and the minimum recombination strength was modelled as $\Gamma_{min} \approx 0.00015$ ($\Gamma_{av} \approx 0.00065$). The gettering efficiency was defined as the ratio of the lifetimes before and after gettering as

$$\eta_{gettering} = \frac{\tau_{gettered}}{\tau_{reference}}. \qquad 3\text{-}2$$

High values were measured in the lowly dislocated areas whereas in the highly dislocated areas hardly any improvement was detected.

In Fig. 3.12 it was already observed that the recovery mainly took place in areas of comparatively low dislocation density, the data evaluation of Fig. 3.18 supports these findings. Only the lowly dislocated areas did benefit from the gettering. According to the model, the background lifetime was increased to about 700 µs and the minimum recombination strength recovered to $\Gamma_{min} \approx 0.0002$ ($\Gamma_{av} \approx 0.0012$). This means that the impurities were effectively gettered from the strain field of many dislocations but not from all of them. In the presented model this means that phosphorus gettering removed impurities from the bulk of the wafer but a minimum recombination strength of the dislocations was kept. The number of dislocations still sets an upper limit to the achievable carrier lifetime.

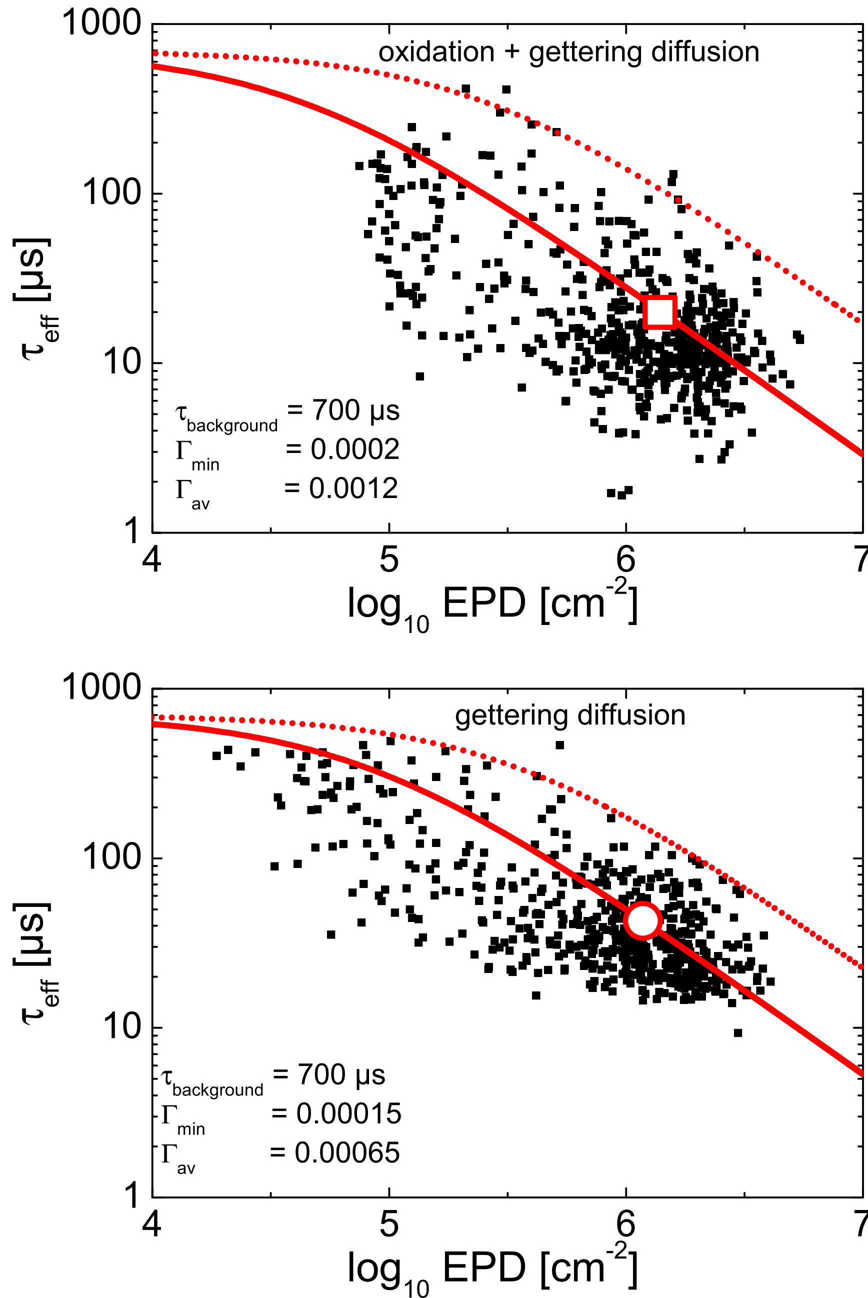

Fig. 3.17: Correlation of etch pit density and minority carrier lifetime. For the sample which was gettered after oxidation (upper graph) the EPD of the emitter-diffused and oxidised wafer was used. The EPD measured on the reference wafer was used for the sample after gettering (lower graph). The dotted line represents a calculation for the lifetime dependence on dislocation density after the model described in [44]. This determines the maximum achievable lifetime when no other defects are present. The hollow symbols represent the arithmetic average for the data points of $N_{dis} \geq 10^{5.5}$cm^{-3}, the solid line is the corresponding fit.

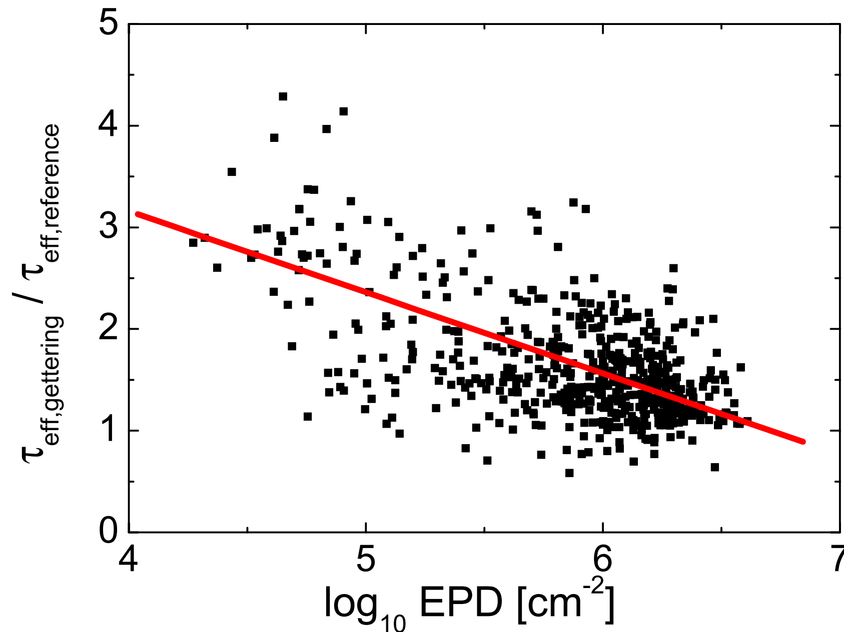

Fig. 3.18: Gettering efficiency derived from the comparison of lifetime of the gettered wafer (Fig. 3.17) with the reference wafer (Fig. 3.15). A big improvement (about a factor of three) can be obtained in lowly dislocated areas whereas in highly dislocated areas only a small gettering effect is detected. The solid line represents the linear fit.

Similar experimental observations have been described by Sopori et al. [50] who found a fixed carrier lifetime for a dislocation density of $N_{dis} \geq 1 \cdot 10^6$ cm^{-2}. Such behaviour can also be described with the presented model by adjusting the parameters for the recombination strength Γ.

3.3.5 Conclusions for the production of multicrystalline silicon solar cells

The experiments described in section 3.3 clearly show that the oxidation at 1050 °C deteriorates the bulk lifetime of multicrystalline silicon. Nevertheless, oxidation of the silicon surface plays a key role in high-efficiency processing of solar cells. It serves as a masking layer which simultaneously passivates the surface (and can act as an anti-reflection coating if no encapsulation is required). Therefore the sequence of phosphorus diffusions and oxidations has to be chosen correctly if an oxidation is necessary.

The performed experiments result in clear guidelines how to maintain a high bulk-lifetime in multicrystalline silicon when applying high-temperature processes.

Gettering

The phosphorus diffusion is capable of effectively gettering mobile impurities such as iron into the phosphorus layer. This gettering layer should be etched away in order to avoid the release of impurities from the gettering site during subsequent high-temperature processes.

Oxidation

The high-temperature processes, namely oxidations, should be applied after gettering since they increase the dislocation density and therefore the number of sites where impurities can accommodate. Oxidation at 1050 °C dissolves precipitated impurities and should, if possible, be followed by a phosphorus diffusion (e.g. emitter diffusion) to recover carrier lifetime (at least partly). It is not beneficial to have a high-temperature oxidation at the end of the process sequence (e.g. for emitter drive-in) since carrier lifetime is decreased again. Furthermore it is advisable to reduce the oxidation temperature and decrease ramp-up and ramp-down gradients to minimise degradation effects.

3.4 Chapter summary

The change of the minority carrier bulk lifetime in multicrystalline silicon during gettering processes and oxidations was investigated. For the examined material phosphorus gettering at temperatures between 860 °C and 900 °C achieved higher minority carrier lifetimes than phosphorus-aluminium co-gettering. One of the reasons for the improved lifetime after the phosphorus diffusion was the removal of iron. This was concluded from injection dependent lifetime spectroscopy on large measurement spots. With spatially resolved measurements of the minority carrier lifetime the local effect of the phosphorus diffusion was investigated. The gettering efficiency was not homogenous all over the wafer: In regions with many dislocations no increase in lifetime was detected whereas in regions of low dislocation densities very high bulk lifetimes were measured. A microscopic model explaining the results was discussed.

The oxidation of multicrystalline silicon at 1050 °C clearly deteriorated the material quality. Besides the negative effect of a rise in dislocation density

precipitated impurities were suspected to have dissolved and spread out in the bulk leading to homogeneously low carrier lifetimes. These could at least partly be recovered by a subsequent phosphorus diffusion.

Nevertheless, the degradation could be prevented by adjusting the oxidation process. Lowering the oxidation temperature to 800 °C significantly reduced the degradation. The ramp-up and ramp-down profiles of the process were shown to have a strong impact, too. Using slow ramps the carrier lifetime of multicrystalline silicon was nearly perfectly maintained.

From the conducted experiments conclusions were drawn with respect to the processing sequence for multicrystalline silicon solar cells: The first process should be the permanent removal of impurities from the material by etching away the gettering layer of a phosphorus diffusion. If an oxidation of the surfaces is necessary this has to be done at low temperatures and should be followed by another phosphorus diffusion.

4 Texture and front surface structure of multi-crystalline silicon solar cells

4.1 Introduction

As early as 1960 solar cells were textured on the front surface to decrease the reflectance [53] and to boost the efficiency. In those days the front surface was shaped by ultrasonic cutting into inverted pyramids. Later on, wet-chemical etching was introduced [54] and the first commercial applications appeared in 1975 for space solar cells [55]. Nowadays all high-efficiency single crystalline silicon solar cells are textured on the front surface to reduce reflection losses and to improve the light-trapping properties. The most prominent way to obtain good results is the etching of pyramids into <100> orientated monocrystalline wafers. This method uses the anisotropic etch rates of potassium (KOH) or sodium hydroxide (NaOH), where <111> planes are etched two orders of magnitude slower than <100> and <110> planes. The result is a surface covered with intersecting <111> planes that form randomly distributed pyramids of varying size in the case of "random pyramids" or, when a cross-hatched masking layer is used, form the "inverted pyramids" structure. This method is an elegant and effective way to texture the surface of monocrystalline wafers with <100> orientation, but it is not applicable for multicrystalline wafers since the multiple grains have different and generally unknown orientations. Therefore it is necessary either to use isotropic etches or to structure the surface by other means which are independent of crystal orientation.

Since an increased absorption of light in the solar cell directly increases the short-circuit current density and consequently the efficiency, the texturing of multicrystalline silicon has become a topic of high importance and is studied by various research groups. Several approaches are described in section 4.2. A special case of high-efficiency texturing for multicrystalline silicon is a hexagonal pattern of etched bowls, the so called "honeycomb" structure. The optimisation of low-temperature plasma processes to achieve a damage-free surface and very good light trapping properties is described in section 4.3.

To enable an easy comparison of different textures, the highly wavelength-dependent reflectance is weighted with the solar spectrum and integrated from $\lambda_0 = 300$ to $\lambda_1 = 1200$ nm via

$$R_W = \frac{\int_{\lambda_0}^{\lambda_1} S(\lambda) R(\lambda) \frac{q\lambda}{hc} d\lambda}{\int_{\lambda_0}^{\lambda_1} S(\lambda) \frac{q\lambda}{hc} d\lambda} . \qquad 4\text{-}1$$

with q being the elementary charge, h Planck's constant, c the velocity of light and $S(\lambda)$ the spectrum AM1.5g. Thus the distribution of the standard spectrum is taken into account and a single value represents the optical quality of the texture for the incident light. The weighted reflectance values R_w found in literature often vary in the integration boundaries λ_0 and λ_1.

4.2 Texturing with random and with defined geometry

During conventional processing of random pyramids on monocrystalline silicon, isopropyl alcohol (IPA) is usually added to the etching solution in order to increase the wettability of the surface. Bubbles of the gaseous reaction products cover the surface and serve as a micro-masking layer. This produces small regions where the attack of the etching species is inhibited. Consequently the <111> planes are revealed by proceeding etching [56]. Any particular micro-mask bubble is not stable over time; macroscopically the masked areas fluctuate over the surface resulting in randomly distributed pyramids of different size (see Fig. 4.1). Reflection is lowered from about 36 % for a planar wafer to about 11 % for the textured one.

Transferring such a chemical system to multicrystalline silicon requires the use of isotropic etches which do not depend on crystal orientation. For the wet chemical approach a solution of hydrofluoric acid (HF) and nitric acid (HNO_3) is suitable because this etch provides smooth surfaces without damage and is nearly perfectly isotropic [57]. The reaction of the acid with silicon is strongly exothermic and phosphoric acid (H_3PO_4) or acetic acid (CH_3COOH) may be added to control the etch. However, the surface becomes smoother and reflectivity is increased instead of decreased. Surface active agents playing the role of IPA in random

pyramid etching are therefore usually added to the etching solution to increase the bubble-masking-effect [58]. Latest results of Hauser et al. [59] show that the saw damage which remains on wire-sawn wafers can replace the special additives to govern the reaction and lead to well structured surfaces. Several research groups have been successful in texturing multicrystalline silicon with this method [59-62] and the roughened surface (see Fig. 4.2) shows weighted reflectance values of about 22 %.

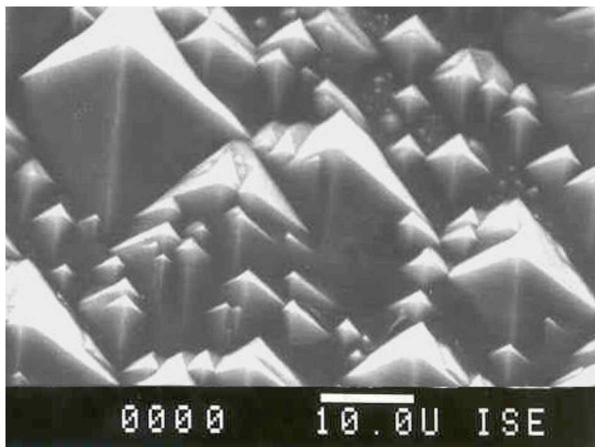

Fig. 4.1: Random Pyramids formed by KOH and IPA solution.

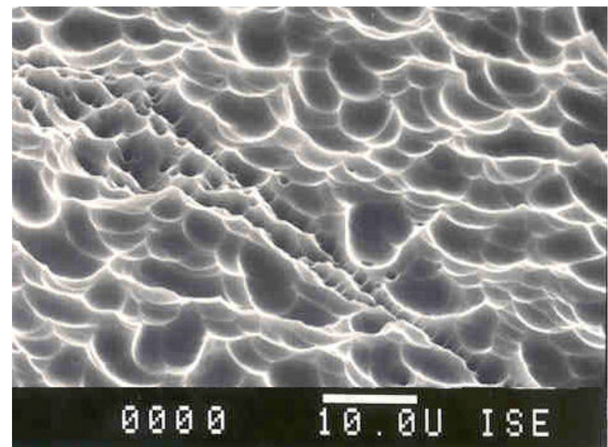

Fig. 4.2: Surface of a multicrystalline silicon wafer etched by a mixture of HF and HNO_3. The diagonal line which was preferentially etched is a grain boundary.

A different wet chemical approach for texturing multicrystalline silicon is the formation of "porous silicon" where a porous layer in the nanometer scale is etched into the surface. Porous silicon layers can be formed electrochemically [63] or in a stain etching solution [64]. Weighted reflectance values as low as 9 % were obtained [65,66] but the short-circuit current density of solar cells was strikingly low. Absorption of light in the porous silicon layer and a high interface state density could explain these results. The alteration of the surface by subsequent processes is reportedly critical and this technique lacks experimental evidence of a well passivated surface.

Another possibility for effective surface texturing is the application of Reactive Ion Etching (RIE) in a plasma reactor. In this configuration the ions gather supplementary energy from an electric field between the electrodes and are accelerated perpendicularly to the wafer's surface. Therefore the etching becomes

anisotropic but, in contrast to caustic wet chemical etching, it does not depend on crystal orientation. This property can be used to achieve high aspect ratios of depth/width of the structures, but it requires a suitable masking process: Initially, the surface is covered with at least the native oxide. This masking layer is not removed homogeneously but perforated at some spots. At these spots etching occurs and a structured surface evolves. While plasma etching with pure sulphur hexafluoride (SF_6) is isotropic in nature, deeper structures can be etched by protecting the sloped side walls of the etch pits [67]. This protective layer can be created by adding oxygen (O_2) to the plasma thus forming a silicon oxide which is removed mainly from the horizontal surface (compare Fig. 4.3).

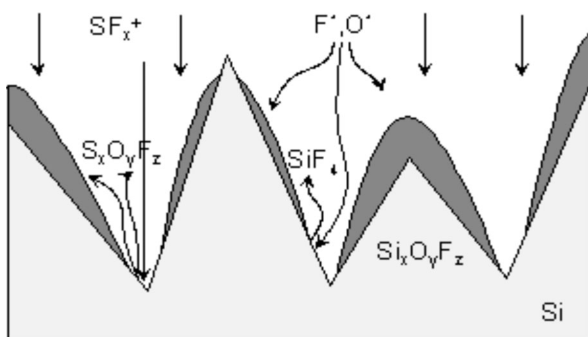

Fig. 4.3: Schematic of sidewall passivation effect for random structures [68].

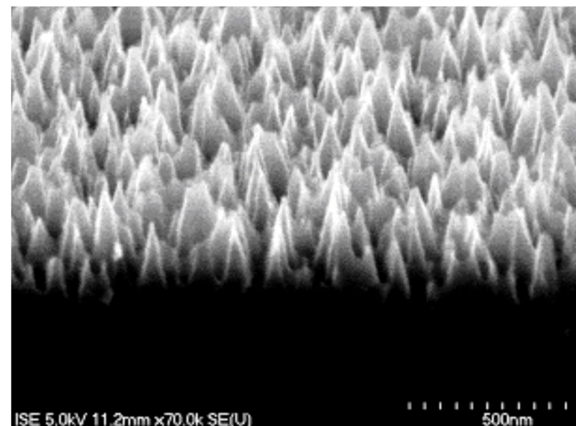

Fig. 4.4: SEM-picture of a black silicon textured surface [68].

The addition of carbon has a similar effect. In this case a polymer blocks the lateral etching of silicon. These carbon sources can be introduced as a gas (e.g. CH_4) or in the form of removed material from photoresist or from a graphite electrode. RIE-textured surfaces show a homogeneous appearance independent of crystal orientation. Kyocera applies a chlorine-based plasma in its production line and achieved 17.7 % efficiency on large area devices [69]. Pushing such processes to the limit, “silicon grass” or “black silicon” is formed which consists of very closely spaced needles of silicon with very high aspect ratios (see Fig. 4.4). Although extremely low reflectance values (1-3 % weighted reflectance [68,70,71]) were achieved this process bears severe inherent problems:

- The total surface area of the silicon is greatly increased resulting in high surface recombination.
- The silicon needles are mechanically unstable and can be easily broken during subsequent processing steps.
- The silicon needles are so small in diameter that subsequent oxidation processes can completely oxidise them. They are then easily removed in HF.

Due to the ion bombardment [72,73], a damaged layer in the order of some tenths of nanometers exists on the surface. RIE processes need to be followed by a damage-free etch back of some silicon to allow for well passivated surfaces. This results in an increase of reflectance to about 7 % [71].

Beside a surface texture with random geometry there exist several ways of surface structuring with defined geometry. The ability to preserve a designated area, preferably flat, for the metal contacts is of particular advantage. One example is mechanical grooving [74,75], where usually V-shaped grooves are sawn into the surface. Reflectance values little above 15 % were achieved [76] and light trapping is improved for cross-grooved samples whose rear surface is structured with grooves that are aligned perpendicularly to the ones on the front. Structuring the surface in a defined way can also be done by means of a laser. One example is intersecting grooves on the front [77], leaving upright cones on the surface. Subsequent wet chemical baths remove the laser-induced damage and broaden the structure. Recent results of Abbott et al. [78], who created arrays of interlocking ablation pits, are low reflectance values of about 10 %. Effective lifetime measurements of textured and passivated surfaces lead to the conclusion that the structured surface can be well passivated.

A great variety of surface geometry becomes feasible when masking layers are used to define the etch pits. Nositschka et al. [79] used colloidal masks of small SiO_2 particles in an organic solution which were spun onto the wafer. A subsequent oxygen-rich microwave (MW) plasma removed the organic residues and the small SiO_2 bowls remained roughly equally spaced as a masking layer. A RIE plasma then etched the silicon around these particles and the surface was structured with upright cones. Reflectance values comparable to mechanical grooving (≈15 %) could be achieved with this technique.

A more sophisticated approach is the use of photolithography for an accurate definition of small structures within the micrometer range. Winderbaum et al. [80] followed this approach in combination with RIE. They used a thick thermal oxide (400 nm) as a masking layer. This led to very well-defined structures but manufactured solar cells showed a deteriorated open-circuit voltage. This was probably due to thermal degradation during high-temperature oxidation (compare chapter 3) and for further experiments they used a sputtered metal mask. The selectivity of the RIE with respect to silicon/metal mask is nearly unlimited and a groove structure with about 8 % weighted reflectance and a pyramid structure with only 5.6 % reflectance were achieved. Manufactured solar cells suffered from low voltages even on the plane references, therefore an assessment of the surface passivation is not possible from that data. Stocks [81] developed the "tub" texturing method where an oxidised wafer is patterned with holes of 4 µm with centres perpendicularly spaced 10 µm apart. An isotropic etch of HF, HNO_3 and H_3PO_4 was then used to form hemispherical tubs. Reflectance values of about 26 % were achieved and light trapping was reported to be even superior to inverted pyramids. About 5 % of the wafer's surface remained planar and were not etched. A hexagonal array of etch pits would reduce this unetched area and therefore increase performance. This was realised by Zhao [26]. In two dimensions the etched pattern resembles honeycombs and thus gave this texturing scheme its name. Due to the excellent passivation and light-trapping that have been proven by experimental results of highly efficient solar cells this geometry is investigated further in the next section.

Table 4.1 Summary of texturing methods described above and assessment in terms of light trapping quality, surface passivation and published highly efficient solar cells. ++ = very good, + = good, 0 = medium, - = bad Only one reference is given in this table.

method	geometry	R_w [%]	reference	surface passivation	high-efficiency cells	light-trapping
Inverted Pyramids	defined	≈ 10	[82]	++	++	++
Random Pyramids	random	≈ 11	[56]	++	++	++
isotropic etching	random	≈ 22	[59]	++	+	+
isotropic etching	defined	≈ 20	[26][a)]	++	++	++
Porous Silicon	random	≈ 6	[83]	0	-	0
RIE	random	≈ 7	[71]	0	+	+
Black Silicon	random	≈ 2	[68]	-	-	++
RIE	defined	≈ 6	[80]	0	-	++
grooving	defined	≈ 16	[75]	++	+	++
laser	defined	≈ 10	[78]	++	0	++
colloidal masks	defined	≈ 15	[79]	0	0	++

a) No reflectance without antireflection layer was published. Experiments of the author of this thesis showed $R_w \approx 20\%$ (see section 4.3.2).

4.3 “Honeycomb”-texturing

One special case of masked texturing is the so called “honeycomb” structure. The name is derived from the hexagonal pattern of etch pits which gives the impression of a honeycomb-like topography in a two-dimensional view. The

geometry is defined by a pattern of equilateral triangles (see Fig. 4.5). This structure is transferred to a suitable masking layer and subsequently exposed to the etching medium.

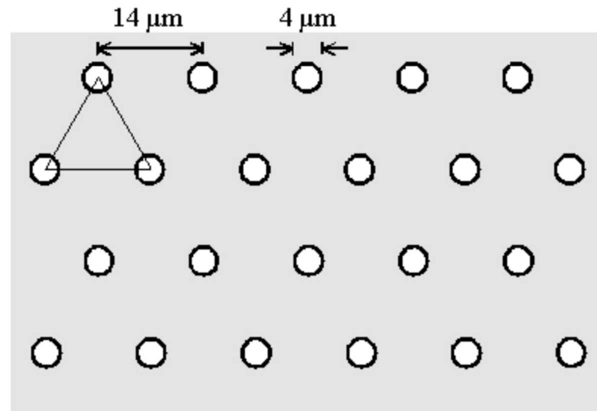

Fig. 4.5: Pattern of the photolithography mask used for "honeycomb" texturing. The important feature is the triangular alignment of the etch pits to achieve a good surface coverage when the etching is completed.

4.3.1 The optimum structure

Analytical calculations of the typical crater-like structures formed during texturing were carried out by Nishimoto et al. [60]. The authors came to the (obvious) result that the reflectance of an isotropically etched structure which consists of spherical segments depends strongly on the aspect ratio $A = h/d$ of height h and width d (see Fig. 4.6) and is minimum for $A = ½$. For light of 600 nm which perpendicularly strikes the surface reflection is reduced to 15 %. This sets an upper limit on achievable antireflection properties of wet chemically etched wafers with spherical structures. In reality the aspect ratio for isotropic etching is smaller than ½ for two reasons:

- The area which was defined in the masking layer remains flat.
- A circular structure can not completely fill a two dimensional plane.

For the latter argument the optimum etching has to find a compromise between etching too little, which leaves planar areas, and etching too much, when neighbouring craters overlap and inclined area is lost. This optimum can be found between 14 and 16 µm (also see 4.3.2).

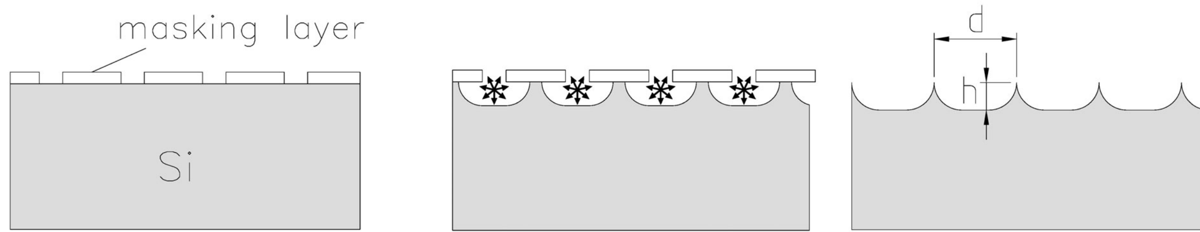

Fig. 4.6: Development of structure with increasing etch time for isotropic etching. The optimum is achieved when the hemispheres coalesce.

4.3.2 Wet chemical etching

For the wet-chemical approach a mixture of HF (50 % vol.) and HNO_3 (70 % vol.) in varying ratios was used in a basin cooled with a radiator. The solutions were defined to be in the HNO_3-rich regime in order to avoid a sub-texture in the structure as it could appear for HF-rich solutions (see section 4.1). The applied masking layer was thermally grown oxide of about 240 nm thickness which had been patterned by photolithography and HF. After stripping the photoresist, the samples were etched for different times and the diameter of the etch bowls determined with a microscope. The measured diameter minus the lithographically defined diameter (4 µm) divided by two gives the isotropic silicon removal (see Fig. 4.7). The removal of the masking oxide was measured on the rear of the samples with an ellipsometer (see Fig. 4.8).

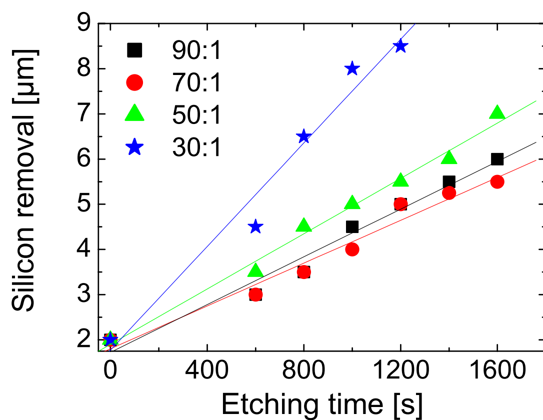

Fig. 4.7: Measured removal of silicon after texturing in HNO_3/HF mixtures of different composition.

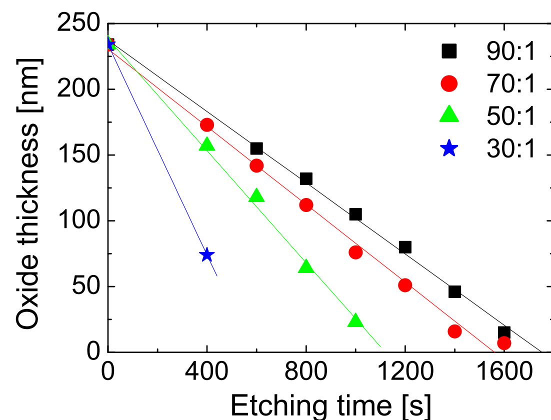

Fig. 4.8: Measured oxide thickness on rear surface after texturing in HNO_3/HF mixtures of different composition.

To achieve a silicon removal of 4.5 µm, which leads to a diameter of 13 µm, it takes, for example, 800 sec in a mixture of 50:1 and etches about 170 nm of the oxide mask. The average selectivity of etching silicon and silicon oxide hardly varies between the different solutions and is about 27 (i.e. for every 27 nm of silicon one nanometer of the oxide mask is removed). Therefore the 240 nm of silicon oxide are sufficient to etch about 6.5 µm of silicon, which results in etched bowls of 17 µm (twice the radius plus 4 µm opening in masking layer, compare Fig. 4.9).

For a more detailed investigation numerical simulations were made which take into account the real three dimensional structure. An array of 120 objects was drawn with the software AutoCAD® [84] and loaded into the programme OptiCAD®. With the assumption of 36 % reflectance of the planar surface the reflected light was calculated as a function of the diameter of the etched bowls (Fig. 4.10). For small diameters up to 14 µm the simulations and the experimental results are in good agreement. The simulation predicts a sharp minimum at 14 µm and a steep increase of reflectance for increasing diameters, but the experiments exhibit a rather flat minimum and a much flatter increment starting above 16 µm.

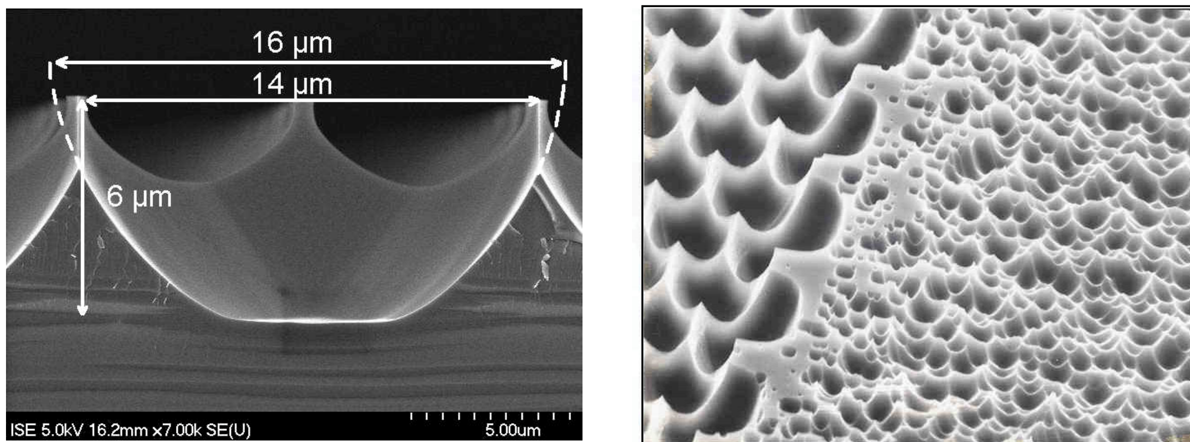

Fig. 4.9: SEM picture of an isotropically etched bowl with 16 µm diameter (left-hand). Due to the defined distance of 14 µm between two neighbouring bowls the structure levels with prolonged etching. When the structure is etched too long the oxide mask becomes perforated a random texture evolves (right-hand). This can lead to a sub-texture in the etched bowls and lower the reflectance.

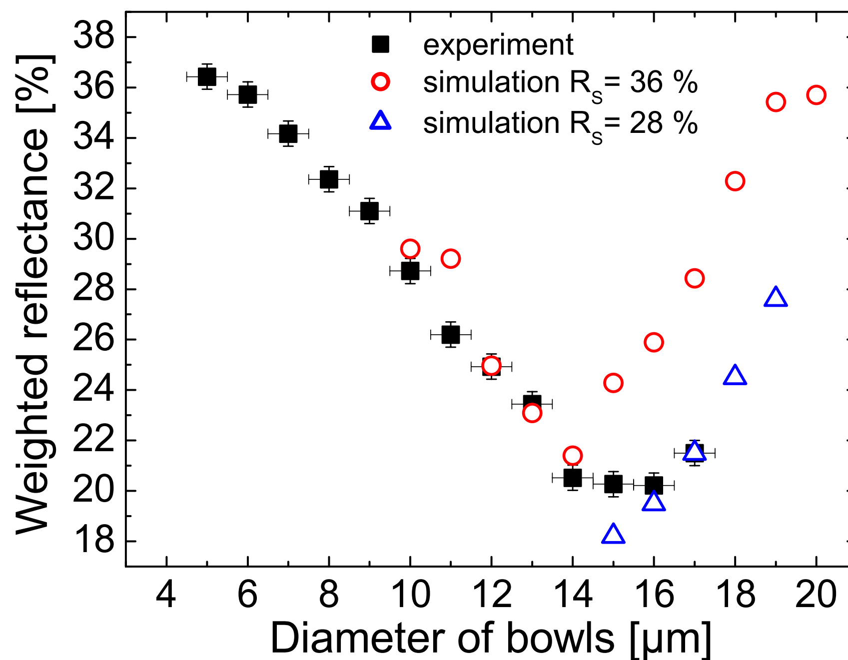

Fig. 4.10: Measured weighted reflectance values and simulation results for wet chemically etched silicon. R_S denotes the reflectivity of the planar surface assumed for the calculations.

This discrepancy can be explained by the assumed reflectance of the surface. A value of 36 % is correct for the bright-etched surface of the wafers before the texturing process, but when the silicon oxide mask is etched away the etching mechanism changes. This was observed with bright-etched samples which were put into the etching solution some with a silicon oxide layer and some without. As a result the uncovered samples had a reflectivity of about 36 % after the removal of several micrometers of silicon whereas the previously oxide-covered samples had a reflectivity of only 28 % and were randomly roughened. The reason for this roughening is probably a micro-masking effect (compare section 4.1) where a structured surface evolves once the mask has small holes where the preferential etching of the silicon can start. When this change of reflectance is accounted for in the simulation (the result is shown as triangles in Fig. 4.10), the discrepancy of the first simulation and experimental results after the transition region between 14 and 16 µm can be explained[5].

[5] This happens around 14 µm because of two reasons: 1) The durability of the silicon oxide in HF is limited. 2) The mask is lifted off the surface when the structures coalesce.

Thus the oxide layer is thick enough for good texturing since the optimum diameter for the investigated pattern is between 14 and 16 µm (Fig. 4.10) and for a diameter of 16 µm only 6 µm of silicon need to be removed (see Fig. 4.9)[6]. The smallest reflectance is 20 % for the chosen structure which is significantly higher than the 15 % calculated by Nishimoto [60].

4.3.3 Plasma etching

The aspect ratio (depth/width) is inherently smaller than ½ for isotropically etched structures and limits the achievable reduction in reflectance to about 20 %. An improvement can be achieved by Reactive Ion Etching in combination with a masking layer (see section 4.1). For the first experiments a 240 nm thick oxide was patterned by photolithography with the hexagonal pattern shown in Fig. 4.5. Gas mixtures of sulphur hexafluoride (SF_6) and oxygen (O_2) varying from 60:0 to 40:20 were used at temperatures between T = 20 °C and T = 200 °C with the power varying from 200 to 500 Watt. The selectivity was calculated as the ratio of etch rate of silicon to the etch rate of SiO_2. The effects are briefly summarised in Table 4.2.

Table 4.2: Influence of process parameters on the selectivity of etch rates of silicon and silicon oxide.

	etch rate Si	etch rate SiO_2	selectivity
increasing temperature	⇨	⇧	⇩
increasing O_2	⬀	⇧	⬂
increasing power	⬀	⇧	⇩

[6] A diameter of 16 µm requires only 6 µm of isotropic etching due to the 4 µm opening in the masking layer; (16-4)/2 = 6.

The reason for choosing the RIE process was the possibility of etching structures which are very deep (leading to a high aspect ratio) and accordingly the selectivity needs to be very high. As a conclusion the process should work at low temperature without O_2 and with little power. Those requirements are hard to meet since the etching process is exothermic, low power prolongs the process time and oxygen has a beneficial impact on the morphology as can be seen in Fig. 4.11 and Fig. 4.12.

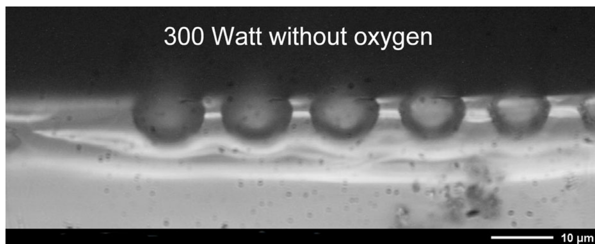

Fig. 4.11: Microscopic picture of the cross-section after plasma etching with pure SF_6.

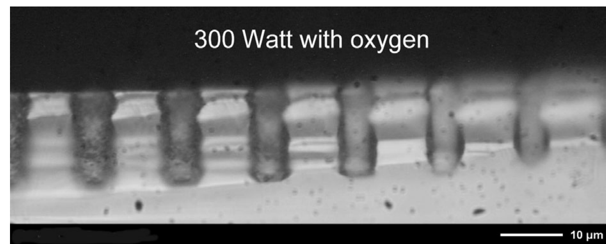

Fig. 4.12: Microscopic picture of the cross-section after plasma etching with a mixture of SF_6 and O_2.

The structure resulting from etching with pure SF_6 is nearly hemispherical whereas the structure etched with SF_6 and oxygen shows a very high aspect ratio. The reason for this feature is the passivation of the side wall as sketched in Fig. 4.13.

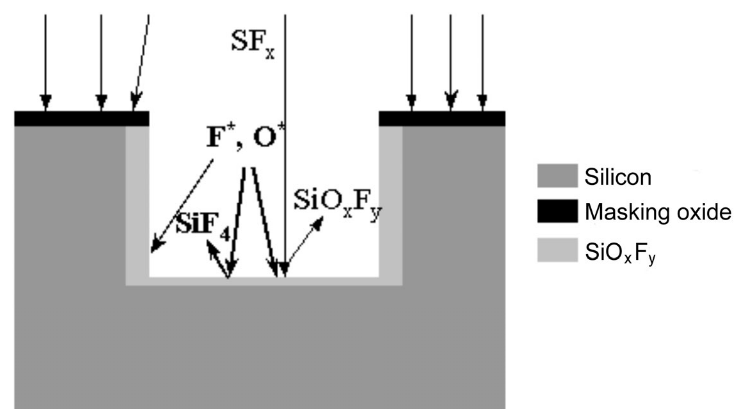

Fig. 4.13: Schematic drawing of sidewall passivation effect.

A protective layer is formed by the addition of oxygen which protects the surface. It is removed mainly from the horizontal plane by the accelerated ions whereas it protects the sidewalls from etching (compare section 4.1). This allows

the design of sophisticated structures where the depth and sidewall slope can be (nearly) independently chosen to achieve good optical properties when the cylinders are broadened accordingly. This result can be achieved by applying a microwave plasma which leads to isotropic etching. Such microwave plasma can either be applied simultaneously with the RIE or subsequently in a second step. The development of the structure is sketched in Fig. 4.14.

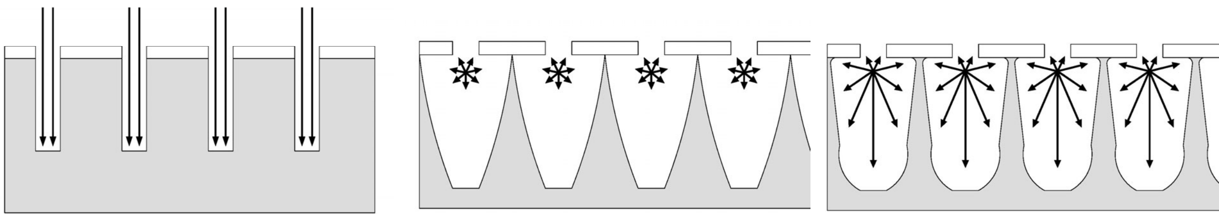

Fig. 4.14: Schematic drawing of the development of the structure etched by RIE (left picture) and an additional microwave plasma (middle). These would be the ideal structures but in reality the experimental results appear as shown in the right-hand picture.

The replenishment of the reactive ions is depth-dependent and leads to a higher etch rate at the top of the cylinder compared to the bottom. Ideally this would lead to cones as drawn in the picture in the middle with sharp spikes where the neighbouring cones meet. In reality the structures have a pinched neck at this point since the silicon directly underneath the mask is in the shadow of the masking layer. Furthermore the depth-dependent etch rate does not vary as expected and a texture which looks like the drawing on the right evolves.

Low reflectance is very important for a high-efficiency solar cell, but it is not the only requirement. A very good passivation of the surface as well as a process which does not damage the bulk is required. For the latter reason a low-temperature masking layer is required since the oxidation at 1050 °C, as it was used for the experiments so far, drastically reduces the minority carrier lifetime in multicrystalline silicon (see chapter 3). Since photoresist is indispensable in achieving the demanded structure it was directly used as the masking layer. This reduces the risk of contamination in comparison to the use of a metal mask [80] and simplifies the process. Instead of the selectivity of the etch rates of silicon and silicon oxide, now the durability of the photoresist and the possibility of complete

removal after the process becomes the important issue. Once again a high durability of the masking layer requires a low temperature and low power. A screening of different photoresists available on the market resulted in a good compromise between the achievable resolution, resist thickness and durability as well as the possibility to remove the resist in a plasma process after the etching.

With the photoresist being the only masking layer, different experiments were performed with the RIE process being responsible for the etching in depth and the Microwave (MW) power used to broaden the structure. The results are displayed in Fig. 4.15 and two trends can be observed. For a plasma with 200 W RIE and simultaneous 1000 W of MW power, the surface reflectance decreases (hollow triangles) with increasing depth of the structure as it evolves by longer etching. For a process of a fixed 10 min with 300 W RIE and increasing MW power (200, 400, 600 and 800 W), the structures become flatter due to the increasing overlap of the neighbouring cones.

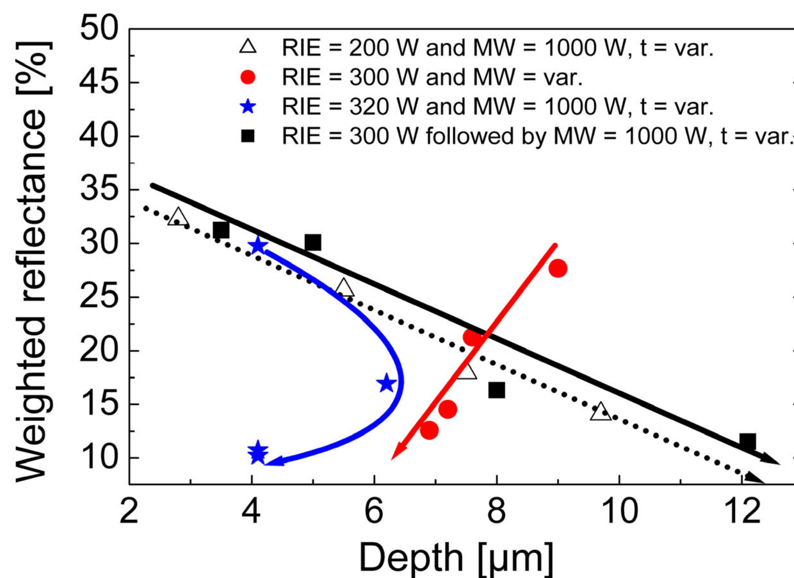

Fig. 4.15: Measured reflectance versus depth of the etched cones. The lines are guides-to-the-eye and the arrow denotes the increasing parameter (see text).

However, the reflectance does not increase with a smaller depth, unexpectedly it decreases (circles). The same happens in a process with 320 W RIE and 1000 W MW power (stars) which was applied for 2,4,6 and 8 min. This is explained by an additional sub-texture on top of the surface (see Fig. 4.16) which evolves during

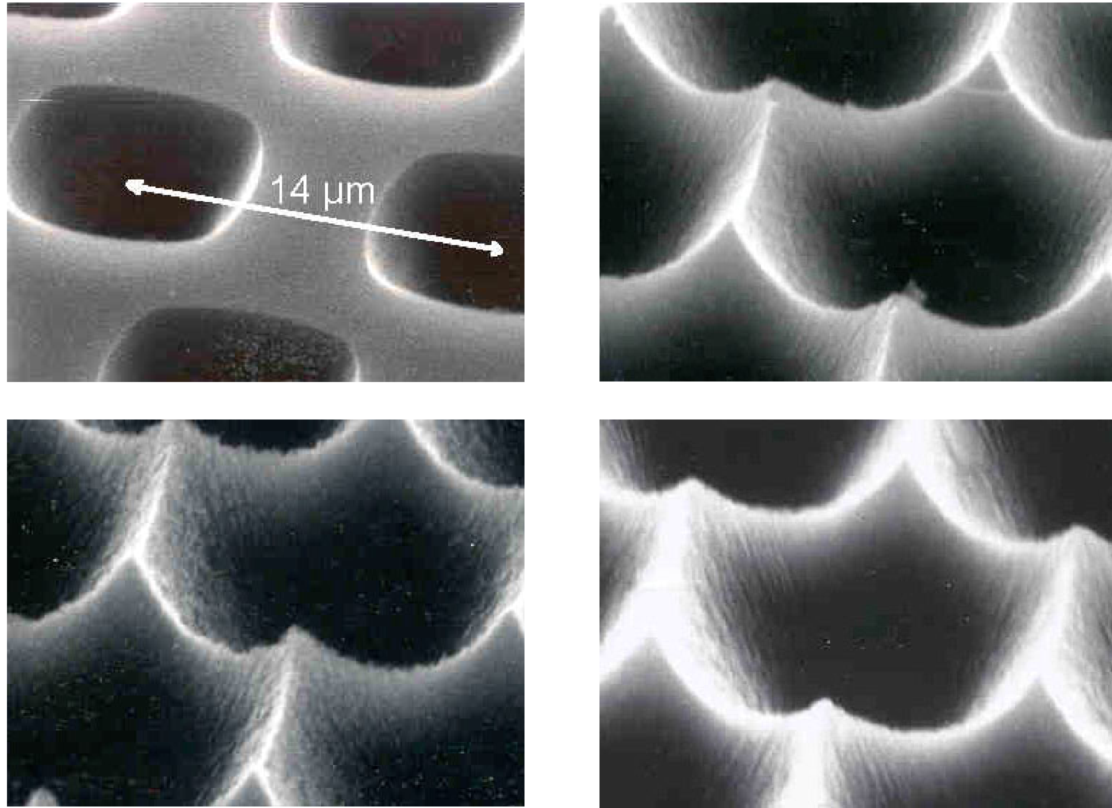

Fig. 4.16: SEM-pictures of wafer surface structured by a photoresist mask and a process of 320 W of RIE and 1000 W of MW power (etching time increases clockwise beginning at the upper left picture).

etching when the plasma is excited by a high (≈ 300 W) RIE power. When the microwave process is applied after the RIE process and not simultaneously the expected relation between depth and reflectance is observed since the sub-texture is removed (squares in Fig. 4.15).

As already mentioned, reflectance is one (important) thing but surface passivation needs to be very good, too. The electrical characterisation was performed by measuring the effective minority carrier lifetime τ_{eff} of four single-sided textured 1 Ω cm boron-doped FZ samples of 4 cm^2 size. The surfaces had a phosphorus diffused 120 Ω/sq emitter with a low surface concentration and thus the samples are n^+pn^+ structures. Surface passivation was achieved by either a 105 nm layer of thermally grown SiO_2 or a stack consisting of 15 nm SiO_2 and 60 nm silicon nitride (SiN_x). Planar reference samples were also processed and allowed the calculation of the recombination at the rear. The lifetime measurements were performed with the microwave photoconductance decay

method (µw-PCD, see Appendix A.1) at various bias light intensities and thus varying excess carrier densities Δn.

These values were used to calculate the absolute value of τ_{eff} at low injection level ($\Delta n = 5{\cdot}10^{14}$ cm^{-3}) from the differential $\tau_{eff,d}$ [85,86]. This approximated the conditions in the solar cell at maximum power point. Further calculations were performed to obtain the effective surface recombination velocity S_{eff} [87]. To calculate the upper limit of S_{eff}, the bulk lifetime was assumed to be restricted by Auger recombination only. Under low-level injection the emitter saturation current density j_{0e} can be calculated from S_{eff} via

$$j_{oe} = S_{eff} \cdot \frac{q \cdot n_i^2}{N_A} \qquad \text{4-2}$$

where q is the elementary charge, n_i the intrinsic carrier concentration and N_A the doping concentration of the bulk [88]. The samples were prepared with an oxide masking layer to allow for wet-chemical etching with the following sequence:

1) anisotropic RIE plasma etching
2a) microwave-enhanced RIE
2b) isotropic wet-chemical etching with HF/HNO_3

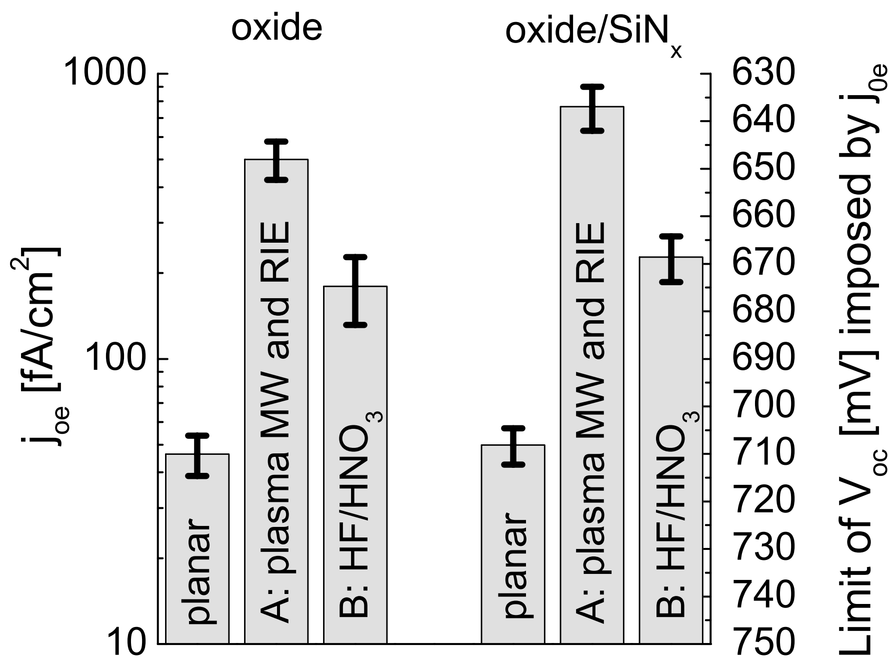

Fig. 4.17: j_{0e} in low injection ($\Delta n = 5{\cdot}10^{14}$ cm^{-3}) and imposed limit on V_{OC} after different surface preparation processes. The error bars represent the standard deviation from four samples.

As shown in Fig. 4.17, the solely plasma etched surfaces revealed significant damage after the texturing process resulting in a high value of j_{0e}. This damage was plasma-induced and due to the ion bombardment of the surface during the process [73]. When the second plasma etching step was replaced by the wet chemical etching, the damage was successfully removed and the emitter dark saturation current density was lower but still reached four times the j_{0e} of the planar reference[7]. This can be explained with the increased surface area which also quadrupled. The limit imposed on the open-circuit voltage V_{OC} of a solar cell was calculated via the equation

$$V_{oc,limit} = \frac{kT}{q} \ln\left(\frac{j_{sc}}{j_{oe}} + 1\right) \qquad 4\text{-}3$$

where kT/q is 25.9 mV at 25 °C and j_{SC} represents the assumed short circuit current density of 38 mA/cm^2 (compare equation 2-44). The results are presented on the right-hand axis in Fig. 4.17. The two passivation schemes of 105 nm SiO_2 and a stack of 15 nm SiO_2 and 55 nm SiN_x showed the same good performance, the latter allowing a subsequent deposition of a second antireflection layer for further reduction of reflectance.

4.3.4 Optical and electrical results measured in completed solar cells

For application in a solar cell process, the oxide layer was replaced by the photoresist mask. This had the advantage of a low temperature process which did not damage the bulk of temperature-sensitive multicrystalline silicon. As the photoresist is not stable in a wet-chemical bath (and would be removed when the structure is over-etched) the damage removal in HF/HNO_3 was replaced by a damage-free pure MW plasma in the absence of oxygen [73]. The resulting reflectance measurements are shown in Fig. 4.18 in comparison with an isotropically etched sample of the same pattern (see section 4.3.2), a planar reference and an inverted pyramid structure (both FZ silicon). The planar reference showed a weighted reflectance of $R_w \approx 36\%$ which was already significantly reduced by the isotropic honeycomb structure to $R_w \approx 20$ %. The application of the damage-free plasma texturing process, which worked with photoresist as the

[7] The j_{oe} of the reference was taken for the calculation of the planar rear surface of the textured sample.

masking layer, reduced reflectance further to $R_w \approx 14$ %, which was in the vicinity of the inverted pyramid texture ($R_w \approx 12$ %).

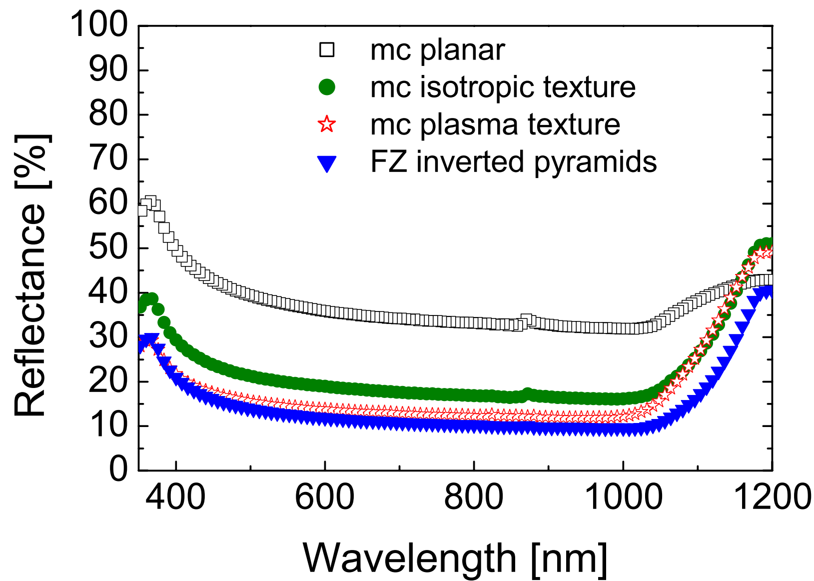

Fig. 4.18: Reflectance measurements of plasma-textured mc-silicon in comparison to a planar wafer, an isotropic “honeycomb” texture and inverted pyramids on monocrystalline silicon. Front and rear surface are blank.

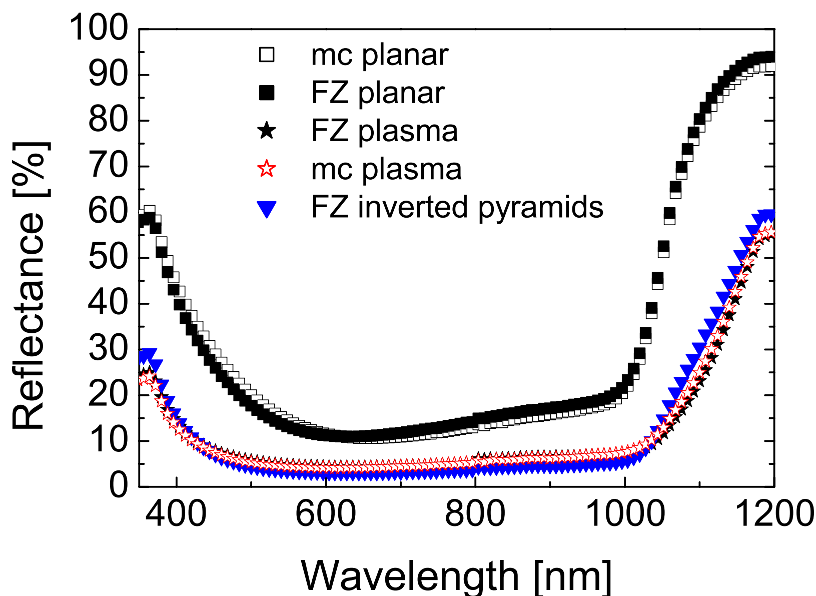

Fig. 4.19: Reflectance measurements of differently textured solar cells on FZ and multicrystalline silicon. The measurements include 2 % metallised area at the front which is covered with 105 nm of thermally grown SiO_2. The rear consists of a stack of 105 nm SiO_2 and 2 µm of evaporated aluminium.

For the investigation of the properties in solar cells, different textures were manufactured and implemented in a simplified high-efficiency process with laser-fired contacts on the rear [89]. In this process, the emitter was driven-in by an oxidation at 1050 °C which simultaneously passivated the front and rear surface with an oxide layer of about 105 nm. The rear surface became mirror-like by deposition of a 2 µm thick layer of evaporated aluminium, whereas reflectance on the front surface was reduced by the antireflection properties of the oxide. Reflectance measurements (Fig. 4.19) show that the light trapping for long wavelength photons (≥ 1000 nm) was as good for the plasma texture as for the inverted pyramid structure. The gain in current due to the reduced reflectance is the difference in the integrated reflectance multiplied by the internal quantum efficiency (QE) and weighted with the spectrum AM1.5g.

The measurements are plotted in Fig. 4.20 and the influence of the front surface recombination can be deduced from the short wavelength photons (≤ 500 nm). For the plasma-textured cells the internal QE was slightly reduced but still at about 95 %. This small reduction is explained by the increased front surface area due to texturing and the increased surface recombination velocity (compare Fig. 4.17).

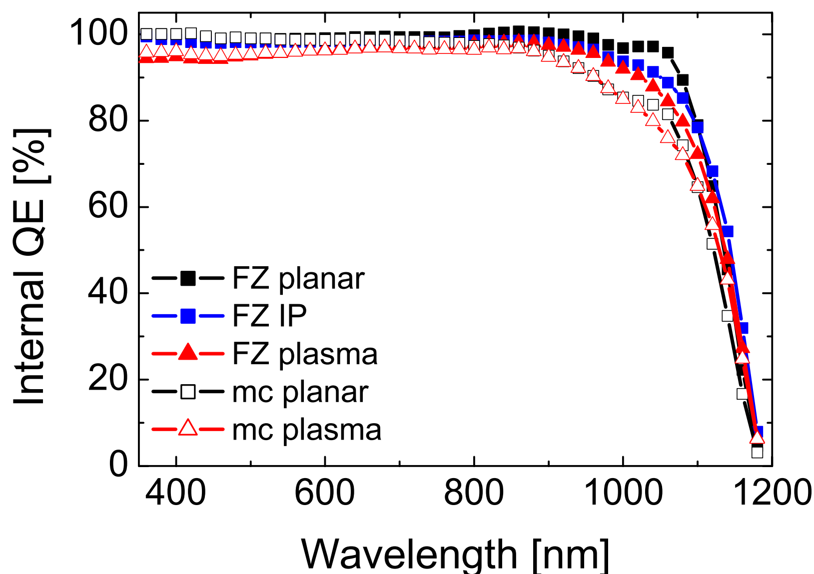

Fig. 4.20: Internal quantum efficiency of differently textured multicrystalline and monocrystalline (FZ) silicon solar cells. The front and rear surfaces are passivated by a 105 nm thick thermal oxide.

The solar cell parameters derived from illuminated *I-V* curve measurements (Table 4.3) reveal that the effect on V_{OC} was a loss of about 15 mV in comparison to the planar sample or the inverted pyramids.

Table 4.3: Results of the best LFC solar cells from FZ (1 Ω cm) and neighbouring wafers of mc-silicon (1.5 Ω cm). The size of the cells is 4 cm^2.

texture	material	V_{OC} [mV]	j_{SC} [mA/cm^2]	FF [%]	η [%]
planar	FZ	679	33.7	80.7	18.5
pyramids	FZ	677	38.7	78.9	20.7
plasma	FZ	663	38.3	80.1	20.4
planar	mc	609	31.7	74.1	14.3
plasma	mc	611	35.8	74.8	16.3

But the greatly enhanced short-circuit current density (a gain of about 4 mA/cm^2) more than compensated for this loss and solar cells with efficiencies greater than 20 % on FZ silicon were achieved with this front surface texture. SEM pictures of the final texture are shown in Fig. 4.21 and Fig. 4.22.

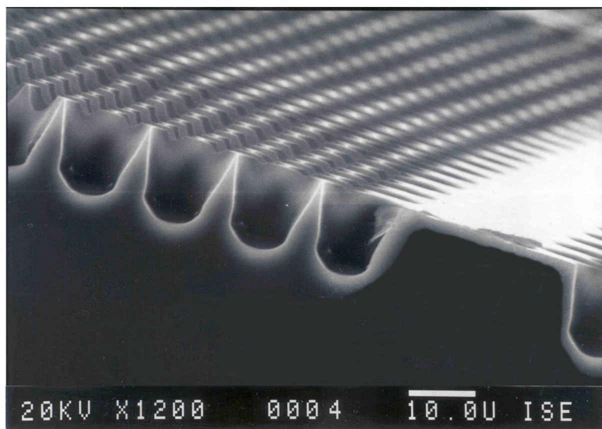

Fig. 4.21: SEM picture of the cross section of a textured FZ wafer. The plateau on the right is reserved for the metal contact.

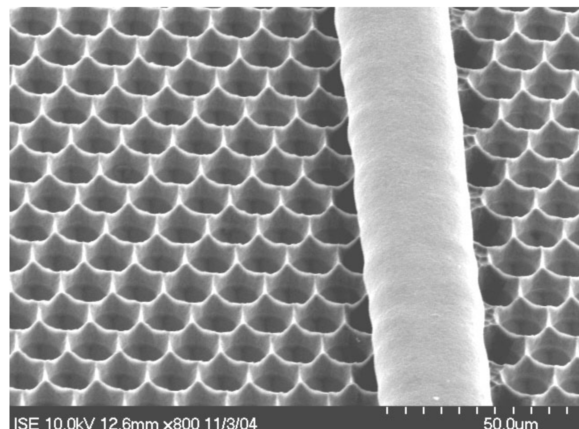

Fig. 4.22: SEM picture of a multicrystalline solar cell. The etched cones are of round shape since the etching process does not depend on the crystal orientation.

For the multicrystalline silicon solar cells the same effect was achieved and a gain of about 4 mA/cm^2 increased the efficiency by 2 % absolute. The open-circuit

voltage and the fill factor of the multicrystalline cells were comparatively low and the quantum efficiency measurements led to the conclusion that this was due to a reduced bulk lifetime and not caused by the texturing process.

The reason was the deterioration of the material by the drive-in oxidation for front and rear surface passivation at 1050 °C (compare chapter 3). Therefore a different passivation scheme at lower process temperatures is needed and has to be adjusted to the demands of the texture. This topic is addressed in chapter 5.

4.4 Chapter summary

Texturing of the front surface is very important to achieve a high solar cell efficiency. Although some good texturing techniques already existed, a new process in a plasma reactor was developed. As a masking layer photoresist was used. This enabled the well defined etching of structures of the desired shape independent of the crystal orientation of the multicrystalline silicon at low process temperatures. The optical properties of the plasma-textured surface were shown to be comparable to the inverted pyramids structure usually applied for solar cells of highest efficiencies on monocrystalline silicon. It was shown that the surface was etched without residual damage and that the increase in surface recombination by about a factor of four is only due to the increased surface area.

5 Emitter diffusion and passivation of textured surfaces

5.1 Introduction

As was shown in the previous chapter, the texturing of the front surface is an important measure to enhance the efficiency of silicon solar cells. Now the question arises, which emitter diffusion is ideally suited for the chosen texturing scheme. It is of high importance to apply anti-reflection layers of suitable refractive indices to maximise light absorption in the cell. This requirement is insufficiently met by a thick passivation oxide of about 100 nm especially since the optical benefit of the layer vanishes when the cell is encapsulated behind a glass of the same refractive index. Thus the goal of the optimisation described in this chapter is an emitter which can be passivated by a thin thermal oxide. It has to be thin enough (≤ 20 nm) to allow for an adopted double layer coating with titanium oxide/magnesium fluoride (TiO_x/MgF_2) to fully exploit the benefit of the well textured front.

5.2 Doping profiles of emitters driven-in by wet oxidation

Usually the emitter of high-efficiency silicon solar cells has a low surface concentration of phosphorus, N_S, and a silicon oxide layer for surface passivation. The standard way to diffuse such an emitter is a two-step process. In the first step a shallow emitter with a high surface concentration is diffused. In the Fraunhofer ISE clean room this is usually done in a tube furnace. Nitrogen flows through liquid $POCl_3$ and carries it to the quartz tube. A flux of pure oxygen is also led into the tube, oxidises the silicon and builds a phosphorus pentoxide layer. Furthermore chlorine compounds clean the surface when they are formed with metals which might be present on the wafer. The P_2O_5 layer created with this process serves as an unlimited source for phosphorus atoms (compare Fig. 5.1 left).

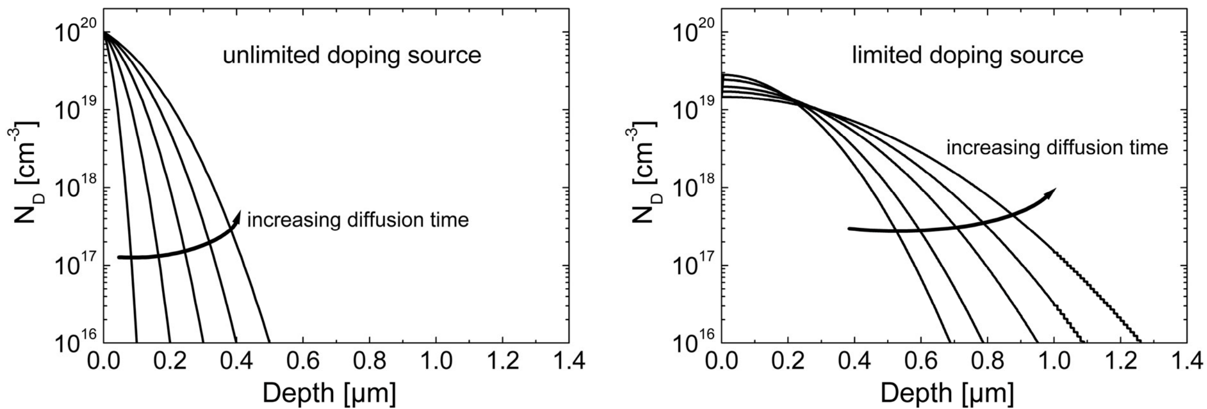

Fig. 5.1: Sketch of development of phosphorus doping concentration N_D with increasing diffusion time for an unlimited doping source (calculations performed with PC1D [90]) and for a limited doping source (calculations according to Sze [91]).

The process temperatures are around 800 °C. After removal of the phosphorus-silicate-glass (PSG), which is formed during the diffusion, this shallow emitter serves as a limited doping source for the second step, the drive-in diffusion. This diffusion is performed at very high temperatures (about 1000 °C) and a gaussian profile, i.e. a deep emitter with low surface doping concentration, evolves. Since the drive-in diffusion in the standard high-efficiency process at ISE is performed in oxygen ambient, the front and rear surface simultaneously become very well passivated by growing a silicon oxide layer of about 105 nm thickness. Unfortunately, the process temperature of 1050 °C is much too high for multicrystalline silicon (see chapter 3) and the standard process will have to be replaced by a new process sequence. A low surface concentration is desirable as surface recombination decreases with decreasing doping concentration [92]. This finding definitely holds for planar surfaces but not necessarily for textured samples [12,93]. Therefore different emitters were processed on samples with planar surfaces as well as on single-sided plasma-textured samples, a process which was developed within this work (see chapter 4). The material used was 1 Ω cm FZ silicon produced by Wacker Siltronic and 1.5 Ω cm multicrystalline silicon produced by ScanWafer.

In a first approach, shallow emitters were diffused for one hour at 800 °C and 820 °C. The subsequent oxidation at 1050 °C was replaced by a modified wet oxidation (details see section 6.2.1) for four hours at 800 °C, 850 °C and 900 °C. An oxide layer for the rear surface in the range of 100-150 nm on the *p*-type bulk

material had proven to be well suited for the LFC process. To avoid further growth, the gas ambient was switched from oxygen to nitrogen during the process according to Table 5.1. Whereas a suitable oxide thickness between 100 and 150 nm was obtained on 1 Ω cm *p*-type base material, the oxide on the (still highly doped) emitter was about 200-300 nm thick. This was far too much for a good anti-reflection coating. Therefore, the oxide was removed in HF and the wafers were oxidised for 20 min at 900 °C with a dry oxidation process which resulted in oxides of about 10-15 nm. This was thin enough to allow for an adapted double layer antireflection coating in order to minimise reflectance. In the second approach, the drive-in oxidation was not performed and the thin oxide was grown directly after removal of the PSG.

Table 5.1: Process parameters for the wet oxidation processes used for drive-in diffusion. The oxide thickness was measured on <100> orientated 1 Ω cm FZ silicon.

T [°C]	t_1 (with oxygen) [h]	t_2 (without oxygen) [h]	$t_1 + t_2$ [h]	oxide thickness [nm]
800	3.5	0.5	4	104
850	2	2	4	128
900	1	3	4	138

The emitter profiles of the different diffusions were measured by secondary ion mass spectroscopy (SIMS) by the company RTG, Berlin, Germany (Fig. 5.2). After the first emitter diffusion at 800 °C, the total amount of donor atoms was the same in all wafers. The profiles in graph A (upper left) did not show the expected characteristics of an emitter with drive-in diffusion. According to theory the integrated amount of phosphorus atoms should still be the same after the drive-in but the distribution should be different, i.e. the deeper profiles should have a smaller surface concentration of donors N_S after oxidation. But the deeper profiles also had a higher surface concentration and consequently a higher overall doping.

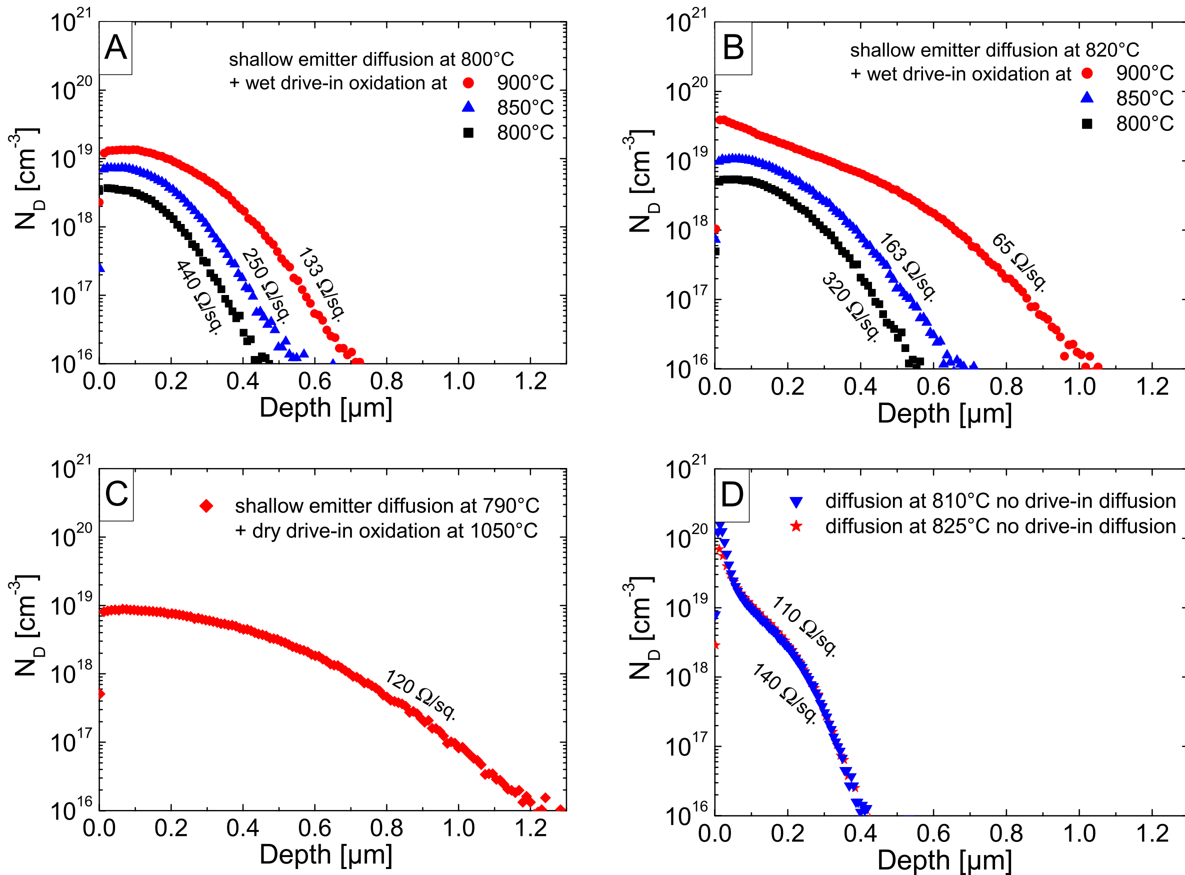

Fig. 5.2: Emitter profiles measured by SIMS and sheet resistance measured with a four point probe. The emitters in the upper half were oxidised for four hours with a wet oxide. The emitter in the lower left was driven-in with a dry oxide for 1 hour. The thick oxides were removed and a thin oxide below 20 nm was grown for surface passivation. The lower right graph shows the profile of the shallow emitters which were not driven-in.

Nevertheless, the profile had a gaussian shape, indicating a limited source for the drive-in as expected. For the emitter diffusion at 820 °C in graph B, the profiles followed the same trends on a higher doping level. This was due to the higher amount of phosphorus which diffused during the first step. The standard dry oxidation process at 1050 °C is shown in picture C. It revealed a higher sum of doping atoms than the profiles after emitter diffusion at 800 °C although the first emitter diffusion took place at 790 °C (and therefore should provide a smaller amount of donors). In picture D the two profiles of emitters without a long drive-in diffusion are presented. They were only oxidised shortly in dry ambient to passivate the surface. The surface concentration of donor atoms was in the range of 10^{20} atoms/cm^3. The diffusion at 825 °C was performed in a different furnace than all the other diffusions, thus the diffusion process parameters are not directly comparable.

The measured emitter sheet resistance of all profiles corresponded well with calculations performed using the mobility model of Masetti et al. [94], this adds to the reliability of the measurement and proves that no samples were mixed up. For an explanation of the unexpected doping profiles of the wet drive-in oxidation, the redistribution of doping atoms during oxidation has to be considered. The doping profile after oxidation depends on the oxidation rate, the relative dopant diffusion rates in the oxide and the silicon and thus on temperature, oxidation ambient etc.. The dopant segregation coefficient m (m = ratio of equilibrium concentration of dopant between silicon and oxide) for phosphorus is greater than unity (m > 1) and thus usually a pile-up of phosphorus occurs [95]. However, in the case of wet oxidation of highly doped layers some of the phosphorus was apparently built into the silicon oxide and could consequently not contribute to the doping profile. The reason for depletion of the phosphorus instead of pile-up can probably be found in the very fast oxidation rates.

5.3 Emitter recombination of planar and textured samples

The 1 Ω cm FZ samples with diffused emitters on both sides received a forming gas anneal for 25 min at 425 °C. Afterwards the effective carrier lifetime was measured with the QssPC technique at an excess carrier density of $\Delta n = 1 \cdot 10^{15}$ cm^{-3} and evaluated according to

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + D_e \cdot \gamma_m^{\ 2} \qquad \text{5-1}$$

$$\tan(\gamma_m \cdot W) = \frac{D_e \cdot \gamma_m \cdot (S_{front} + S_{rear})}{(\gamma_m \cdot D_e)^2 - S_{front} \cdot S_{rear}} . \qquad \text{5-2}$$

W is the wafer thickness, D_e is the diffusion constant for electrons, S_{front} and S_{rear} are the surface recombination velocity at the front and at the back surface respectively, and γ_m is the smallest found eigenvalue of the upper equation [87,96]. For the planar samples both surfaces contributed to the same extent to surface recombination and S_{front} and S_{rear} are equal. This value was then used as the S-value of the non-textured side of the plasma-textured sample, thus the influence of the texture on emitter recombination could be deduced. The measurements of the

effective minority carrier lifetime were converted to emitter dark saturation current densities j_{0e} via (see also equation 2-41)

$$j_{0e} = \frac{n_i^2 \cdot q}{N_A} \cdot S_{eff} \,. \tag{5-3}$$

Table 5.2 summarises the results and the emitter profile parameters.

Table 5.2: Summary of emitter profile parameters measured by SIMS. The measured dark emitter saturation current density for planar and plasma textured surfaces were calculated from the minority carrier lifetime measurements.

No.	T_{diff} [°C]	$T_{drive\text{-}in}$ [°C]	$t_{drive\text{-}in}$ [h]	R_{sheet} [Ω/sq]	N_S [cm^{-3}]	x_j [µm]	$j_{0e,\ planar}$ [fA]	$j_{0e,\ textured}$ [fA]
1	800	900	4	133	$1.3\cdot10^{19}$	0.70	56	284
2	800	850	4	250	$7.4\cdot10^{18}$	0.55	34	288
3	800	800	4	440	$3.7\cdot10^{18}$	0.45	23	280
4	820	900	4	65	$4.0\cdot10^{19}$	1.05	102	166
5	820	850	4	163	$1.0\cdot10^{19}$	0.65	57	215
6	820	800	4	320	$5.0\cdot10^{18}$	0.55	48	202
7[8]	825	---	---	140	$7.0\cdot10^{19}$	0.42	101	187
8	810	---	---	110	$1.5\cdot10^{20}$	0.43	115	593
9	790	1050	1	120	$9.0\cdot10^{18}$	1.25	57	262

The limit imposed by j_{0e} on the open-circuit voltage V_{OC} of a solar cell was calculated via the equation

$$V_{oc,limit} = \frac{kT}{q} \ln\left(\frac{j_{sc}}{j_{oe}} + 1\right) \tag{5-4}$$

where kT/q is 25.9 mV at 25 °C (compare equation 2-44). The short-circuit current density was assumed to be $j_{SC} = 38$ mA/cm^2 and the results are presented on the right-hand axis in the graphs. For the planar samples (Fig. 5.3, solid symbols) a

[8] The diffusion at 825 °C was performed in another tube furnace with a different control system for the phosphorus layer deposition. Thus the combination of diffusion temperature and emitter profile is not directly comparable to the others.

strong correlation between emitter sheet resistivity and saturation current density could be established.

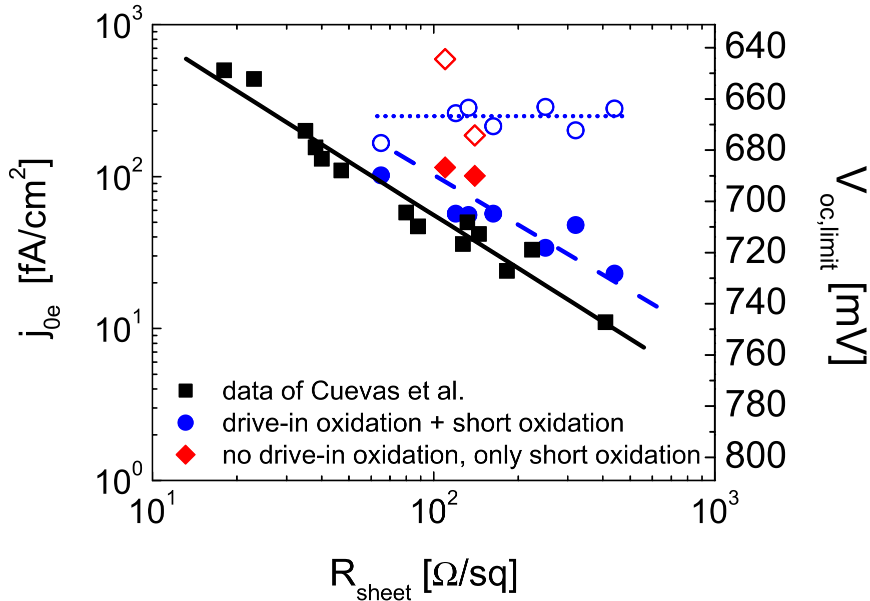

Fig. 5.3: Dark saturation current density j_{oe} and imposed limit on V_{OC} of emitters passivated by a thin thermal oxide as a function of emitter sheet resistivity. Planar (solid symbols) and plasma-textured samples (hollow symbols) were investigated. The lines are guides-to-the-eye (solid: data of Cuevas [97], dash: this work planar, dots: this work plasma textured).

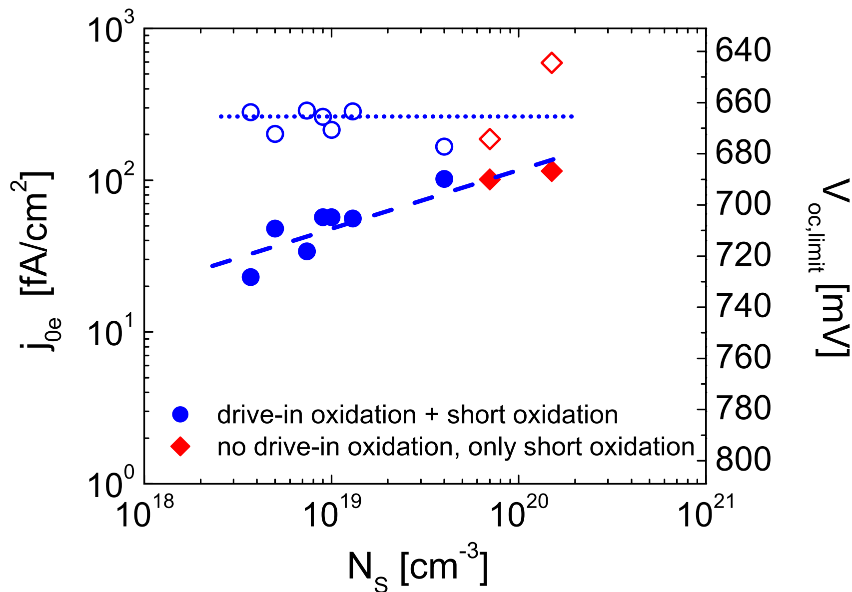

Fig. 5.4: Dark saturation current density j_{oe} and imposed limit on V_{OC} of emitters passivated by a thin thermal oxide as a function of phosphorus surface concentration N_S. Planar (solid symbols) and plasma-textured samples (hollow symbols) were investigated. The lines are guides-to-the-eye.

This was in good agreement with data published by Cuevas et al. [97] which was derived from a very similar experiment. For the planar samples, the emitter saturation current density decreased linearly with increasing sheet resistivity. The emitters without drive-in oxidation exhibit slightly higher recombination values than the driven-in counterparts. The reason could be found in the dependence of recombination on the phosphorus surface concentration as shown in Fig. 5.4. For the plasma-textured samples (Fig. 5.3, hollow symbols) the recombination was much higher than for the planar samples, which was partly due to the increased surface of the texture. The textured samples did not benefit from higher sheet resistivities, i.e. j_{0e} was hardly affected by the differences in the emitter properties. This is also evident in Fig. 5.4 where the emitter recombination did not benefit from a reduced surface concentration of $N_S \leq 10^{20}$ cm^{-3}. For the plasma-textured samples a relation between j_{oe} and the depth of the emitter x_j (measured on planar samples where the phosphorus concentration reached the bulk boron doping level of $N_A = 1.5 \cdot 10^{16}$ cm^{-3}) could not be established either. This led to the conclusion that the geometry of the texture (see Fig. 5.5) with its many sharp peaks, had a major impact on emitter recombination. Those peaks were probably always highly doped, even for the lowly doped planar emitters, since the phosphorus pentoxide layer delivered the phosphorus atoms from all sides. Consequently, the plasma-textured samples were limited by this geometrical issue. The choice of the best emitter diffusion process can take other factors into account, e.g. the gettering of impurities which can occur during phosphorus diffusions or the thermal degradation of multicrystalline silicon at high temperatures.

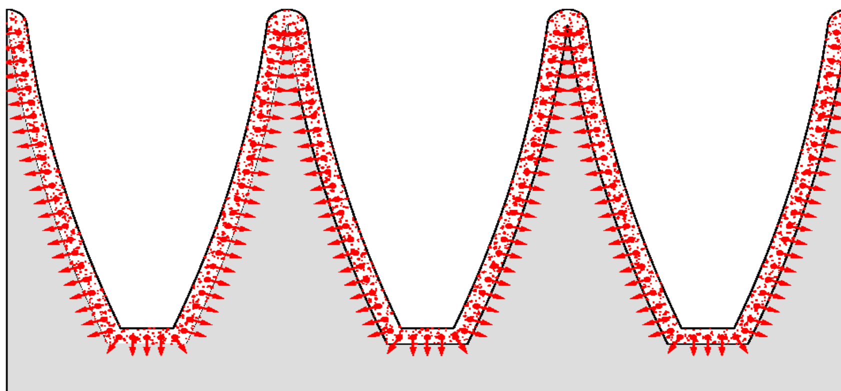

Fig. 5.5: Schematic drawing of emitter diffusion for a plasma textured surface. The very sharp peaks are highly doped after any emitter diffusion and determine j_{0e}.

5.4 Effect of emitter diffusion on minority carrier lifetime in multicrystalline silicon

One important effect of the emitter diffusion is the change of minority carrier lifetime in multicrystalline silicon caused by thermal degradation and/or gettering of impurities (see chapter 3). For the emitter diffusions of the previous chapter, plasma-textured and planar neighbouring wafers of the same brick were processed in the same run with the FZ-samples. The effective minority carrier lifetime was measured with the QssPC method and evaluated at an excess carrier density of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}. The textured samples with emitter showed lower effective minority carrier lifetimes than the planar samples. The measurements of the multicrystalline wafers reflect the properties of the emitter and the texture. To separate recombination in the bulk from surface recombination, the emitter was etched away from the planar samples and the wafers were covered with a silicon nitride, which effectively suppressed surface recombination ($S \approx 10$ cm/s).

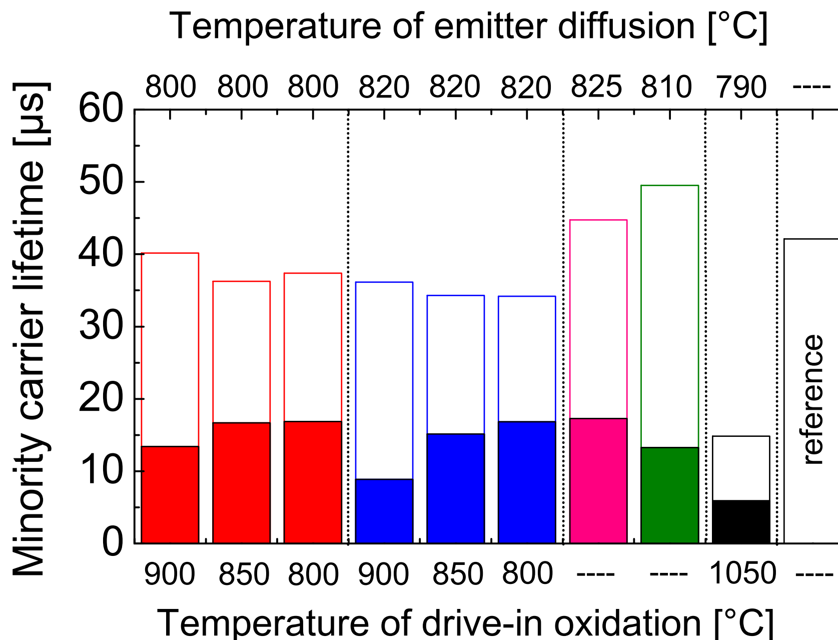

Fig. 5.6: Measurement of minority carrier lifetime in multicrystalline silicon. The measurements are arithmetic average values of QssPC measurements on every wafer evaluated at an excess carrier density of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}. All emitters were passivated by a thin thermal oxide layer. The filled bars denote the effective carrier lifetime τ_{eff} of plasma-textured samples, the hollow bars show the bulk lifetime of silicon nitride passivated planar samples after the emitter was etched away.

Thus, the measured lifetimes represent the bulk lifetime τ_{bulk} in very good approximation. The result is displayed in Fig. 5.6. For the measurements including the emitter on the surface, the emitter saturation current densities were re-calculated. But this led to much higher j_{0e}-values than for the FZ samples discussed in the previous section. The reason is probably found in an increment of τ_{bulk} due to a hydrogen passivation during silicon nitride layer deposition, a topic being under discussion at the moment (see [98-100] and section 7.2). This would lead to an overestimate of the recombination in the emitter. Nevertheless, the determination of the bulk lifetime from the samples passivated with silicon nitride allowed for an assessment of the deteriorating effect caused by the oxidation and the beneficial gettering effect of the emitter diffusion. The obtained data shows, that the wet drive-in oxidations for fours hours at temperatures between 800 °C and 900 °C did not degrade the minority carrier lifetime. At least not irreversibly as the silicon nitride deposition could have caused a hydrogenation of the bulk, which improved the carrier lifetime. Thus the wet oxidation could be used for emitter drive-in. The oxidation for one hour at 1050 °C significantly reduced the material quality and should be excluded from processing of multicrystalline silicon solar cells.

Compared to the reference sample an increased carrier lifetime was only detected for the single-step emitters which were not driven-in. This was probably caused by the beneficial effect of the gettering. These processes could be used for solar cells where the rear surface passivation took place before emitter diffusion or when it is a low-temperature process which does not alter the doping profile.

Now the last question remaining to be answered before choosing the best emitter diffusion for the solar cells, is the contact formation on the front. This is the topic of the next section.

5.5 Effect of emitter diffusion on the fill factor

The next factor which has to be considered in order to build a high-efficiency solar cell from multicrystalline silicon, is the formation of electric contact of the metal grid on the front. Since the grid fingers are on a planar surface which was preserved from texturing, solar cells with an overall planar front were manufactured for reasons of simplicity. The material was 1 Ω cm FZ and the emitter was diffused and oxidised together with the lifetime measurement samples

of the previous chapter. The rear contact was formed by the laser-fired contact process (LFC, [101]) after evaporation of a 2 µm thick aluminium layer. The front contact was formed by a thin evaporated stack system of titanium, palladium and silver (Ti/Pd/Ag) on a lithographically structured photoresist. After a lift-off process the contacts were thickened by electroplating. The double layer antireflection coating on top of the thin thermal oxide increased the short-current density to about 36 mA/cm^2, a value expected for the textured multicrystalline silicon cells. The cells were annealed in forming gas for 15 min at 350 °C to allow for good contact formation. The resulting average fill factors of the cells under standard testing conditions are shown in Fig. 5.7. All emitters allow for high fill factors of about FF ≈ 80 %.

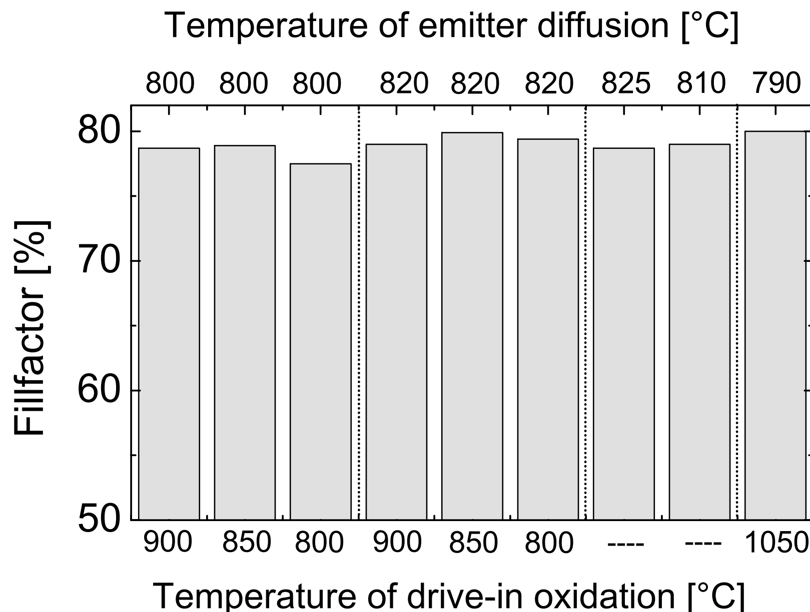

Fig. 5.7: Fill factor of solar cells on 1 Ω cm FZ with different emitter diffusion (compare section 5.4). Each value is the average of seven solar cells. All emitter diffusions can be very well contacted with the evaporated Ti/Pd/Ag stack system and allow fill factors of about 80 %.

5.6 Chapter summary

Several doping profiles of phosphorus diffused emitters suitable for high-efficiency silicon solar cells on *p*-type substrates were presented. The use of the wet oxidation process at temperatures between 800 °C and 900 °C to drive-in shallow emitters resulted in a lower overall doping of the silicon than the use of a

standard dry oxidation at 1050 °C. This was due to the enhanced incorporation of phosphorus into the fast growing oxide and enabled a high flexibility in emitter design. The emitter sheet resistance was tailored to values between 65 Ω/sq and 440 Ω/sq. The emitter dark saturation current densities measured after the surface passivation with a thin thermal oxide revealed the expected dependence on sheet resistivity and phosphorus surface concentration on planar surfaces. However, for the plasma-textured surfaces no significant dependence on the emitter profile was detected. Emitters without drive-in oxidation showed equally good electrical properties and the limit imposed by the dark emitter saturation current density j_{0e} on the achievable open circuit voltage was beyond $V_{OC} > 660$ mV. The minority carrier lifetimes of multicrystalline silicon were the highest for these emitters with a steep profile and high fill factors of processed solar cells were achieved. These shallow emitters were diffused after the oxidation of the rear, which this way was masked against the diffusion and simultaneously electrically passivated. The emitter diffusion at 825 °C was selected for further development of a multicrystalline silicon solar cell structure with a plasma-textured front.

6 High-efficiency multicrystalline silicon solar cells

6.1 Introduction

As was shown in the previous chapters, the standard processes used for monocrystalline FZ silicon of high purity and very low dislocation density are not applicable to multicrystalline silicon because anisotropic texturing does not work and high-temperature oxidations degrade the bulk lifetime. The response of the bulk to high-temperature oxidations for rear surface passivation was investigated in chapter 3, the adapted front surface texture and emitter diffusion were described in chapters 4 and 5. Two additional processes, which are necessary to form the rear surface structure, the wet oxidation and the laser-fired contacts, are investigated in more detail in this chapter.

Based on these process steps a process sequence is developed. The minority carrier lifetime of the multicrystalline silicon is monitored throughout this process sequence. Numerous solar cells are produced from block cast material of different manufacturers and the obtained efficiencies are presented in the last section.

6.2 Rear surface structure for multicrystalline silicon solar cells

One of the most important features of a high-efficiency silicon solar cell is the passivation of the rear surface. Several approaches with silicon nitride passivation of the silicon surface [20,102,103] gave good results, but oxide passivated references still resulted in higher efficiencies. Dauwe [104] showed that the lower performance of the silicon nitride passivated cells was mainly due to a parasitic shunting of the floating junction, which is induced by the high density of fixed positive charges in the silicon nitride layer. One technological measure to solve this problem is the formation of a local back-surface-field (LBSF) around the contact (to electrically isolate the contact). Another is the use of layers which mainly passivate the surface via a reduction of the interface density of states D_{it} and not via a field effect, such as very silicon rich silicon nitride or amorphous

silicon. Unfortunately, increased process complexity (LBSF) or a reduced thermal stability of the layer are significant drawbacks of such an approach.

Another approach is the use of improved aluminium alloying to reduce the recombination at the rear. The best result of 18.6 % efficiency on 1 cm^2 area was obtained with a rapid thermal process (RTP) firing of screen-printed aluminium paste [22]. However, a high temperature and extremely fast ramp-up and ramp-down rates were applied to achieve a low surface recombination velocity. Defect-rich areas of the multicrystalline wafer were degraded and decreased the average efficiency which could be obtained from an entire large-area wafer. The reflectivity of alloyed aluminium is comparatively low which reduces light-trapping. The different thermal expansion coefficients of aluminium and silicon lead to mechanical stress. This results in bowed wafers, a critical point especially when very thin wafers ($W \leq 150$ µm) are considered.

Thus, silicon oxide still is the best choice if a process is found which does not deteriorate the bulk lifetime of multicrystalline silicon. The solution is the oxidation in wet ambient (as opposed to dry oxidation) since the growth rates are increased by about one order of magnitude and much lower oxidation temperatures can be chosen. This approach was previously followed by Stocks [37] and simultaneously and independently of the author of this thesis by Schmiga [38].

6.2.1 Wet oxidation process

The oxidation of the silicon surface is a well known process in the semiconductor industry. Usually it takes place at temperatures of about 1000 °C to obtain very dense and high-quality layers. To reduce the time for a growth of masking layers the oxidation in steam ambient is frequently used.

The water in the furnace used throughout this thesis was created by a pyrogenic system which burns hydrogen H_2 and oxygen O_2 molecules at the gas inlet end of the oxidation tube. This provides water vapour of high purity and control. The chemical reaction during oxidation of the silicon surface can be summarised as

$$Si + O_2 \rightarrow SiO_2 \qquad \text{6-1}$$

$$Si + 2\,H_2O \rightarrow SiO_2 + 2\,H_2 \qquad \text{6-2}$$

for dry and wet oxidation, respectively. The growth of the oxide layer is non-linear. It has been proposed by Deal and Grove [105] that during thermal oxidation three consecutive reactions occur. The fluxes are equal under steady-state conditions:

1. Transfer of the oxidant from the gas phase to the outer oxide surface.
2. Diffusion of the oxidising species through the already formed oxide.
3. Reaction of the oxidising species with silicon at the Si-SiO_2 interface.

The following general relationship has been derived:

$$X^2 + AX = B(t+\tau). \tag{6-3}$$

X is the oxide thickness and τ is defined as

$$\tau = \frac{X_0{}^2 + AX_0}{B} \tag{6-4}$$

where X_0 is the original oxide thickness at $t = 0$ and A and B are constants. The solution of this equation is

$$X = \frac{A}{2}\left(\sqrt{1+\frac{4B}{A^2}(t+\tau)} - 1\right). \tag{6-5}$$

For short times $(t+\tau) << A^2/4B$ this simplifies to

$$X = \frac{B}{A}(t+\tau) \tag{6-6}$$

and B/A is therefore the linear rate constant. For the second limiting case of long duration and $(t+\tau) >> A^2/4B$ it follows:

$$X^2 = B(t+\tau). \tag{6-7}$$

Thus B is the parabolic rate constant. The correction time τ is related to the initial oxide thickness X_0. For oxidation in dry oxygen thin oxides (< 30 nm) are not satisfactorily described by equation 6-3. Rather, the plot of oxide thickness versus oxidation time tends to extrapolate through the thickness axis at about X = 15 nm [95] (at $t = 0$, see Fig. 6.1).

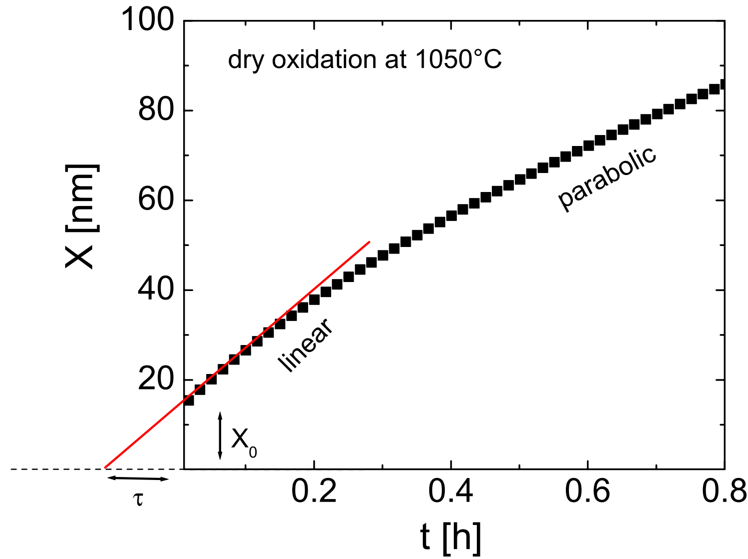

Fig. 6.1: Oxide thickness versus oxidation time for dry oxidation. In the thin oxide regime (up to about 30 nm) the general equations do not give a good description of experimental results. Thus the correction factor τ or the initial oxide thickness X_0 are introduced to account for this rapid initial growth.

For wet oxidation this rapid initial growth was usually not observed [106], more recent studies of Ngau et al. [107] detected it for the <110> crystal orientation.

The parameters A and B depend on many factors like temperature, doping of the silicon, pressure, oxidation ambient, etc.. The strongest dependence can be observed for the temperature and the crystal orientation and, very important, the oxidation ambience. Some reference data published in a review article by Moynagh [108] are given in Table 6.1.

Table 6.1: Linear rate (B/A) and parabolic rate (B) constants for wet and dry oxidation for lightly doped silicon ($N_D \leq 1 \cdot 10^{20}$ cm^{-3}).

ambient	T [°C]	B/A [µm/h]	B [µm^2/h]
dry	< 950 °C	$4.666 \cdot 10^5 \cdot \exp(-1.76 \text{ eV}/kT)$	$1.373 \cdot 10^7 \cdot \exp(-2.22 \text{ eV}/kT)$
wet	< 900 °C	$1.236 \cdot 10^6 \cdot \exp(-1.60 \text{ eV}/kT)$	$1.698 \cdot 10^4 \cdot \exp(-1.17 \text{ eV}/kT)$
dry	> 950 °C	$5.997 \cdot 10^9 \cdot \exp(-2.75 \text{ eV}/kT)$	$2.484 \cdot 10^2 \cdot \exp(-1.10 \text{ eV}/kT)$
wet	> 900 °C	$1.056 \cdot 10^8 \cdot \exp(-2.05 \text{ eV}/kT)$	$4.200 \cdot 10^2 \cdot \exp(-0.78 \text{ eV}/kT)$

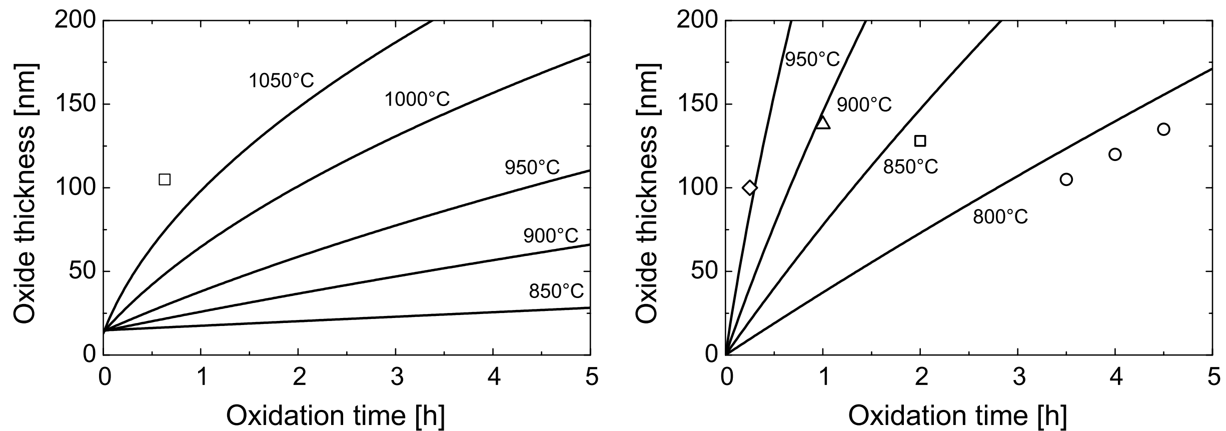

Fig. 6.2: Calculated oxide thickness as a function of oxidation time and temperature for dry (left-hand) and wet ambience (right-hand). The data was taken from Table 6.1 for <100> oriented silicon. The hollow symbols are experimental data points obtained within this thesis.

The linear rates depend on the crystal orientation since the growth rate is limited by the oxidation of the surface [107]. The parabolic rate constants are independent of crystal orientation since the diffusion of the oxidising species is the limiting process. The <111> orientation has the highest growth rates, followed by <110> and <100>. Calculations for <100> oriented silicon surfaces are illustrated in Fig. 6.2. The match between experimental data and the calculations is limited. For the dry oxidation this can be explained by the chlorine which was present during oxidation because of DCE (trans-1,2-dichloroethylene) added to the atmosphere. A proposed mechanism for the reaction of HCl in a dry oxidation is

$$O_2 + 4\,HCl \rightarrow 2\,H_2O + 2\,Cl_2 \qquad \text{6-8}$$

The chlorine reduces the growth of oxidation induced stacking faults and removes some metallic impurities. The formed H_2O increases the oxidation rate. DCE was not added during the wet oxidation since the chemical reaction described above would then be driven to the left, reducing the amount of water and slowing down the oxide growth rate [95]. The match between the experimental data and the calculation is good for the wet oxidation at 950 °C and 900 °C. For the 850 °C and 800 °C process about 20 nm less oxide are grown than expected. However, the general trend is described and the deviations might be due to differences in the amount of steam added to the oxygen atmosphere or gas flow rates in general.

6.2.2 Surface passivation using wet oxidation

One important property of the wet oxidation process is the passivation of the silicon surface. For sufficiently low values of the surface recombination velocity S the following equation holds [87]:

$$\frac{1}{\tau_{eff}} \cong \frac{1}{\tau_{bulk}} + \frac{2S}{W}. \qquad 6\text{-}9$$

To extract the value of S from the measured effective carrier lifetime τ_{eff} via this equation the bulk lifetime τ_{bulk} and the wafer thickness W have to be known. For high-purity FZ silicon the assumption of a negligible contribution of recombination in the bulk to the total recombination usually is a valid assumption. But for multicrystalline silicon τ_{bulk} is often low enough to dominate the measured effective carrier lifetime. A determination of the bulk lifetime from neighbouring wafers which were covered with silicon nitride (silicon nitride can very effectively suppress surface recombination), was not applied due to the uncertainty of a possible hydrogenation of the bulk during layer deposition (see section 7.2). Furthermore, a possible detrimental effect of the oxidation on the bulk lifetime would falsify the results. Thus, a different approach was followed, where the separation between bulk and surface recombination was achieved experimentally by a variation of sample thickness W for a set of neighbouring wafers with the same crystal structure and identical surface structure. This was achieved by solely mechanical grinding [109] of gettered multicrystalline silicon wafers (produced by ScanWafer) of 1.5 Ω cm base resistivity. Subsequently the wafers were etched for five minutes in 80 °C hot 40 % potassium hydroxide (KOH). The wafers were wet-chemically cleaned and oxidised for 3.5 h in steam ambience. This resulted in an oxide thickness of 105 nm on <100> oriented silicon. After a forming gas anneal at 425 °C for 60 min the effective carrier lifetime was measured with the QssPC technique at an excess carrier density of $\Delta n = 1 \cdot 10^{15}$ cm^{-3} to avoid trapping artefacts. The wafer thicknesses varied between 42 and 192 µm, thus generation of free carriers within the sample was thickness dependent which had to be taken into account for the evaluation (see Appendix A3).

The plot of the inverse effective lifetime against the inverse wafer thickness is shown in Fig. 6.3.

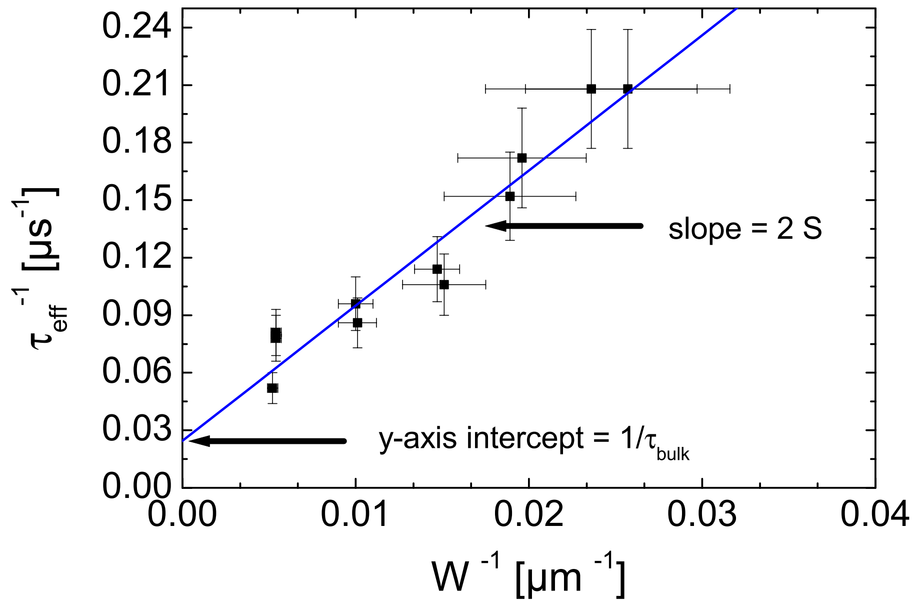

Fig. 6.3: Plot of inverse effective lifetime τ_{eff}^{-1} against inverse wafer thickness W^{-1} at $\Delta n = 1\cdot10^{15}$ cm^{-3} of neighbouring oxide-passivated multicrystalline silicon samples. The surface recombination velocity S can be determined by the slope and the bulk lifetime τ_{bulk} can be derived from the axis intercept.

The error bars result from the standard deviation measured for every wafer thickness and 15 % uncertainty in effective lifetime measurement. The linear fit of the data leads to an extracted bulk lifetime of $\tau_{bulk} = 41$ µs (± 15 µs) and a surface recombination velocity of S = 353 cm/s (± 32 cm/s). Stocks and Cuevas performed a very similar experiment and published values of $S = 125$ cm/s and $\tau_{bulk} = 280$ µs for 1.5 Ω cm multicrystalline silicon [37]. The deviations to the results obtained within this thesis might arise from a different surface treatment (Stocks used an acidic etch and thus the wafers had a smoother surface) and a different supplier of multicrystalline silicon.

The value of $S \approx 350$ cm/s is not directly the value representing the surface passivation in a completed solar cell. This can be seen in Fig. 6.4 where the measured effective lifetime of 1 Ω cm FZ samples in different states is shown. Directly after oxidation, the surface passivation was rather poor which resulted in low effective lifetimes. A forming gas anneal (60 min at 425 °C) improved the passivation. Assuming the bulk to be limited by Auger recombination only, surface recombination values of $S \leq 320$ cm/s ($\Delta n = 1\cdot10^{15}$ cm^{-3}) were achieved, about the same as on multicrystalline silicon.

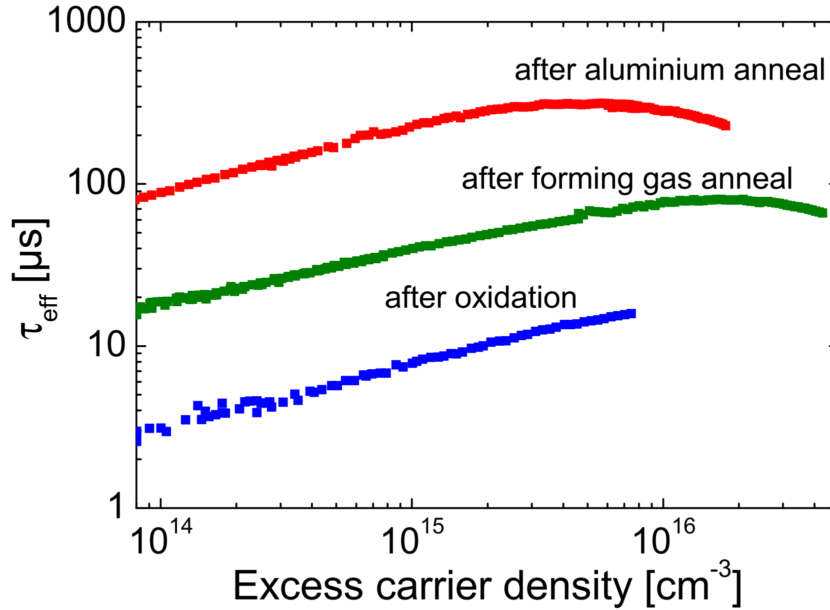

Fig. 6.4: Effective carrier lifetime τ_{eff} of a 1 Ω cm FZ wafer after different process steps. Under the assumption of a high bulk lifetime τ_{bulk} = 1800 µs, this yields values of S = 2500 cm/s directly after oxidation, S = 320 cm/s after forming gas anneal and S = 65 cm/s after aluminium anneal, the condition it has in the applied solar cell structure (evaluation at $\Delta n = 1\cdot10^{15}$ cm^{-3}).

After an aluminium anneal the surface passivation was further improved (a layer of 1 µm of evaporated aluminium was deposited on the surfaces, after that annealing in forming gas for 15 min at 425 °C was performed). This is usually explained by a reaction of aluminium with H_2O adsorbed at the SiO_2 surface which releases atomic hydrogen. The H-atoms then diffuse quickly to the Si surface and satisfy, or passivate, the remaining dangling bonds. The formation of Si-H bonds with atomic hydrogen is more efficient than with molecular hydrogen, which is used for a forming gas anneal [97]. This passivation effect is reported to be unstable under prolonged exposure to UV-light [110] but it was not applied to the front of the solar cells within the work of this thesis, only to the rear which is never reached by UV-light[9]. The surface recombination in our sample was reduced to $S \leq 65$ cm/s. However, in a completed solar cell the effective rear surface recombination velocity, $S_{rear,eff}$ is greater than this value, because the recombination at the contact points has to be taken into account. This is done in the next section.

[9] UV-light does not penetrate deep enough from the front and the metallic aluminium on the back would block UV-light coming from the rear.

6.2.3 Recombination velocity of oxidised surfaces with laser-fired point-contacts

In order to determine the recombination parameters for the LFC process and the wet oxidation, FZ samples with base resistivities in the range from $\rho \approx 0.5\ \Omega$ cm to $\rho \approx 7\ \Omega$ cm were thermally oxidised. This was done in a dry oxidation process at 1050 °C and by a wet oxidation at 800 °C. A layer of 1 µm of evaporated aluminium was deposited on top. Three wafers of every base resistivity were divided into four quarters and on both sides laser-fired contacts were applied with three different pitches (250, 500 and 1220 µm distance between contact points in a rectangular pattern), the fourth quarter was not contacted. After a forming gas anneal (25 min at 425 °C) the aluminium was etched away in hydrochloric acid (HCl) and the effective carrier lifetime was measured with the QssPC method at an excess carrier density of $\Delta n = 1\cdot10^{15}$ cm^{-3} to allow for comparison with previously acquired data on multicrystalline silicon.

The effective surface recombination velocity S_{eff} was derived with equation 6-9 under the assumption of a bulk lifetime which was only limited by Auger recombination, thus the calculated S-values represent the upper limit. Each data point in Fig. 6.5 represents the arithmetic average of three samples. No significant difference between the two oxidation processes was observed, demonstrating the possibility to substitute the dry oxidation process by the wet oxidation without loss of quality.

The obtained data was fitted by minimising the deviation between the measured values and the calculations with the equation

$$S_{eff} = S_0 \left(\frac{N_A}{N_{onset}} \right)^{\alpha} . \qquad \text{6-10}$$

S_0 shifts the calculated curve in vertical direction, N_A is the base doping, N_{onset} is the first evaluated doping concentration to normalise the fraction in brackets and α the exponent which determines the slope. Such parameterisation was also used by Cuevas et al. [111], Dicker [112] and Kray [113] who found similar values. The parameters for both, wet and dry oxide, are given in Table 6.2.

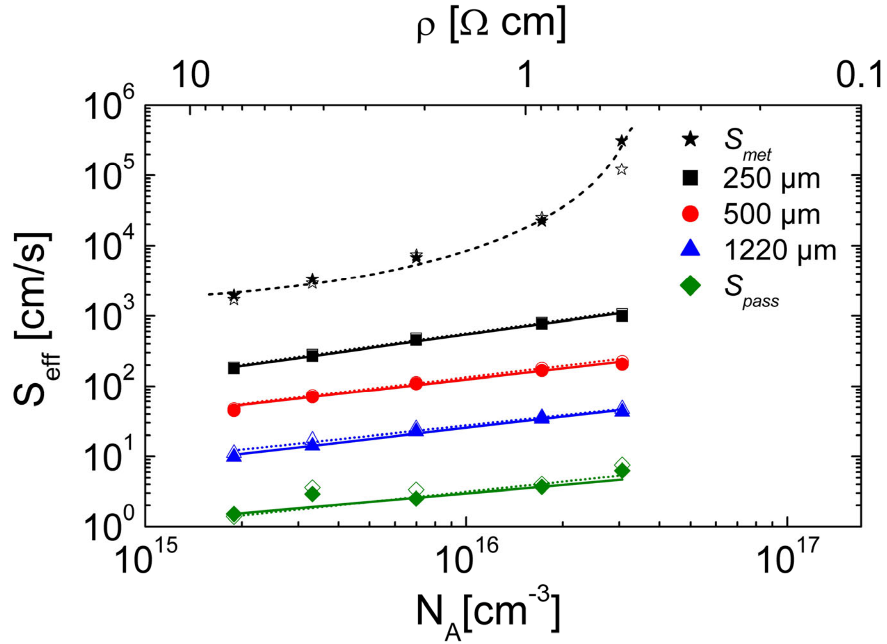

Fig. 6.5: Upper limit of effective rear surface recombination velocity of wafers passivated with 105 nm of thick oxide grown under dry (hollow symbols) and wet (solid symbols) conditions. Different contact spacings were applied. The lines are best fit according to equation 6-10 except for S_{met}, where the dashed line is a guide-to-the-eye only.

Table 6.2: Fit parameters according to equation 6-10 for S_{eff} as a function of base doping and LFC pitch. No significant difference between the dry oxide at 1050 °C and the wet oxide at 800 °C was observed.

oxide	pitch [µm]	S_0 [cm/s]	N_{onset} [cm^{-3}]	α
wet	∞	2	$1.9{\cdot}10^{15}$cm^{-3}	0.47
wet	1220	12	$1.9{\cdot}10^{15}$cm^{-3}	0.46
wet	500	56	$1.9{\cdot}10^{15}$cm^{-3}	0.47
wet	250	267	$1.9{\cdot}10^{15}$cm^{-3}	0.42
dry	∞	3	$1.9{\cdot}10^{15}$cm^{-3}	0.43
dry	1220	19	$1.9{\cdot}10^{15}$cm^{-3}	0.46
dry	500	73	$1.9{\cdot}10^{15}$cm^{-3}	0.53
dry	250	446	$1.9{\cdot}10^{15}$cm^{-3}	0.34

The high level of surface passivation of the oxidised silicon is shown by the very low surface recombination velocities. These were determined to be below $S_{pass} \leq 10$ cm/s for a base doping smaller than $N_A \leq 3{\cdot}10^{16}$ cm^{-3} and even decreased

further for lower base doping concentrations. The application of laser-fired contacts increased the effective rear surface recombination. However, the resulting S_{eff} is still very low. For example, a typical contact spacing of 500 µm for $\rho = 1.5\ \Omega$ cm multicrystalline silicon resulted in $S_{eff} \approx 120$ cm/s and for a very dense contact pattern of 250 µm for 5 Ω cm material $S_{eff} \approx 300$ cm/s was measured. In comparison to Fig. 6.4 the surface recombination values for the non-contacted reference is about a factor of ten smaller. This might be due to better process conditions which probably improved in terms of cleanliness with intensified use of the hydrogen burner.

Recently, Fischer published an analytical model to calculate the surface recombination velocity of solar cells with point-contacts on the rear [21]:

$$S_{eff} = \frac{D_e}{W}\left(\frac{L_P}{2W\sqrt{\pi f}}\arctan\left(\frac{2W}{L_P}\sqrt{\frac{\pi}{f}}\right) - \exp\left(-\frac{W}{L_P}\right) + \frac{D_e}{fWS_{met}}\right)^{-1} + \frac{S_{pass}}{1-f}. \qquad 6\text{-}11$$

D_e denotes the diffusion constant of minority carriers, W the wafer thickness, L_p the contact pitch, f the metallisation fraction, S_{met} and S_{pass} the surface recombination velocity at the metallised and passivated areas of the rear, respectively. Plagwitz et al. experimentally verified the model via the diode saturation current on carrier lifetime samples for amorphous silicon as passivation layer [114]. Kray and Glunz applied the model to silicon oxide passivated rear surfaces with photo-lithographically defined contacts and laser-fired contacts [115].

The model was used to extract the surface recombination velocity under the metal contacts S_{met}. This required the fraction of metallised area which can easily be calculated when the contact radius of the LFC point is known. Kray determined this contact radius to be 46 µm [113]. Also for S_{met} a clear dependence on the base doping concentration was observed (Fig. 6.5). This is explained by the aluminium alloy under the contact point which creates a back-surface-field and is more effective for lowly doped substrates [116].

The experimental data was fitted with the model in order to calculate the effective rear surface recombination velocity as a function of the contact pitch (see Fig. 6.6). For a given base resistivity S_{eff} increases by about one order of magnitude for a decreased distance between the laser-fired contacts from $L_p \approx 1200$ µm to 250 µm. This can have a significant effect on the solar cell parameters, therefore

this parameterisation is helpful for the optimisation of the laser-fired contacts for multicrystalline silicon solar cells as described in the following section.

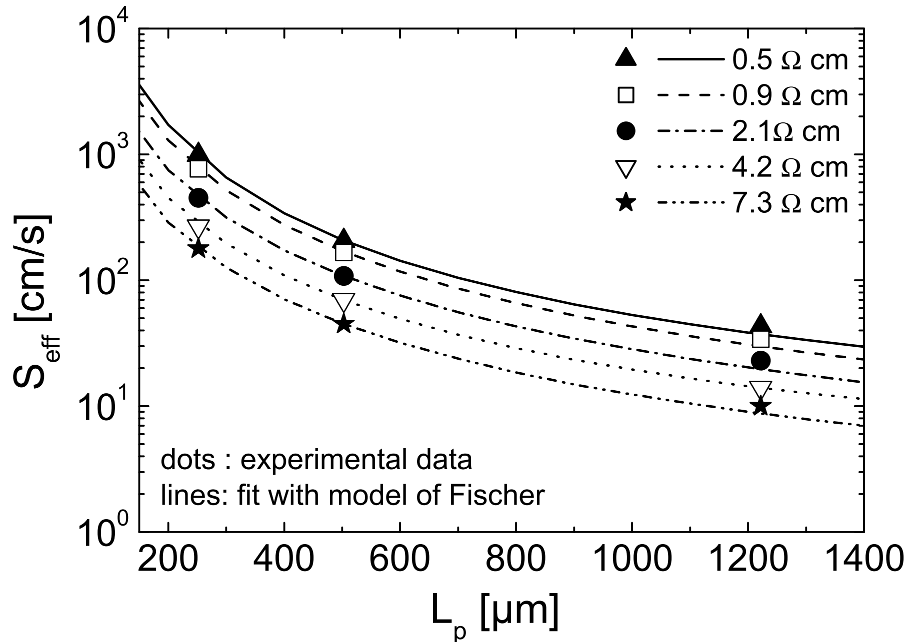

Fig. 6.6: Effective surface recombination velocity S_{eff} for a thick wet oxide of about 100 nm as a function of laser-fired contact distance L_p. The dots are experimental data points of Fig. 6.5. They were fitted with the model of Fischer (see equation 6-11).

6.2.4 Laser-fired contacts for multicrystalline silicon

In order to achieve a good fill factor, and thus a high efficiency of a solar cell, a low series resistance R_S is required. It is determined by the front contact metallisation, the contribution of the bulk resistivity and the rear contact resistance (see section 2.3.3). In the previous chapter it was shown that the effective surface recombination velocity at the rear $S_{eff,rear}$ increases with a higher density of contact points. This leads to higher recombination and the open circuit voltage V_{OC} of a solar cell is decreased. The same applies for the short-circuit current density j_{SC} where the additional effect of a decreased internal reflectance with increased laser-fired contact area reduces light-trapping [113]. However, when the distance between the contacts is decreased, the series resistance is also reduced because of the shorter path which the holes (as the majority carriers) have to diffuse to the contacts. Furthermore, less current flows through every single contact with contact resistance R_C which reduces power dissipation. For the calculation of the resistance

of the bulk and the rear contact the geometry of the contact spacing and cell thickness have to be taken into account. This leads to the term "spreading resistance" which considers the flow of current between the two contacts on front and rear. Simulations for optimum contacting spacing were performed by Catchpole and Blakers for the PERC cell structure [117] and for a local back-surface-field under the contacts, the PERL structure, by Zhao et al. [118]. The higher the base resistivity the more contacts are needed to obtain a low series resistance and thus high fill factors. Using such simulations or the analytical equation of Fischer [21], the optimum contact pitch could be calculated according to wafer thickness and base resistivity.

Experimentally the optimum LFC contact spacing for a wafer of $\rho \approx$ 1-2 Ω cm is in the range of 750-1000 µm for a square pattern and high fill factors in excess of 80 % are achieved for monocrystalline silicon solar cells. In order to check whether this can be transferred to multicrystalline silicon, 100 contact points were fired on the rear of a 1 cm^2 multicrystalline silicon solar cell of 1.5 Ω cm base resistivity, where the rear was covered with a wet oxide and 1 µm of evaporated aluminium. This corresponded to a 1000 µm pitch and a poor fill factor of only 72 % was achieved (see Fig. 6.7).

The series resistance was determined from comparison of the *I-V* curves in the dark and under illumination [119] as $R_S \approx 2.2\ \Omega\ cm^2$. On the same solar cell 100 contacts more were fired and the fill factor increased considerably to 77 % with the series resistance dropping to $R_S \approx 0.6\ \Omega\ cm^2$. This procedure was continued until a fill factor higher than 79 % was reached for a pitch of 378 µm and series resistance became negligible[10]. The corresponding cell with the same crystal structure from a neighbouring wafer with a full area evaporated metal contact resulted in 80 % fill factor indicating the upper limit with respect to rear contact design. Since the values for V_{OC} and j_{SC} decreased with increasing amount of contacts an optimum for the efficiency of the cell was obtained for about 600 µm contact pitch (Fig. 6.8).

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[10] For such low values the fill factor is limited by other parameters like j_{02} or R_P.

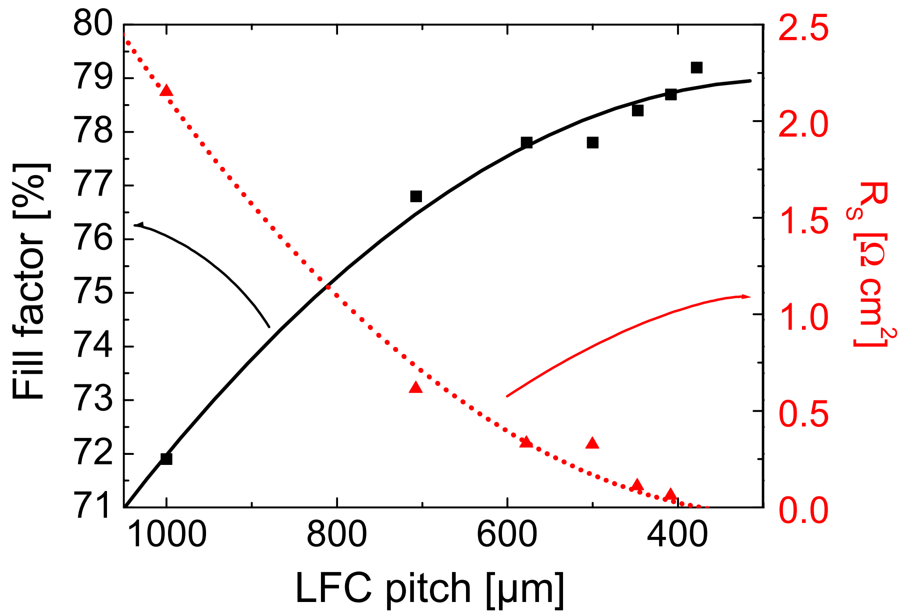

Fig. 6.7: Measured fill factor of a multicrystalline silicon solar cell versus LFC pitch (left–hand scale, squares). The contacts were subsequently fired on the rear of the same cell. The series resistance (right-hand scale, triangles) was derived from comparison of illuminated and dark *I-V* curves. The lines are guides-to-the-eye.

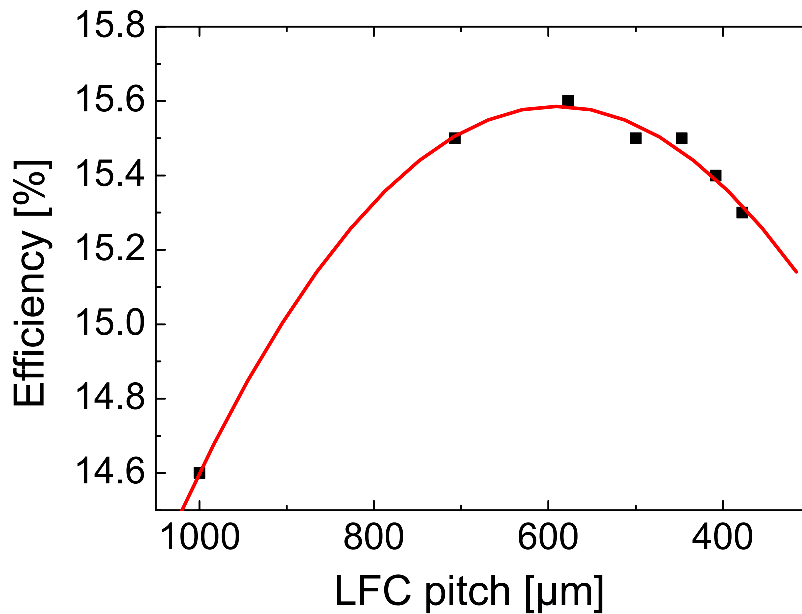

Fig. 6.8: Measured efficiency of a multicrystalline silicon solar cell of 1.5 Ω cm base resistivity versus LFC pitch. The contacts were subsequently fired on the rear of the same cell. The line is a guide-to-the-eye. The plasma-textured front did not have an antireflection coating thus the efficiency is only on a moderate level.

Multicrystalline silicon requires more contacts than corresponding monocrystalline wafers to achieve high fill factors. The reason might be found in the crystal structure because multicrystalline silicon has a high number of dislocations and grain boundaries. The mobility of carriers can be greatly reduced by scattering at dislocations [120,121] which can lead to a ten times higher specific resistivity across grain boundaries at room temperature [122]. This can greatly increase the series resistance in the bulk especially if some grains are not contacted due to a wide contact spacing. Then the current has to pass a grain boundary to reach the rear contact (see Fig. 6.9).

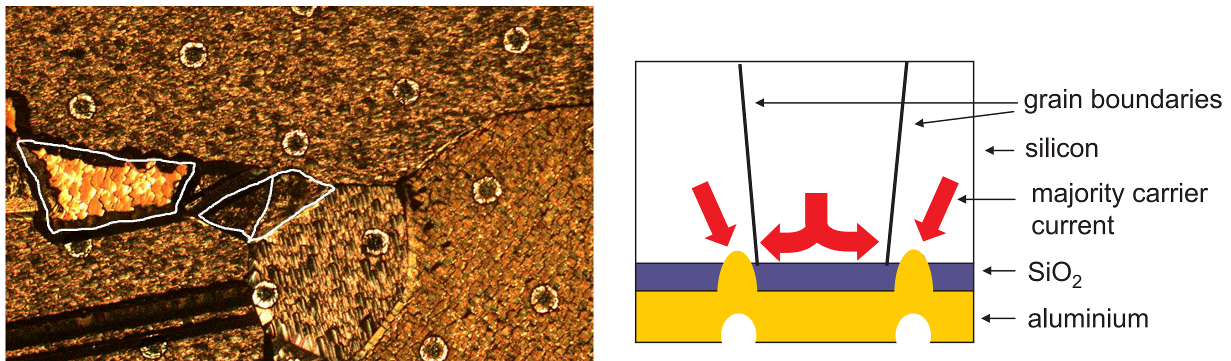

Fig. 6.9: Picture of the rear of laser-fired contacts on a multicrystalline silicon solar cell (left-hand). Although the distance between two laser-fired contacts is only is 500 µm there are still some small grains not directly contacted (marked by white lines). In these grains the majority carriers have to pass a grain boundary to reach the rear metal layer (right-hand).

6.3 Cell structure, process sequence and results

6.3.1 Cell structure and mask design

In the previous chapters and sections the processes to manufacture a high-efficiency multicrystalline silicon solar cell were characterised. These were in detail:

- Gettering to increase the material quality (chapter 3)
- Texturing (chapter 4)
- Emitter diffusion adjusted to textured surface (chapter 5)
- Highly reflective rear surface passivation without degradation of the bulk (chapter 3.2.4 and section 6.2.2)

- Laser-fired contacts for the rear (section 6.2.4).

The resulting cell structure for multicrystalline silicon developed in this thesis is shown in Fig. 6.10. In comparison to the cell design developed for high-efficiency monocrystalline silicon solar cells (see section 2.4) the oxidations necessary to build the cell structure were reduced to the minimum. The masking oxides for the local boron diffusion on the rear and the local emitter diffusion under the contacts on the front were omitted and the masking oxide for the front surface texturing process was replaced by a mask made of photoresist.

A photoresist-guided electroplating of the front contacts was not applied since the increased process complexity would require more wafer handling. This increases the risk of breaking the thin multicrystalline wafers.

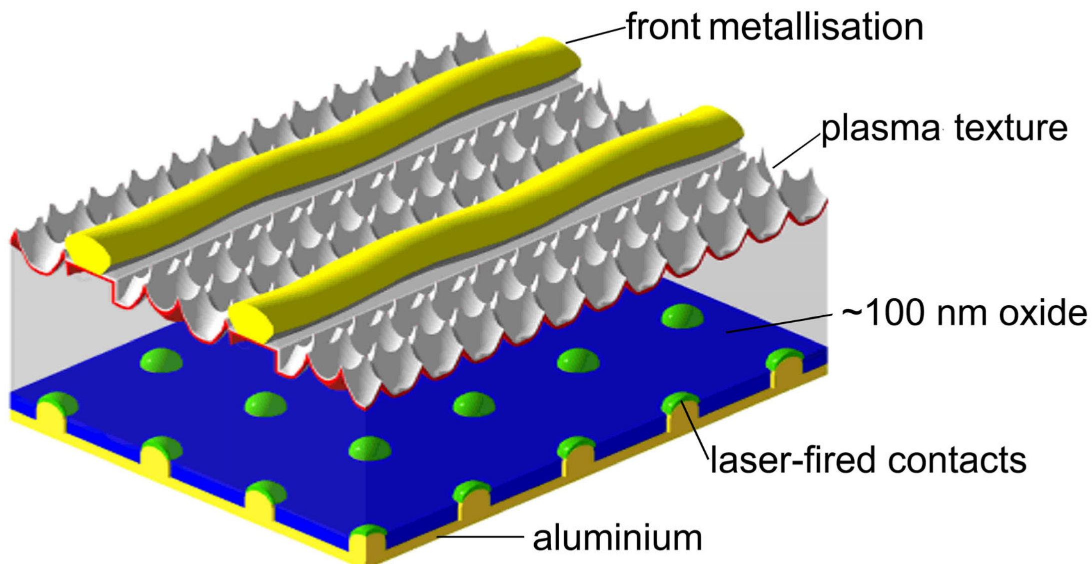

Fig. 6.10: High-efficiency cell structure for multicrystalline silicon. For the sake of clarity the double layer antireflection-coating on the front is not shown.

The main features of the developed cell structure are (from front to rear):

- Evaporated contacts. The front metal contact is built from an evaporated stack system of titanium, palladium and silver (Ti/Pd/Ag). This thin layer has a low contact resistivity and for a high grid conductivity the metallisation lines are thickened by electroplating of silver.
- Double layer antireflection coating. The use of a double layer coating of TiO_x/MgF_2 significantly reduces the primary reflection losses in comparison to

a single layer by adjusting layer thickness and refractive indices to the whole solar spectrum.

- Thin silicon oxide for surface passivation. A thin silicon oxide of about 15 nm thickness is thermally grown on top of the emitter. There was no aluminium anneal performed due to the increased process complexity and concerns about the long-term stability when exposed to UV-light [110].
- Plasma-textured front surface. The surface consists of deep cones which were etched using a lithographically defined mask of photoresist. The structured surface increases the possibility for incident light to be coupled into the cell. Furthermore the tilted surface leads to a refracted ray path and increases the distance of light coupled into the cell to reach the rear surface. This improves the absorption probability.
- Thin base of multicrystalline silicon. Although a thick wafer increases the absorption probability for long wavelength photons, multicrystalline silicon can benefit from a reduced cell thickness. The ratio of diffusion length/cell thickness is increased and the distance which generated carriers need to diffuse to the *p/n*-junction is decreased.
- Silicon oxide passivated rear surface. The rear surface is excellently passivated with an Al-nealed oxide of about 100 nm thickness. This reduces the rear surface recombination velocity and increases the minority carrier diffusion length. The excellent optical and electrical properties compensate the loss in carrier generation caused by the reduced cell thickness.
- Aluminium evaporated onto the silicon oxide. An aluminium layer of 1-2 µm thickness evaporated on silicon oxide works as a nearly perfect mirror. Long wavelength photons reaching the rear surface are reflected and pass through the whole wafer a second time. Together with the textured front this acts as a very good light-trapping scheme and enables several internal reflections.
- High dopant concentration under the rear contacts. A local silicon/aluminium alloy (p^+) underneath the rear contacts minimises the contact resistance and decreases recombination at the contacts. This is done by the laser-fired contact process and leaves the passivating oxide around the contacts unaffected [101].

A large number of solar cells which are electrically separated from each other are desirable since with such cells the material quality can be studied in detail on small areas (see chapter 7). Furthermore many process parameters can be tested on one wafer of 100 cm^2 size. This was done for the front metallisation by varying the

number of grid fingers (11 and 13) and the contact width (3 and 5 µm) for 36 solar cells of 1 cm^2 area. Six cells of 4 cm^2 with 25 grid fingers and 5 µm contact opening were defined. All cells were electrically isolated from each other by masking the emitter diffusion around the cells on the front. To enable the exact determination of the cell parameters, the cells were confined by a photo-lithographically defined evaporated aluminium mask between the cells. Every cell was measured individually with all neighbouring cells being shaded during the measurement. A picture of a completely processed wafer is shown in Fig. 6.11. Due to the effective front surface texturing, the multicrystalline structure is hardly visible on the cells but clearly detectable on the aluminium area mask.

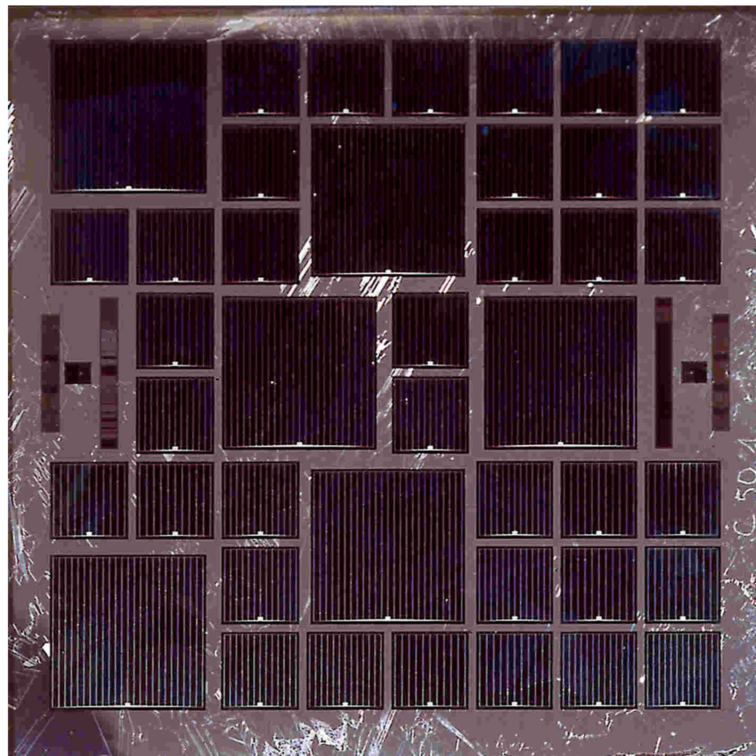

Fig. 6.11: Picture of 42 small solar cells on one wafer of 10·10 cm^2. Every small solar cell can be measured independently and the area is defined by an evaporated shadow mask. The metallisation including the busbar is completely inside the defined aperture area. The structures in the middle of the picture (left and right edge) are metallisation test structures and symbols used for alignment of the lithographic masks.

6.3.2 Process sequence

In section 2.5 it was shown that the standard processing sequence for high-efficiency monocrystalline silicon solar cells was not directly applicable to multicrystalline silicon. The main reasons were the texturing, which didn't work on the different crystal orientations, and the many high-temperature oxidations at 1050 °C, which severely degraded the bulk lifetime. The process sequence which was developed for multicrystalline silicon solar cells in this thesis is shown in Fig. 6.12. The first process after removal of the surface damage from sawing/grinding is the gettering of unwanted impurities in the bulk. The easiest, most reliable and successful method turned out to be a phosphorus diffusion from both wafer surfaces (see section 3.2). Impurities agglomerate in a layer close to the surface and are permanently removed by etching away several micrometers of silicon.

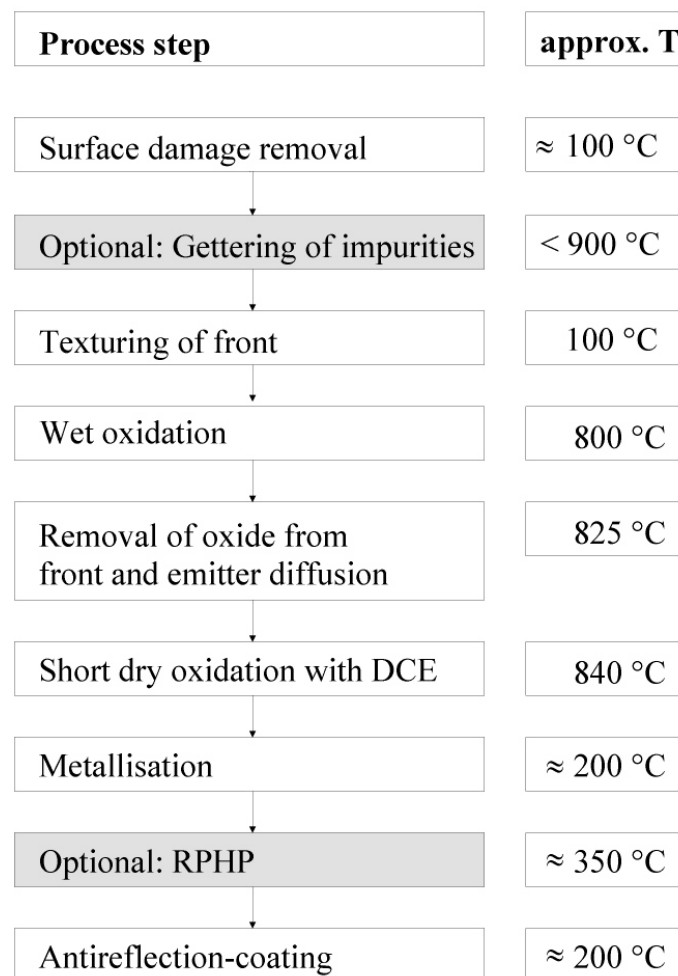

Fig. 6.12: Process sequence for high-efficiency multicrystalline silicon solar cells and approximate process temperatures. The gettering in the beginning and the hydrogen passivation at the end (RPHP) are optional and not necessary for very clean material.

When the material is clean enough this gettering might be not necessary. The wafer is textured on the front surface with a low-temperature plasma etching process. This is followed by a wet oxidation at 800 °C which does not degrade the bulk lifetime. The oxide on the cell's front surface is wet-chemically etched away and on the rear the oxide masks the emitter diffusion. After wet-chemical removal of the phosphorus silicate glass (PSG), where about 100 nm of oxide are left on the rear, a thin oxide of about 15 nm on the front is grown under dry conditions (dichloroethylene is added to the oxidation ambience). This thin layer passivates the front. It is partially etched away (area defined by photolithography) for the evaporation of the metal contacts by a stack of Ti/Pd/Ag, which later on are thickened by electroplating. A layer of 2 µm of evaporated aluminium is deposited on the rear and the contacts are laser-fired. The cell is then annealed in forming gas for about half an hour at temperatures around 400 °C. Optionally, a hydrogen passivation can be applied to further improve the bulk lifetime before the last step, in which a double layer antireflection coating of TiO_x/MgF_2 is evaporated.

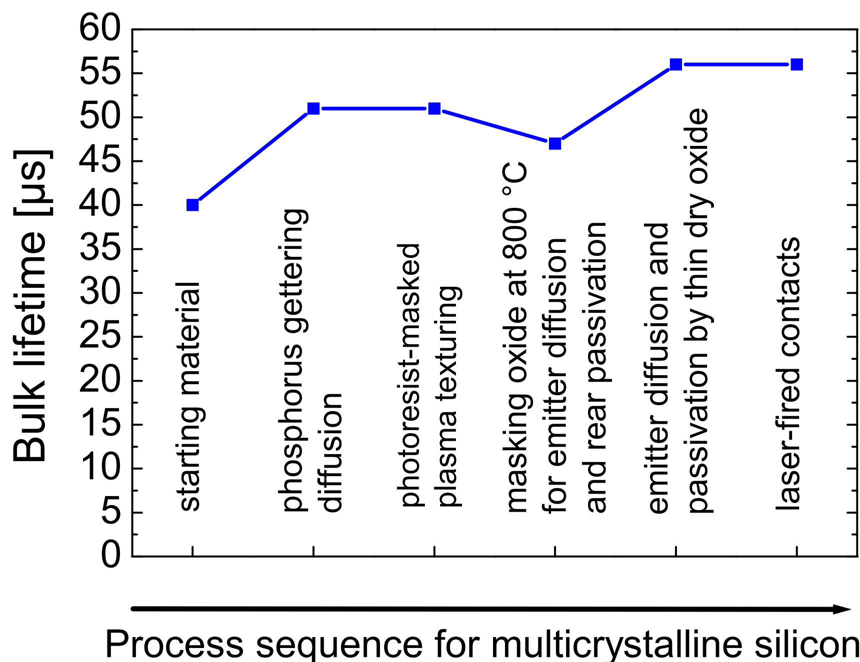

Fig. 6.13: Bulk lifetime of multicrystalline silicon wafers passivated with silicon nitride. The oxidation at 800 °C only led to a small degradation and was recovered by the emitter diffusion. The bulk lifetime after the whole process chain was even higher than the lifetime of the starting material.

The processes were optimised to maintain a high bulk lifetime during manufacturing of a high-efficiency cell structure. This was verified by measurements of the minority carrier lifetime of samples, taken out of the batch of wafers after the different processes. Some micrometers of the surfaces were wet chemically etched away and cleaned in order to provide identical conditions for every sample. Well passivating silicon nitride was deposited on the surfaces and the effective carrier lifetime, which is nearly identical with the bulk lifetime, was measured with the QssPC method at an excess carrier density of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}. The results are shown in Fig. 6.13.

6.3.3 Cell results on different types of multicrystalline silicon

Usually multicrystalline silicon wafers have base resistivities between 0.5-2 Ω cm and are in most cases boron-doped. But also gallium can be used to grow *p*-type silicon. This has the advantage that the boron-oxygen defect, typically observed in wafers grown with the Czochralski method [123,124], cannot reduce the cell efficiency due to the absence of boron. However, during this work degradation was not observed for the cells on boron-doped silicon either, which is explained by the lower oxygen concentration in multicrystalline silicon, the other partner of the boron-oxygen complex.

Gallium has a low segregation coefficient in silicon, thus the base resistivity strongly varies between bottom and top of the ingot. The material used in this thesis manufactured by Dai-ichi Kiden varied between $\rho \approx 2$ Ω cm (bottom) to $\rho \approx 8$ Ω cm (top) [125]. This is no problem for the developed cell structure because the rear surface passivation improves with increasing base resistivity (see Fig. 6.5) and the p^+-alloy under the LFC contacts results in low contact resistance even for a high base resistivity.

Lower base doping in general can have a beneficial effect on the recombination lifetime as was calculated by Geerligs and Macdonald [126]. In the presence of defects with asymmetric capture cross sections $\sigma_n > \sigma_p$ the minority carrier lifetime in *p*-type silicon is enhanced with increasing base resistivity. As an example the recombination lifetime of iron in boron doped silicon was calculated in dependence of the base resistivity. According to the calculation for a comparatively low base

resistivity ($\rho \leq 3\ \Omega$ cm) an iron concentration of $[Fe_i] = 3 \cdot 10^{11}$ cm^{-3} limits the minority carrier lifetime to 10 µs (see Fig. 6.14).

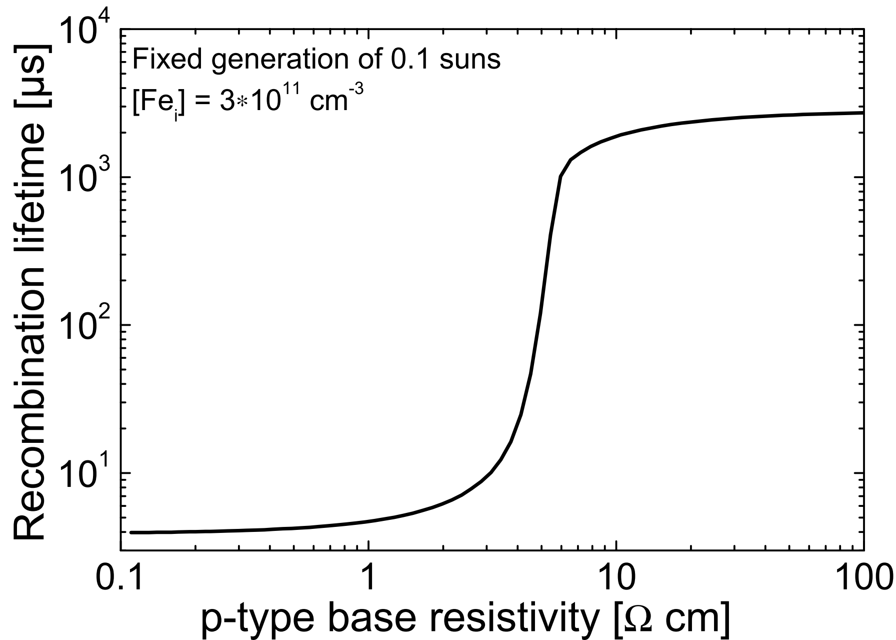

Fig. 6.14: Dependence of recombination lifetime from base resistivity for iron in boron-doped silicon. The calculations were performed with the parameters published by Geerligs and Macdonald [126]. For resistivities above 5 Ω cm a minority carrier lifetime in excess of 100 µs can be reached even with an iron concentration of $[Fe_i] = 3 \cdot 10^{11}$ cm^{-3}.

For a resistivity in excess of 5 Ω cm 100 µs and more can be reached, i.e. although the material is contaminated with iron, the carrier lifetime is not limited anymore by this specific defect to values which would affect solar cell efficiency. In other words: High-resistivity material is more tolerant to contamination. The increase in lifetime also applies for the boron-oxygen complex, well known for Czochralski-pulled material, because of the smaller amount of boron with decreasing base doping. This defect can also be present in oxygen-rich multicrystalline [127].

The developed cell structure was applied to mono- and multicrystalline silicon of different suppliers. The best cell results for 1 and 4 cm^2 aperture area for monocrystalline FZ silicon are shown in Table 6.3. High efficiencies around 20 % were achieved under standard testing conditions (25 °C, 1000 W/m^2, AM1.5g) for a wide range of base resistivity $\rho = 0.5\text{-}9\ \Omega$ cm.

Table 6.3: Table of best cell results of 1 cm^2 and 4 cm^2 aperture area for monocrystalline FZ silicon of various base resistivity. Efficiencies in excess of 20 % were achieved for a range from $\rho = 0.5$-9 Ω cm. The average values were calculated from the cells on the same wafer that did not have obvious metallisation problems and therefore fill factors of $FF \geq 70$ %. The 4 and 9 Ω cm material was only available as 4 inch round wafers, thus only 34 cells could be processed with the masks designed for 4 inch square wafers.

producer and cell-ID	area [cm^2]	ρ [Ω cm]	W [µm]	V_{OC} [mV]	j_{SC} [mA/cm^2]	FF [%]	η [%]
Wacker Siltronic							
mc8_FZ_05_1_A6	1	≈ 0.5	≈ 250	644	39.6	80.6	20.6
mc8_FZ_05_1_E5	4	≈ 0.5	≈ 250	641	39.7	80.0	20.4
Average of 40 cells				639±5	39±0.4	79.1±2.3	19.7±0.7
mc6_FZ_1_B1	1	≈ 1	≈ 220	660	39.8	80.7	21.2
mc6_FZ_1_E3	4	≈ 1	≈ 220	660	39.7	80.2	21.0
Average of 34 cells				641±8	39.4±0.3	79.7±2.9	20.1±0.8
mc13_FZ_4_2_D7	1	≈ 4	≈ 250	639	40.0	79.6	20.3
mc13_FZ_4_2_E2	4	≈ 4	≈ 250	635	39.7	78.5	19.8
Average of 33 cells				634±2	39.9±0.2	78.1±0.8	19.7±0.3
mc13_FZ_9_2_C4	1	≈ 9	≈ 250	645	40.4	78.2	20.4
mc13_FZ_9_2_E2	4	≈ 9	≈ 250	642	39.8	77.2	19.7
Average of 34 cells				636±4	40.1±0.3	76.9±1.2	19.6±0.4

The same was process was also applied to a variety of multicrystalline silicon materials from different suppliers, the results are shown in Table 6.4. Part of the wafers were mechanically ground before the process. This beard the benefit of an increased ratio of minority carrier diffusion length/cell thickness without improving the material quality, but for thin wafers of about 100 µm mechanical stability became a major problem. The wafers mainly broke during handling with

Table 6.4: Table of best cell results of 1 cm^2 and 4 cm^2 aperture area for multicrystalline silicon of various base resistivity. Efficiencies of about $\eta \approx 20$ % were achieved for a wide range from $\rho = 0.5$-5 Ω cm. The average values were calculated from cells on the same wafer that did not have obvious metallisation problems and fill factors of $FF \geq 70$ %.

* = independent calibrated measurement at Fraunhofer ISE CalLab

+ = independent calibrated measurement at NREL

producer and cell-ID	area [cm^2]	ρ [Ω cm]	W [µm]	V_{OC} [mV]	j_{SC} [mA/cm^2]	FF [%]	η [%]
ScanWafer boron-doped							
mc8_S10_94_C6	1	≈ 1.5	≈ 170	640	38.8	80.8	20.1
mc8_S10_94_E5	4	≈ 1.5	≈ 170	638	38.8	80.0	19.8*
Average of 33cells				625±12	37.8±0.8	76.1±3.4	18.0±1.2
Eurosolare boron-doped							
mc8_C_50_1_A7	1	≈ 0.5	≈ 250	641	37.0	81.5	19.3
mc8_C_50_1_E6	4	≈ 0.5	≈ 250	637	37.5	80.1	19.1
Average of 39 cells				626±10	35.9±0.9	78.4±2.3	17.6±1.0
Kawasaki Steel boron-doped							
mc6_K1_D1	1	≈ 0.6	≈ 218	653	38.8	78.6	19.9*
mc6_K3_D1	1	≈ 0.6	≈ 99	664	37.7	80.9	20.3+
mc8_K5_E5	4	≈ 0.6	≈ 150	639	37.5	80.4	19.3
Average of 148 cells				635±12	36.8±0.8	77.7±2.9	18.1±1.0
Dai-ichi Kiden boron-doped							
mc13_BC5_F_C1	1	≈ 1.2	≈ 270	640	38.8	80.0	19.9
mc13_BC5_F_E6	4	≈ 1.2	≈ 270	630	37.8	78.7	18.7
Average of 32 cells				618±16	37.6±0.9	77.8±1.8	18.1±1.2
Dai-ichi Kiden gallium-doped							
mc13_GaC5_F_A7	1	≈ 5	≈ 270	623	39.3	79.5	19.5
mc13_GaC5_F_E1	4	≈ 5	≈ 270	622	39.0	78.1	19.0
Average of 27 cells				608±11	38.7±0.5	76.2±2.1	18.0±0.9

tweezers and not during processing, a phenomenon also known for thin monocrystalline silicon wafers [128]. For this reason and due to some plating problems (not all front contacts of the cells were plated on the wafer) not all 42 cells, which were processed on a wafer, could be taken into account for an averaging of the efficiencies. Only the solar cells with fillfactor $FF \geq 70\%$ were considered, this left about 30 cells on every wafer which could reliably be processed.Very high efficiencies in excess of 20 % efficiency were measured on small multicrystalline silicon solar cells. Although the cells had relatively small aperture areas, even for the 1 cm^2 solar cell with efficiencies of about 20 %, the material was still multicrystalline as is shown in Fig. 6.15.

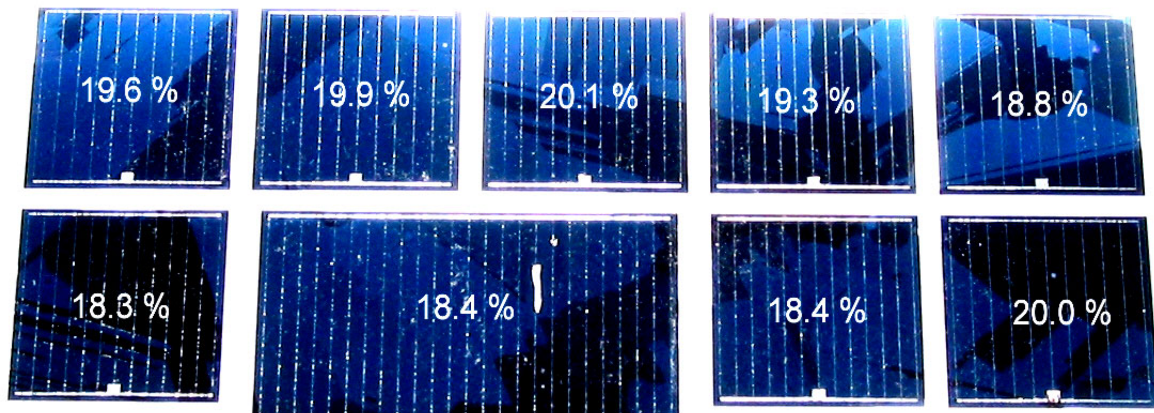

Fig. 6.15: Photography of eight adjacent solar cells of 1 cm^2 and one half cell of 4 cm^2 size on one wafer (mc6_K3). In comparison to Fig. 6.11 a very intense light was used during the photography. Thus the grain structure between the cells underneath the aluminium aperture area is not visible anymore (white) but this technique enabled to see that all cells consist of several grains.

The independently confirmed efficiency of 20.3 % is the highest efficiency reported for multicrystalline silicon to date [19]. The 19.8 % efficiency on a 4 cm^2 cell and the high average values of about 18 % as they were achieved on a large variety of material show the potential of solar cell efficiencies which may be reached on entire large area wafers. The histogram for 148 cells processed on five wafers from the same brick produced by Kawasaki Steel is given in Fig. 6.16.

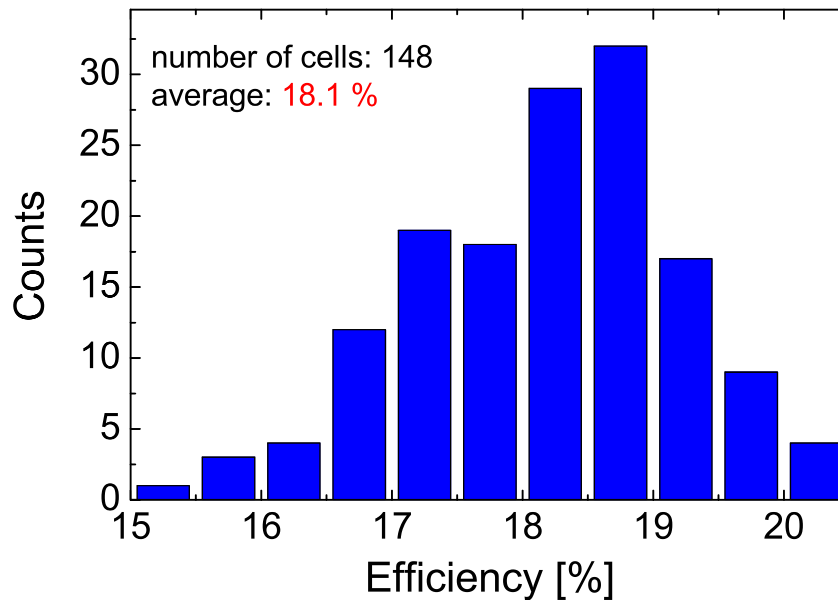

Fig. 6.16: Histogram of solar cell efficiencies of five wafers from the same brick produced by Kawasaki Steel. The average values were calculated from cells that were neither broken nor had obvious metallisation problems and thus fillfactors of $FF \geq 70$ %. An average efficiency of 18.1 % was achieved for 148 solar cells of 1cm^2 and 4 cm^2 size and shows the potential of solar cell efficiencies which may be reached on entire large area wafers.

The major reason for the efficiency distribution is the inhomogeneity of the material with respect to minority carrier lifetime which determines the values for V_{OC} and j_{SC}. A typical distribution is shown in Fig. 6.17 where also the contour of solar cells are drawn into the image. Solar cells which were processed in regions of high lifetime show very high efficiencies, a mix of high and low lifetimes leads to medium efficiencies and solar cells in areas of bad material quality show low efficiencies.

The important feature of the developed cell process is the direct dependence of the solar cell parameters on the minority carrier lifetime. This enabled the detailed modelling of multicrystalline solar cells as it is described in chapter 7.

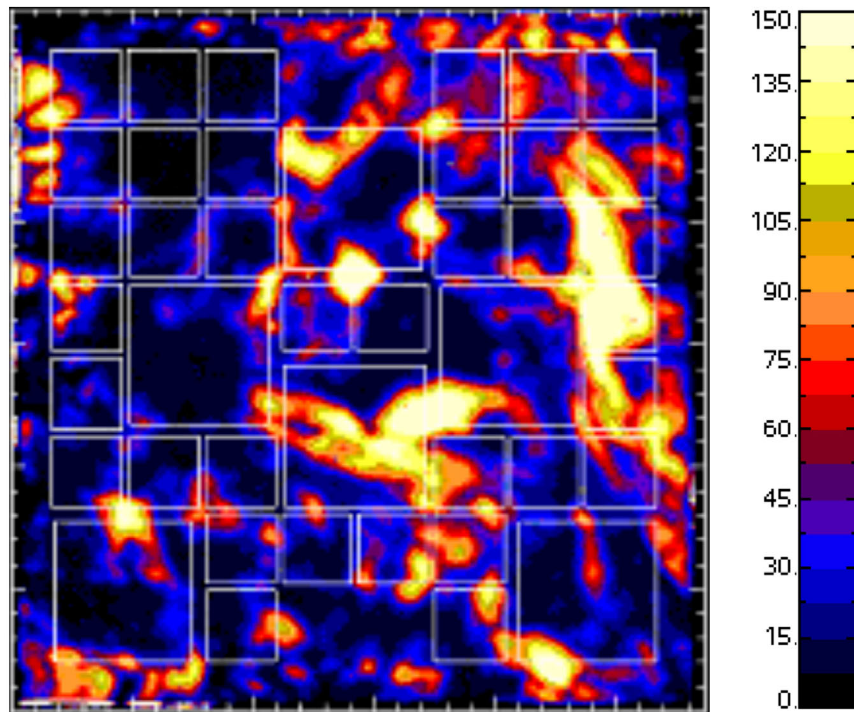

Fig. 6.17: A typical distribution effective minority carrier lifetime for a multicrystalline silicon wafer used for high-efficiency solar cells. The image is blurred because of the emitter on the front which enables a carrier flow between regions of different lifetime. The major reason for the broad distribution of solar cell efficiency is the material inhomogeneity. The contours of the 42 solar cell processed on every wafer are drawn as white lines.

6.4 Chapter summary

The oxidation rate of the silicon surface was significantly enhanced by the addition of water steam to the gas atmosphere during oxidation. Therefore the process temperature could be lowered from the standard 1050 °C to 800 °C. This reduction prevented the degradation of multicrystalline silicon, nevertheless the passivation quality was kept on the same high level. The rear surface recombination velocity was experimentally determined for a broad range of base resistivity as a function of the laser-fired contact spacing. Compared to monocrystalline silicon this distance between the contacts on the rear needed to be decreased for multicrystalline silicon in order to achieve high fill factors. This was explained by a hampered current transport across the grain boundaries which would require every single crystal to have at least one contact point. However, despite the loss in rear surface passivation due to an increased fraction of contacted area, the effective rear surface recombination velocity was still low enough to be

applied to high-efficiency solar cells ($S_{eff} \approx 120$ cm/s for 1.5 Ω cm material and 500 µm contact pitch, $S_{eff} \approx 300$ cm/s for 5 Ω cm material and 250 µm contact pitch).

This rear surface structure was combined with the processes for gettering, surface texturing and emitter diffusion whose development was described in the previous chapters. Degradation of the material was successfully avoided by the choice of low temperatures and an adequate process sequence: During processing the minority carrier lifetime of the multicrystalline silicon increased instead of decreased.

Although the developed cell structure was comparatively simple (no selective emitter, no aluminium anneal on the front, single-step electroplating of evaporated contacts, laser-fired contacts instead of local boron diffusion), very high efficiencies could be obtained for a broad range of block cast materials and base resistivity ($\rho \approx 0.5$-5 Ω cm). Excellent results of about $\eta \approx 20$ % for small area solar cells of 1 and 4 cm^2 and high average efficiencies of $\eta \approx 18$ % for an entire wafer were obtained. The independently confirmed efficiency of $\eta \approx 20.3$ % for a 1 cm^2 cell under standard testing conditions was the first multicrystalline silicon solar cell in excess of $\eta \geq 20$ %. This result was obtained on a wafer of less than 100 µm thickness demonstrating the high quality of the cell structure in terms of surface passivation and light-trapping.

Nevertheless, the material quality still has a strong influence on the solar cell parameters. This dependence makes the cell structure an ideal tool for the characterisation of multicrystalline silicon material and is therefore applied in the next chapter.

7 Influence of inhomogeneous carrier lifetime on solar cell parameters

7.1 Introduction

This chapter deals with the measurement and effects of inhomogeneous carrier lifetime as they are usual in multicrystalline silicon. The first section shows that preparation of lifetime test structures is critical and that the standard preparation to assess the material quality, i.e. deposition of silicon nitride to suppress surface recombination, does not create appropriate measurement conditions for the prediction of solar cell parameters. Instead a measurement of the effective carrier lifetime after all high-temperature processes is favourable. With the emitter being present on the surface of such samples, a proper evaluation has to deal with this additional conductivity increasing the current flow from regions of high to regions of low lifetime.

A method to consider this effect in the evaluation of spatially resolved CDI measurements is developed and the derived minority carrier lifetime converted into dark saturation currents of elementary solar cells. In a simplified analytical model, where no sophisticated network simulations are necessary, the measurements are used to predict the solar cell parameters and a very good match between the simulated and measured results is obtained.

7.2 Sample preparation for lifetime measurements

Standard techniques measure the effective lifetime which comprises the bulk recombination lifetime and surface recombination. The latter can effectively be suppressed by suitable surface passivation methods so that the bulk lifetime can be extracted. Standard procedures of surface passivation are iodine/ethanol solutions, thermal oxidation, deposition of a silicon nitride layer or a shallow emitter diffusion plus an additional thin thermal oxide. With the exception of the iodine/ethanol solution (which is not long-term stable) those methods bear the risk of effectively changing the parameter under investigation, the bulk lifetime. This

may be caused by degradation of the multicrystalline silicon material due to the high temperatures which are involved with oxidations. Also an improvement of the material quality caused by gettering of impurities during phosphorus diffusion is possible. Silicon nitride layers deposited at low temperature lead to an excellent surface passivation (S ≈ 10 cm/s) and are long-term stable. Thus they would be the preferred method, but whether the bulk of multicrystalline silicon is improved by hydrogenation (hydrogen is incorporated in the precursor gas silane (SiH_4)) is still an open question.

To investigate this issue, an experiment was set up with neighbouring wafers of the same ingot. Fig. 7.1 shows the average effective lifetimes measured with the QssPC method on nine measurement spots on every 125·125 mm^2 neighbouring wafer after different treatments.

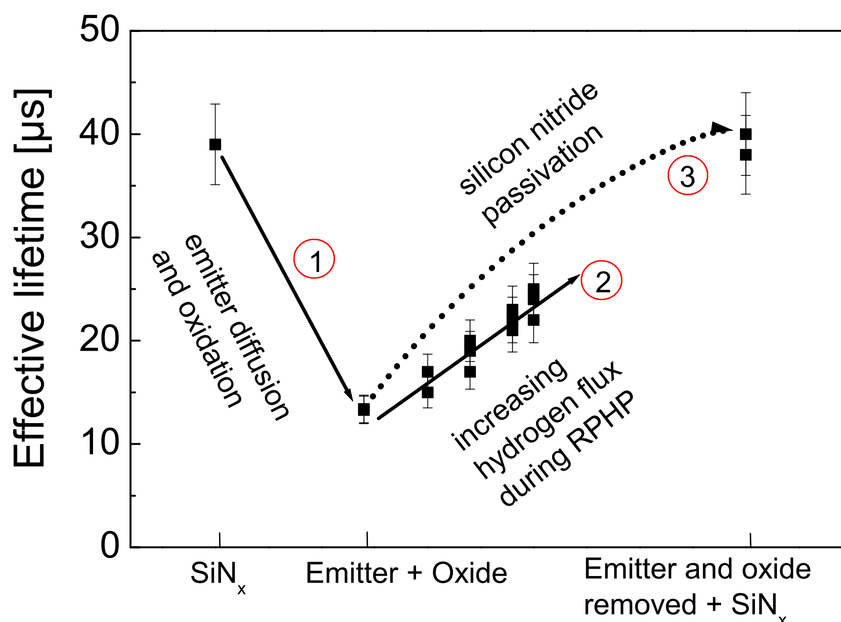

Fig. 7.1: Effective minority carrier lifetime measured with QssPC technique at an injection level of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}. The 40 µs of the reference sample without heat treatment and direct silicon nitride passivation drop to 14 µs after emitter diffusion and oxidation. It can at least partially be recovered by increasing hydrogen passivation. A passivation with silicon nitride is able to recover the lifetime to the initial value.

The reference wafer without high-temperature or intentional hydrogenation treatment was passivated with the silicon nitride layer in 9 min at 350 °C and had a lifetime of about 40 µs. A neighbouring wafer received an emitter diffusion at 820 °C which was driven-in with a wet oxidation at 800 °C. After etching away the

oxide in HF, a dry oxidation for 20 min at 900 °C provided a thin oxide. With a following forming gas anneal for 25 min at 425 °C, this oxide passivated the surface well enough to measure about 250 µs on 1 Ω cm FZ silicon reference samples (at an injection level of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}) which can be converted to a maximum surface recombination velocity value of 40 cm/s. Due to this step the effective lifetime of the multicrystalline wafers dropped from 40 µs to 14 µs (1) and since surface passivation was excellent, this means that the bulk has either been damaged or that this is the initial value without a hydrogenation coming from the silicon nitride layer deposition itself.

Several neighbouring wafers of the same run were then intentionally hydrogenated in a remote plasma hydrogen passivation (RPHP) reactor installed at Fraunhofer ISE [129]. The effective lifetime improved with increasing hydrogen flux during the 45 min process at 350 °C up to a value of about 25 µs (2). This was not due to an improved surface passivation as on FZ-reference samples the effective lifetime was not changed. It was the hydrogenation of the bulk which took places in the multicrystalline wafers only. Wafers of which the emitter was etched away and which were passivated with silicon nitride reached an effective lifetime of about 40 µs (3). This was the same as the reference wafer. These results can be interpreted as follows:

- The emitter diffusion and oxidation degraded the bulk lifetime in comparison to the reference wafer (1). This degradation was healed at least partly by intentional hydrogenation in the plasma reactor.

Or:

- The lower effective lifetime of the emitter-diffused sample is due to the missing hydrogenation of the silicon nitride passivation.

Since the deposition of silicon nitride on the thermally treated samples can recover the value of the reference wafer, it is tempting to see this as a proof of the hydrogenation during layer deposition.

Since the QssPC technique only measures average values for areas of about 11 cm^2 CDI measurements of two wafers were taken for a better comparison between the two surface passivation methods. The measurements are presented in Fig. 7.2.

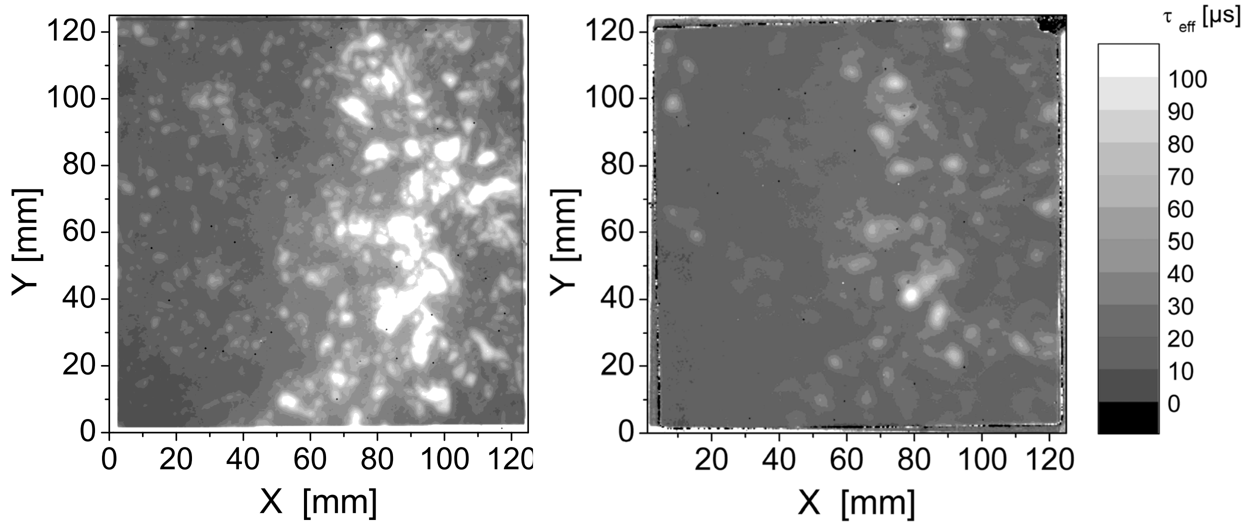

Fig. 7.2: CDI image of a silicon nitride passivated reference sample (left-hand) and of an emitter diffused and oxidised sample after hydrogen passivation (right-hand).

The silicon nitride passivated reference showed a rather fine grained structure where many details were observable. The CDI image of the sample with emitter and a thin oxide was more homogeneous and has fewer parts which are either very good or very bad. This was also observable in the histograms shown in Fig. 7.3.

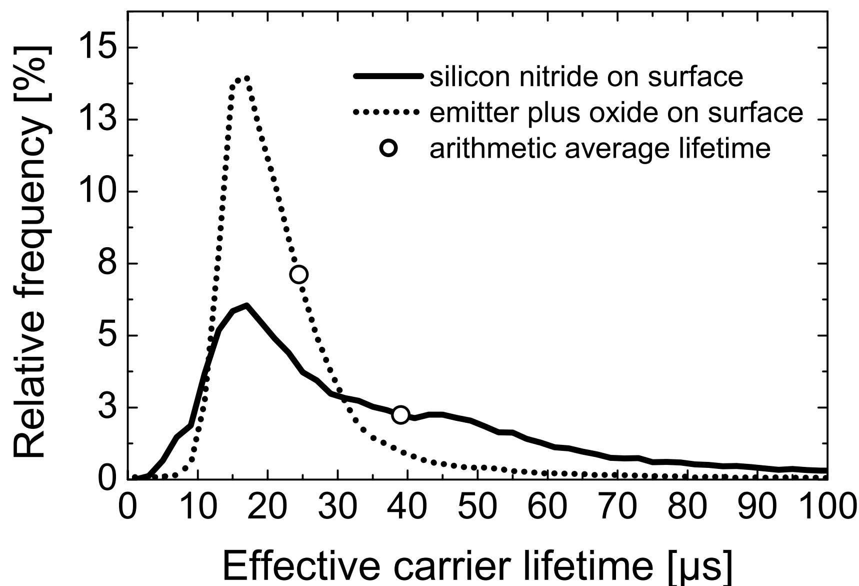

Fig. 7.3: Histogram of the reference wafer with silicon nitride surface passivation and a hydrogenated wafer with emitter and thin oxide. Arithmetically averaged lifetimes are 39 µs and 26 µs respectively.

The distribution of measured lifetimes was much broader for the silicon nitride passivated sample than for the emitter diffused and oxide passivated sample. This could be explained by the additional lateral conductance provided by the diffused emitter, which led to a carrier flow from regions of high lifetime to regions of low lifetime, a topic further investigated in section 7.3. The arithmetic averages of the histograms are also shown and provoke the question whether arithmetic averaging of the measured lifetimes in each pixel is the appropriate measure to characterise the distribution, a topic addressed in section 7.5. From the experiments described above, a clear hydrogen passivation of the bulk of multicrystalline silicon caused by the deposition of the silicon nitride layer could not be proven, but it could not be excluded either. Due to this uncertainty a degradation caused by the thermal oxidation is still possible but than it was at least partly healed by a hydrogenation of the bulk. Since in this chapter the effect of inhomogeneous material quality on the performance of solar cells is under investigation, it is advisable to prepare the samples in the same way as the corresponding completed solar cells. This includes all possible gettering effects, thermal degradation and surface passivation. The influence of the emitter on the lifetime measurements is discussed in the next section.

7.3 Influence of emitters on carrier lifetime measurements

In the previous chapter it was discussed that the probably best method to prepare the wafer for lifetime measurement for modelling is a sample which was exposed to all high-temperature processes and diffusions since such treatment can change the bulk lifetime. Furthermore, a possible hydrogenation of the bulk caused by deposition of a silicon nitride layer could not be ruled out. Therefore a sample with the emitter diffusion and passivation as it is applied in the corresponding solar cells seems to be the best choice. The drawback is that this conducting layer (the emitter) enhances the carrier transport between regions of different material quality. This was already described in the previous section where the histograms of wafers with the same crystal structure were blurred in the case of an emitter as surface passivation in contrast to a silicon nitride passivation. The basic idea to explain this observation is a carrier transport through the emitter during the

measurement between regions (grains) of high and low carrier lifetimes[11]. Using the equations derived in section 2.2. this is discussed in the following for the "standard" case of a *p*-type base. The electrons are the minority carriers in the base and majority carriers in the *n*-type emitter. For a n-type base the equations have to be changed accordingly.

The local excess carrier density Δn can be described by the quasi-Fermi-level ε_{FC} which is

$$\varepsilon_{FC} = \varepsilon_C + kT \ln\left(\frac{n_0 + \Delta n}{N_C}\right) \tag{7-1}$$

where kT is the thermal voltage, n_0 the equilibrium density of electrons in the dark and N_C the density of states of electrons. The current flow j_e of electrons (being the minority carrier in a p-type base) between regions of high and low lifetime is caused by a gradient in the quasi-Fermi-level and depends on the conductivity σ_e for electrons and the elementary charge q via the equation

$$j_e = \frac{\sigma_e}{q} grad\,(\varepsilon_{FC}) \tag{7-2}$$

This means that from the observation of different carrier lifetimes, it can be concluded that there are currents flowing between the different regions under (quasi-) steady-state measurement conditions. These currents are maintained by the light-induced generation of carriers and the recombination, which is different in different regions of the sample. Usually the measured excess carrier concentration is converted into a carrier lifetime via

$$\tau_{eff} = \frac{\Delta n}{G} \tag{7-3}$$

which is the conclusion of the continuity equation under steady-state conditions

$$0 = \frac{1}{q} div\, j_e - \frac{\Delta n}{\tau_{eff}} + G \tag{7-4}$$

under the assumption that no current flow is present, i.e. $div\, j_e = 0$. The discussion above shows that this assumption is not correct. At least for emitter-diffused samples the current flow from regions of high lifetime to regions of low lifetime is

[11] The method to calculate this current flow from CDI measurements and to predict the solar cell parameters was developed by Jan Christoph Goldschmidt in a diploma thesis supervised by the author.

not negligible. The standard evaluation results in to too small values in high lifetime regions and to too high values in low lifetime areas. Therefore equation 7-3 needs to be modified to

$$\tau_{eff} = \frac{\Delta n}{G + \frac{1}{q} div\, j_e} . \qquad \text{7-5}$$

For further calculations the sample is divided into two regions, the emitter and the base. Within these regions, homogeneous material properties in vertical direction are assumed. This is justified by the columnar growth of the block cast material and necessary, since the CDI yields the excess carrier density in two dimensions only. An integration over the sample width W results in the correct dimensions. With the knowledge of the mobility μ_e the conductivity for electrons in the base $\sigma_{e,base}$ is

$$\sigma_{e,base}(x,y) = q\, n(x,y)\, \mu_e . \qquad \text{7-6}$$

For the emitter, homogeneous properties can be assumed in x- and y-direction. The conductivity of the electrons $\sigma_{e,emitter}$, which now are the majority carriers, is given by the measured sheet resistance R_{sheet} and the thickness of the emitter $W_{emitter}$ by

$$\sigma_{e,emitter} = \frac{1}{R_{sheet} W_{emitter}} . \qquad \text{7-7}$$

Due to the low concentration of electrons in the base, the conductivity is much higher in the n-type emitter, although the emitter is usually very thin. Therefore, the electrons between high and low lifetime regions in the base flow through the emitter and are re-injected at the place where they can recombine with the holes which flow via the base. This was qualitatively verifieded by a DESSIS simulation[12] where two regions differing in lifetime (17.5 and 55 µs) were simulated and the current flow under steady-state conditions was calculated[13]. On top of the structure an emitter of 140 Ω/sq. connected the two regions. The main result was that the majority of the electrons takes the emitter path to flow from the high lifetime region to the low lifetime region (Fig. 7.4).

[12] The DESSIS simulation was calculated by Martin Hermle from Fraunhofer ISE.

[13] To avoid convergence problems a smooth transition between low and high lifetime was applied.

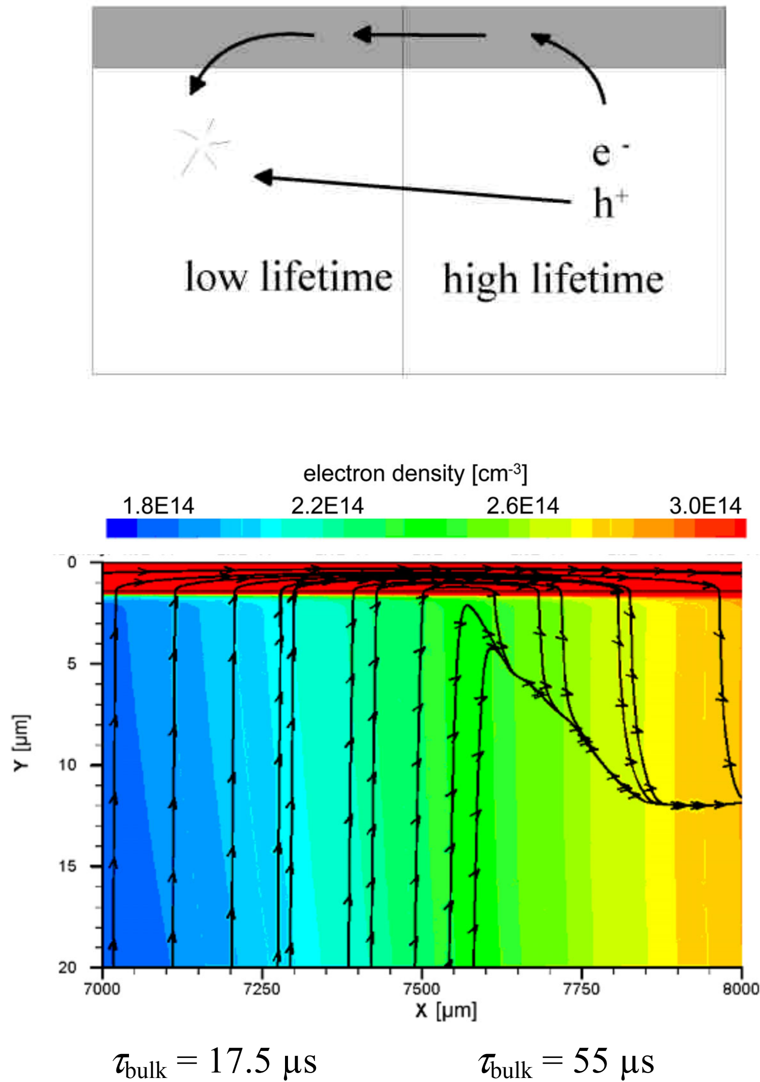

Fig. 7.4: Schematic current flow between a "good" (high lifetime) and a "bad" (low lifetime) grain is shown in the upper graph. The emitter provides the necessary conductivity for the minority carriers (electrons) to follow the gradient in the Fermi-level. The simulation with DESSIS of a sample with different bulk lifetimes is presented in the lower graph. The arrows denote the electron flow in the opposite direction and show that the emitter is the main path for the electrons to flow from the high-lifetime regions to the low lifetime regions.

In the following the current in the base can therefore be neglected in comparison to the current in the emitter, although the different carrier lifetimes (and thus concentrations) in the base are the driving force for the current. Only the emitter significantly acts as a conducting layer and thus the current is determined by

$$j_e \approx j_{e,emitter} = \frac{\sigma_{e,emitter}}{q} grad\left(\varepsilon_{FC_{base}}\right). \qquad 7\text{-}8$$

7.4 Evaluation of CDI measurements of samples with emitter

For the calculation of the current flow through the emitter, the equations derived in the previous section have to be modified according to the two-dimensional measurement results obtained from the CDI system.

The energy of the conduction band edge ε_C can be assumed constant throughout the base in vertical as well as in horizontal direction. With equation 7-1 and neglecting n_0 compared to Δn this leads to

$$j_{e,emitter}(x,y) = \frac{\sigma_{e,emitter}}{q} grad\left(kT \ln\left(\frac{\Delta n_{base}(x,y)}{N_C}\right)\right). \qquad 7\text{-}9$$

In this equation the free electron density in the base $\Delta n_{base}(x,y)$ per volume needs to be known but the CDI measures $\Delta N(x,y)$, the whole excess carrier density per area. The contribution of the emitter to the gradient is negligible because the layer is very thin. Dividing ΔN by the sample thickness W assumes homogeneous conditions in vertical directions and results in the correct dimensions, thus it is $\Delta n_{base}(x,y) = \Delta N/W$. Integration of the continuity equation 7-4 over the sample thickness W and the generation per area $F(x,y)$ results in

$$0 = \int_0^W \frac{div\, j_e}{q} dz - \frac{\Delta N(x,y)}{\tau_{eff}} + F(x,y). \qquad 7\text{-}10$$

Since the current through the emitter is dominant, the contribution of the base as a conducting layer is neglected. Using equation 7-8 it follows

$$\int_0^W \frac{div\, j_e}{q} dz \approx \int_{W_{base}}^W \frac{div\, j_{e,emitter}}{q} dz = \frac{W_{emitter}\, div\, j_e}{q} \qquad 7\text{-}11$$

where W_{base} and $W_{emitter}$ are the widths of the base and the emitter. Consequently using equations 7-7 and 7-9 to 7-11 this leads to the modification of the effective carrier lifetime τ_{eff} under steady-state conditions from equation 7-3 to

$$\tau_{eff} = \frac{\Delta N(x,y)}{F(x,y) + \frac{kT}{R_{sheet}\, q^2} div\, grad\left(\ln\left(\frac{\Delta N(x,y)}{W\, N_C}\right)\right)}. \qquad 7\text{-}12$$

This equation takes the emitter acting as conducting layer between regions of high and low carrier lifetime into account. The equation consists of measurable parameters or physical constants only. It neglects the resistance of the base in

vertical direction which might limit currents for very high gradients. This can be seen in the instability of the equation when the second summand in the denominator, which is the correction to the standard evaluation, becomes negative and could cause a singularity. These overcorrections would result in atypically high lifetimes. However, this does not cause real problems since for high lifetimes the dependence of V_{OC} and j_{SC} of lifetime saturates. These problems occur rather seldom since such artefacts appear only at very steep transitions.

In order to apply equation 7-12 to experimental data, the Laplace operator has to be transferred to the discrete, two-dimensional case. This is achieved by the difference quotient of the neighbouring pixels. With a being the distance between two pixels, the first derivative of a function f at the place (i,j) becomes

$$\frac{d}{dx} f(i,j) = \frac{f(i,j) - f(i-1,j)}{a} \tag{7-13}$$

from which the second derivative can be deduced as

$$\frac{d^2}{dx^2} f(i,j) = \frac{\frac{d}{dx} f(i+1,j) - \frac{d}{dx} f(i,j)}{a} = \frac{f(i+1,j) + f(i-1,j) - 2f(i,j)}{a^2}. \tag{7-14}$$

The same applies for the y-direction and therefore the Laplace operator in two dimensions is

$$\frac{d^2}{dx^2} f(i,j) + \frac{d^2}{dy^2} f(i,j) = \frac{f(i+1,j) + f(i-1,j) + f(i,j+1) + f(i,j-1) - 4f(i,j)}{a^2}. \tag{7-15}$$

Neither before nor after application of the Laplace operator the data was averaged or smoothed.

7.5 Modelling of multicrystalline silicon solar cells

The challenge of modelling a multicrystalline silicon solar cell is the implementation of spatially inhomogeneous material properties. One obvious parameter is the bulk lifetime which varies in multicrystalline silicon rather strongly. But the surface passivation might also vary with the different grain orientations. To model the influence of grain boundaries would, even if an appropriate model existed, rely on the knowledge of the position or at least the amount and electrical activity of the crystal defects. This calls for sophisticated two- or three-dimensional simulation. Such simulations are very complex and time

consuming and the measurements of factors like the surface passivation on different grains of multicrystalline silicon is not even possible due to the insufficient knowledge of the bulk properties. A solution to circumvent the complexity of the simulation is the reduction of a measured parameter distribution to one representative value. The most prominent parameter, the bulk lifetime, was investigated by several authors (e.g.[21,130-133]). The challenge is to find an appropriate weighting function which reflects the interactions of the regions in a solar cell under operation because a simple arithmetic or harmonic averaging leads to wrong results. An averaging procedure of $1/L$ [132] with L being the diffusion length or numerically derived weighting functions [131] improve the results but the local distribution of high and low lifetimes is not taken into account.

Another approach is a network simulation where small elementary cells with specific properties are connected via resistors (emitter sheet resistance, front and rear metallisation). With the carrier lifetime being the varying parameter such simulations fail to describe the cell performance, which is due to the neglect of the current flow between regions differing in lifetime [112].

In this chapter a network model of a solar cell is used in which the cell consists of several elementary diodes with individual dark saturation currents $I_{0,i}$ and short-circuit currents I_{sc}.(see Fig. 7.5). The effective minority carrier lifetime is acquired with a high resolution with the CDI system. The modelling procedure to derive the values of j_{sc} and V_{OC} for the actual completed solar cell is described in the following sections.

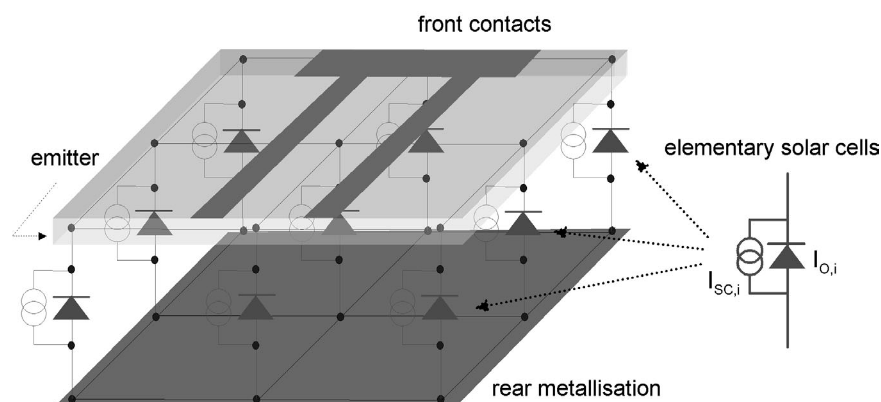

Fig. 7.5: Simplified model of a solar cell which consists of numerous elementary diodes with individual dark saturation currents $I_{o,i}$ and short circuit currents I_{sc}. Except for the optical properties (i.e. reflection), the contacts are not taken into account and series resistance and shunts are neglected. This facilitates the calculation since no sophisticated network simulation has to be applied.

7.5.1 Modelling of the short-circuit current density j_{SC}

Under short-circuit conditions the gradients in the quasi-Fermi level in vertical direction are very steep which leads to high current densities. All carriers which do not recombine are separated by the *p/n*-junction. Every elementary solar cell contributes its individual current to the overall current:

$$I_{SC} = \sum_{i=n}^{N} I_{SC,i} \ . \tag{7-16}$$

The individual current $I_{sc,i}$ depends on the material quality and thus on τ_{eff}, which can be determined in a lifetime measurement. However, the dependence of the short-circuit current density on the minority carrier lifetime cannot be expressed in analytical form with high precision. One reason is the AM1.5g spectrum not being available in analytical form. It is an essential input parameter for the absorption and reflectance properties which are in turn wavelength-dependent. Therefore the one-dimensional solar cell simulation program PC1D [90] was used to calculate the relationship between I_{sc} and τ for the specific solar cell structure under investigation (e.g. textured or planar front, antireflection coating, cell width). For the lifetime test structures of which the effective lifetime is measured (i.e. samples with emitter on front and passivated rear), the relation $I_{sc}(\tau_{eff})$ needs to be known. For samples with silicon nitride passivation on both surfaces $I_{sc}(\tau_{bulk})$ is important. Since τ_{eff} is neither an output nor an input parameter in PC1D, it was derived from the excess carrier density Δn in the middle of the cell and the generation in the cell G via

$$\tau_{eff} = \frac{\Delta n}{G} \ . \tag{7-17}$$

This is converted into an effective diffusion length L_{eff} with the equation

$$L_{eff} = \sqrt{D_e \tau_{eff}} \ . \tag{7-18}$$

The obtained relation is then approximated by a numerical fit (see Fig. 7.6) with the function

$$j_{sc}(l) = a\ln(l) + b\,l^3 + c\,l^2 + d\,l + e \qquad with \quad l = \frac{L}{\mu m} \ . \tag{7-19}$$

This simplifies further calculations since only the parameters *a,b,c,d* and *e* have to be implemented into the evaluation software and I_{SC} can now be calculated without

applying the simulation program for every single pixel (which would be too time consuming for an array of 288·288 = 82944 pixels).

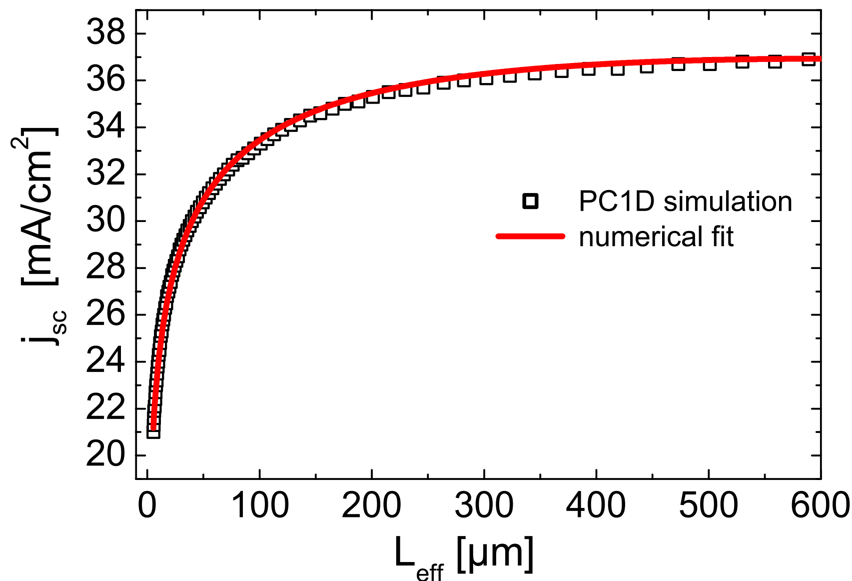

Fig. 7.6: Simulated short-circuit current as a function of effective diffusion length for the elementary solar cells. The PC1D-simulation was approximated by an analytical fit function to allow for a simplified calculation for every elementary solar cell.

7.5.2 Modelling of the open-circuit voltage V_{OC}

The dark saturation current I_0 is the current which can be measured in a diode under high reverse bias without illumination. It has its source in the thermal generation of carriers in a region of one diffusion length around the space charge region. In equilibrium, thermal generation equals recombination and areas with different recombination activity therefore have different dark saturation currents. Due to the high reverse bias nearly all thermally generated carriers are separated by the *p/n*-junction because of the large gradient in the quasi-Fermi level. The total dark saturation current is the sum of all *N* elementary cells:

$$I_0 = \sum_{i=1}^{N} I_{0,i} \;. \tag{7-20}$$

The dark saturation current is derived for every pixel of the CDI measurement from samples which already possess the passivated emitter on the front and a

passivated rear. Such sample has already seen the potentially upgrading gettering or degrading high-temperature processes as discussed in 7.2. It is calculated with

$$I_{0,i} = \frac{q\,D_e\,n_i^{\,2}A}{L_{eff,i}\,N_A} \qquad \text{7-21}$$

where D_e is the diffusion constant for electrons, n_i is the intrinsic carrier concentration, N_A is the doping concentration of the p-type base and A the area of the pixel (= elementary solar cell). $L_{eff,i}$ is the minority carrier diffusion length and it is linked to the effective minority carrier lifetime of the specific pixel $\tau_{eff,i}$ via:

$$L_{eff,i} = \sqrt{D_e\,\tau_{eff,i}}\ . \qquad \text{7-22}$$

For comparison, CDI measurements can also be taken from samples with silicon nitride surface passivation. The dark saturation current in the base I_{0b} is then calculated with

$$I_{0b,i} = \frac{q\,D_e\,n_i^{\,2}A}{L_i\,N_A}\cdot\frac{\sinh\left(\frac{W}{L_i}\right)+\frac{S\,L_i}{D_e}\cosh\left(\frac{W}{L_i}\right)}{\cosh\left(\frac{W}{L_i}\right)+\frac{S\,L_i}{D_e}\sinh\left(\frac{W}{L_i}\right)}. \qquad \text{7-23}$$

S is the surface recombination velocity at the rear and derived from a different set of samples (see section 6.2.2), W denotes the wafer thickness and L_i is the diffusion length derived from the bulk lifetime $\tau_{bulk,i}$ with the equation

$$L_i = \sqrt{D_e\,\tau_{bulk,i}}\ . \qquad \text{7-24}$$

For the calculation of I_0 from silicon nitride passivated samples, S and I_{0e} are not measured on every single pixel but the values are taken from previous measurements on different samples and assumed to be spatially homogeneous. The total dark saturation current is the sum of the base and the emitter dark saturation current I_{oe}, which was determined in section 5.3:

$$I_0 = I_{0b} + I_{0e} \qquad \text{7-25}$$

This procedure could add up to a higher uncertainty since these values might depend on crystal orientation.

The open-circuit voltage V_{OC} is a function of the dark saturation current I_0 and the short-circuit current density I_{SC}:

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{I_{sc}}{I_0}+1\right) \qquad \text{7-26}$$

where kT/q is the thermal voltage (25.9 meV at 25 °C). Thus the V_{OC} calculation is derived from an analytical expression only without the need for further sophisticated modelling of the interaction of the elementary solar cells.

7.6 Comparison of experiment with modelling

The theoretically derived equations of the previous chapter were implemented in a software called IDL® (Interactive Data Language) which is well suited for calculations with large matrices and their visualisation. The PC1D-model was adjusted according to surface texture, anti-reflection coating, thickness etc. depending on the solar cell structure. The key parameter, the effective minority carrier lifetime, was measured with the CDI system on neighbouring wafers of the ones from which the solar cells were manufactured. Thus the crystal structure was nearly identical. Both types of sample preparation were investigated. For the first type surface passivation was obtained by a silicon nitride passivation on both sides. The second type consisted of solar cell precursors which had an emitter passivated by a thin thermal oxide on the front and a thick oxide on the rear. For these samples the evaluation of the CDI measurement was applied, which takes the conductivity of the emitter into account. From the measured minority carrier lifetimes a "prediction" of the V_{OC} and j_{SC} values is calculated and compared to experimental results from solar cells which were manufactured on equivalent neighbouring wafers.

7.6.1 Prediction of solar cell parameters from silicon nitride passivated samples

For a silicon nitride passivated sample, the bulk lifetime τ_{bulk} was extracted from the CDI measurement (surface recombination can be neglected). The equations of section 7.5.1 were applied and the calculated value for the j_{SC} was plotted in comparison to the measured value of the completed solar cells (Fig. 7.7). The bisecting line is also shown and visualises a perfect match in which all data points would be lined on this diagonal. The quality of the modelling can therefore easily be assessed by the deviation from this line.

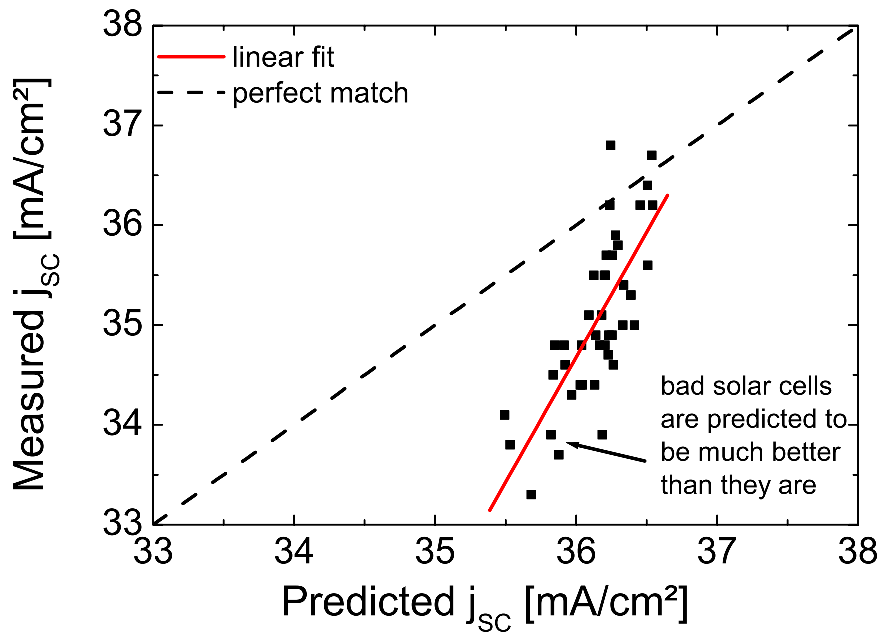

Fig. 7.7: Comparison of measured and calculated values for j_{SC} from an all silicon nitride passivated sample. The diagonal represents a perfect match between measurement and modelling, which was not achieved with this calculation.

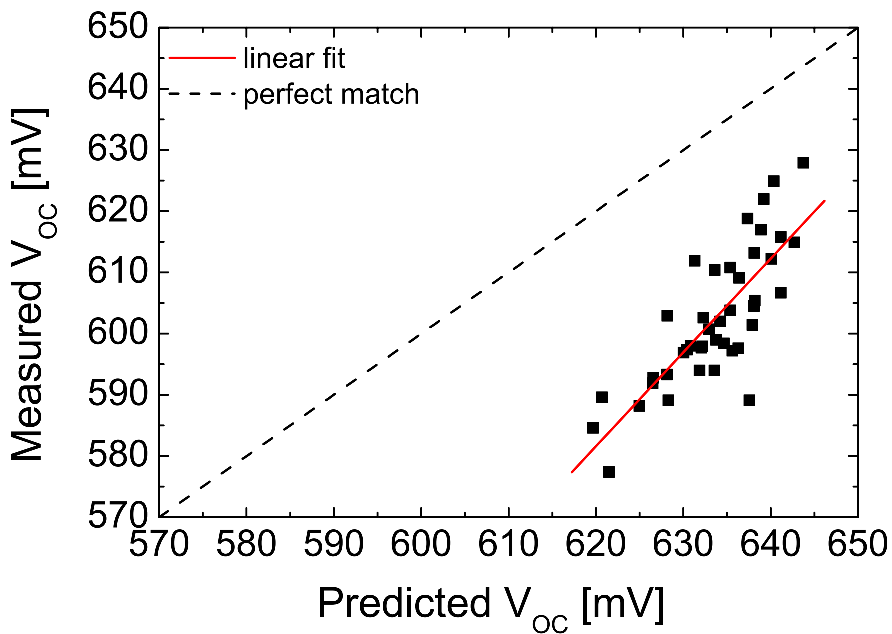

Fig. 7.8: Comparison of measured and calculated values for V_{OC} from an all silicon nitride passivated sample. The diagonal represents a perfect match between measurement and modelling, which was not achieved with this calculation.

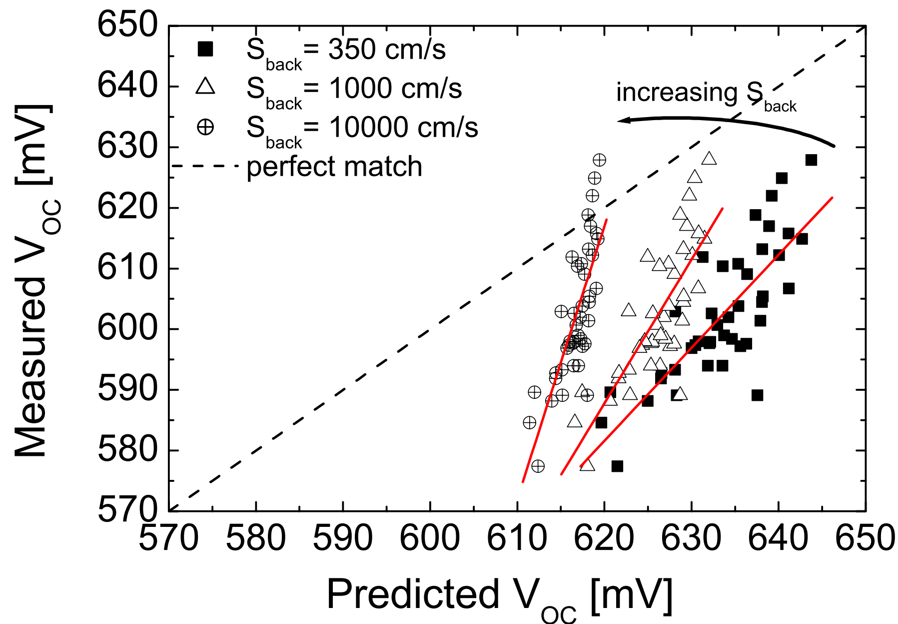

Fig. 7.9: Effect of variation of the rear surface recombination velocity S_{rear}. An increment did not improve the quality of the prediction on the base of silicon the nitride passivated lifetime sample and experimentally measured values.

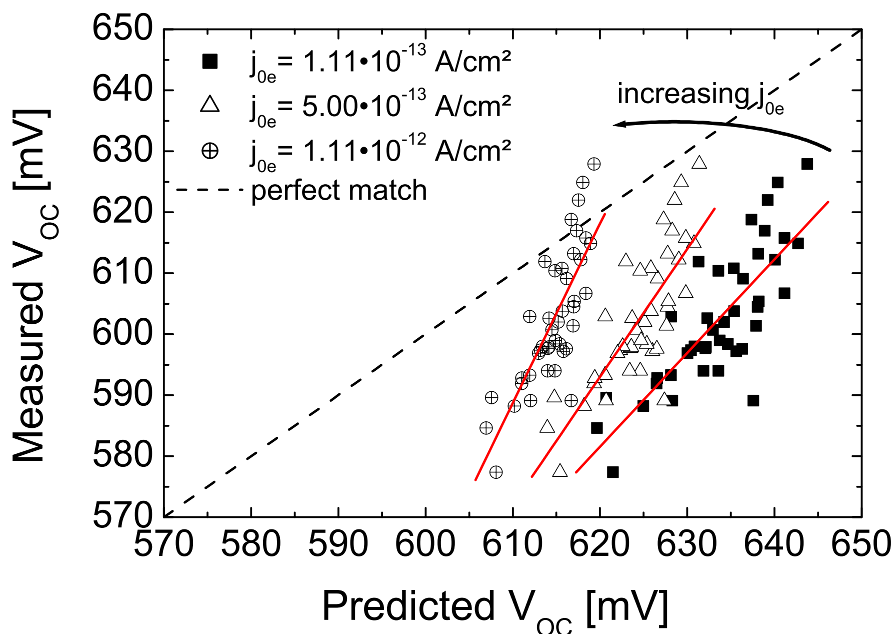

Fig. 7.10: Effect of variation of the emitter dark saturation current density j_{0e}. An increment did not improve the quality of the prediction on the base of silicon the nitride passivated lifetime sample and experimentally measured values.

Although the modelling in principal led to correct predictions (solar cells with high j_{SC} were also predicted to be better than the ones with low j_{SC} values) no good agreement was achieved. The same applies for the modelling of the V_{OC} values (Fig. 7.8), where the solar cells were predicted to be much better than the experiment could achieve. To check whether a too optimistic emitter dark saturation current density j_{0e} or a too low rear surface recombination S_{rear} had caused this deviation of experiment from theory, a parameter variation was performed (Fig. 7.9). But the effect was an even worse correlation since in the calculation the good solar cells suffered significantly more from the increased recombination than the bad ones.

The deviations might be due to hydrogenation of the bulk of multicrystalline silicon during silicon nitride passivation. As long as the same effect does not occur during solar cell processing, the sample does not reflect the real material properties and modelling has to fail. Thus a prediction based on the lifetime measurement of silicon nitride passivated samples does not lead to satisfying results.

7.6.2 Prediction of solar cell parameters from samples with a solar cell structure

Since the prediction of solar cells from the silicon nitride passivated samples did not lead to a good correlation between the measured solar cell parameters and the predicted values, a sample with an emitter on the front (passivated by a thin thermal oxide) and a thick oxide on the rear was used to predict the values of j_{SC} and V_{OC} (Fig. 7.11 and Fig. 7.12).

The match between measurement and model was improved compared to the silicon nitride passivated sample. The linear fit of the data points reveals that the predicted values of the experimentally measured “good” solar cells ($\geq$ 38 mA/cm^2 and $\geq$ 625 mV) were systematically too low whereas the model predicted too high values of j_{SC} and V_{OC} for “bad” solar cells. This can be explained by the emitter present during the lifetime measurement which enabled a carrier flow between regions of high and low lifetime. Thus the emitter-correction derived in section 7.4 had to be applied. It corrected the current flow from good regions of high lifetime (loss of carriers) into bad regions of low lifetime (gain of carriers).

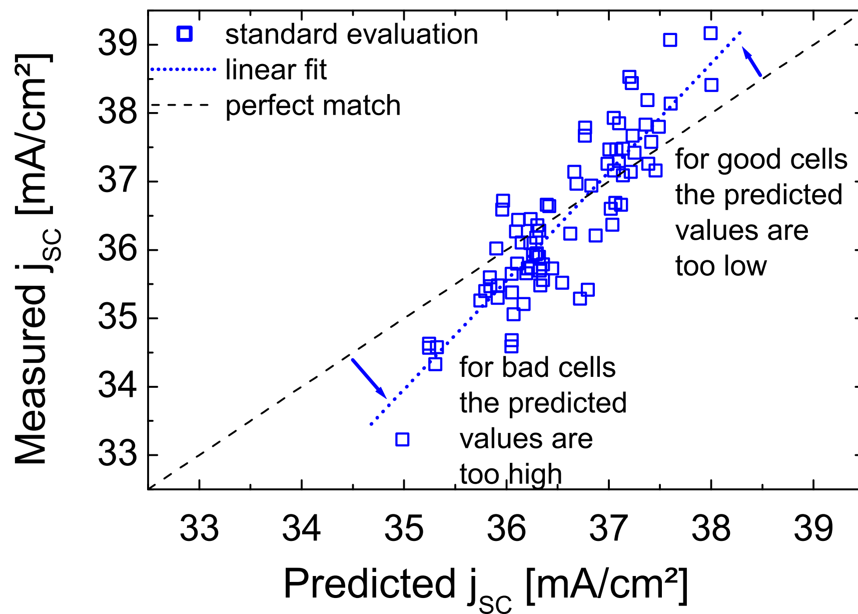

Fig. 7.11: Comparison of measured and calculated values for j_{SC} based on a sample with an emitter on the front and a thick thermal oxide on the rear. The match between simulation and experiment is much better than for the prediction based on the silicon nitride passivated sample. However, for good cells the predicted values are too low whereas for bad cells the predicted values are too high.

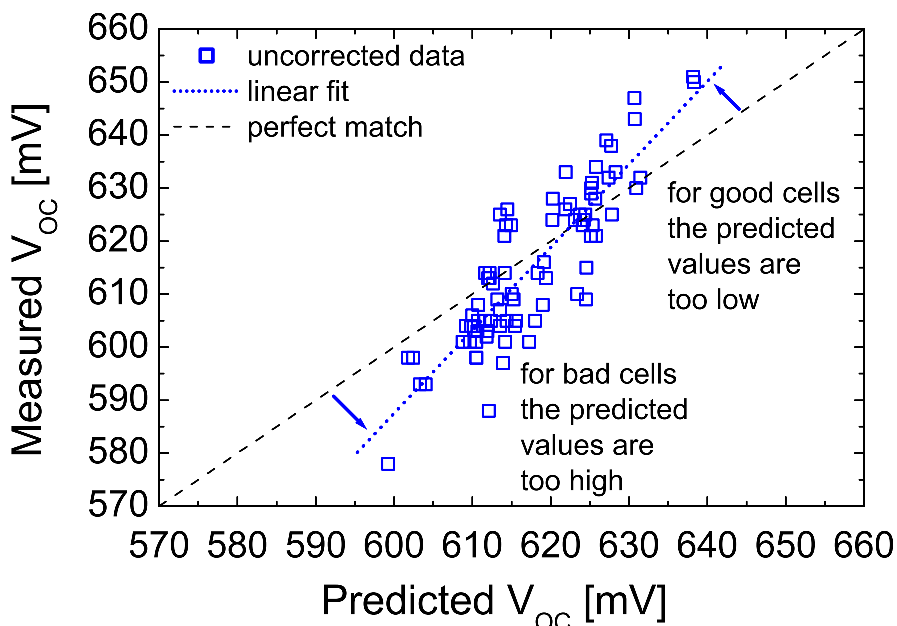

Fig. 7.12: Comparison of measured and calculated values for V_{OC} based on a sample with an emitter on the front and a thick thermal oxide on the rear. The match between simulation and experiment is much better than for the prediction based on the silicon nitride passivated sample. However, for good cells the predicted values are too low whereas for bad cells the predicted values are too high.

The topography changed from a smooth image with the standard evaluation to a coarse grained image after the emitter-corrected evaluation (Fig. 7.13 and Fig. 7.14).

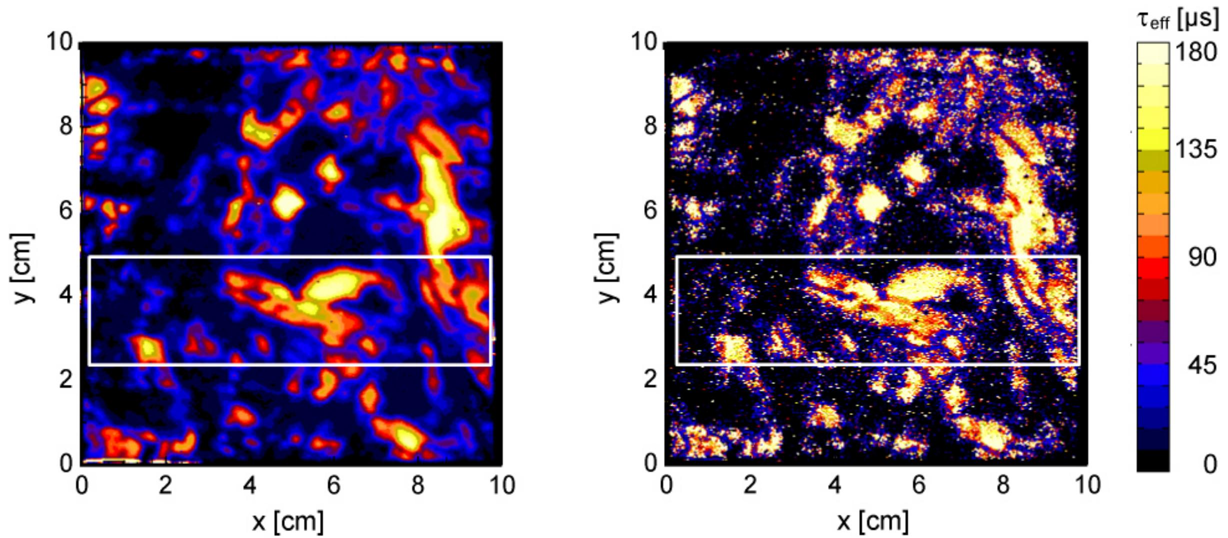

Fig. 7.13: CDI measurement of a multicrystalline silicon wafer with emitter on the front and thick oxide on the rear. The left-hand image shows the lifetime topography as measured, the right-hand image after the emitter-corrected evaluation. The white rectangle marks the area which is shown in the zoom in Fig. 7.14.

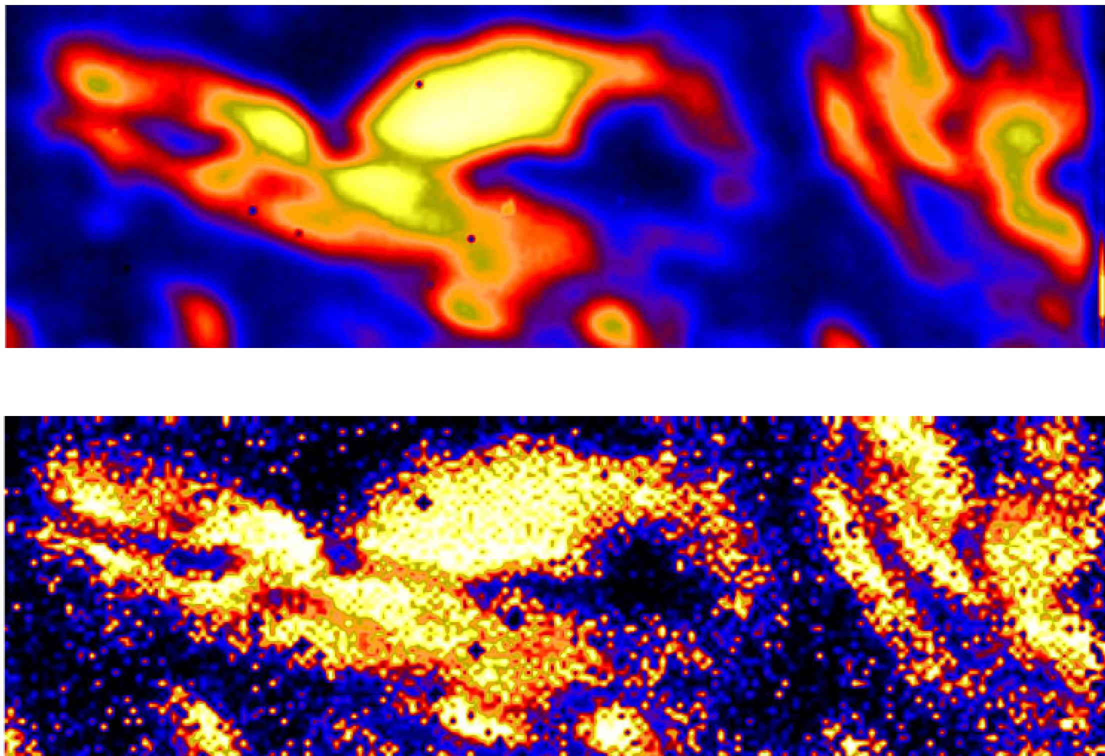

Fig. 7.14: Zoom of Fig. 7.13. CDI measurement of a multicrystalline silicon wafer with emitter on the front and thick oxide on the rear. The upper image shows the lifetime topography as measured, the lower image after the emitter-corrected evaluation.

This is also visible in the histograms of these two images where the emitter-corrected evaluation led to an increment of the pixels with very low lifetimes and very high lifetimes at the expense of the medium lifetime pixels (Fig. 7.15).

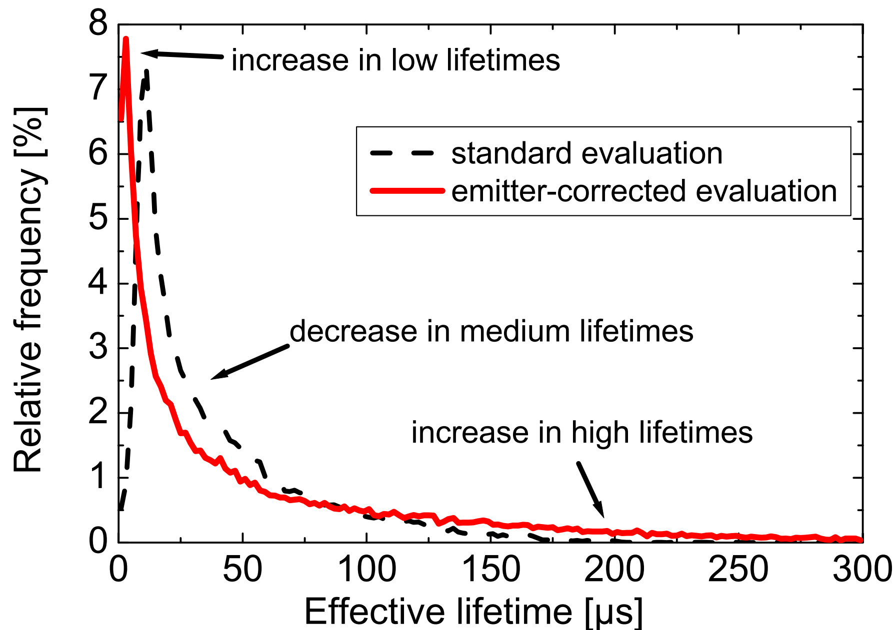

Fig. 7.15: Histogram of the CDI measurement of a multicrystalline silicon wafer with emitter on the front and a thick oxide on the rear after standard evaluation (dashed line) and after the emitter-corrected evaluation (solid line).

The result of a prediction from these corrected data changed remarkably (Fig. 7.16 and Fig. 7.17). The linear fit of the predicted values from the emitter-corrected data now matched the ideal case nearly perfectly. The current flow from good regions with high lifetime via the emitter to bad regions of low lifetime was successfully corrected.

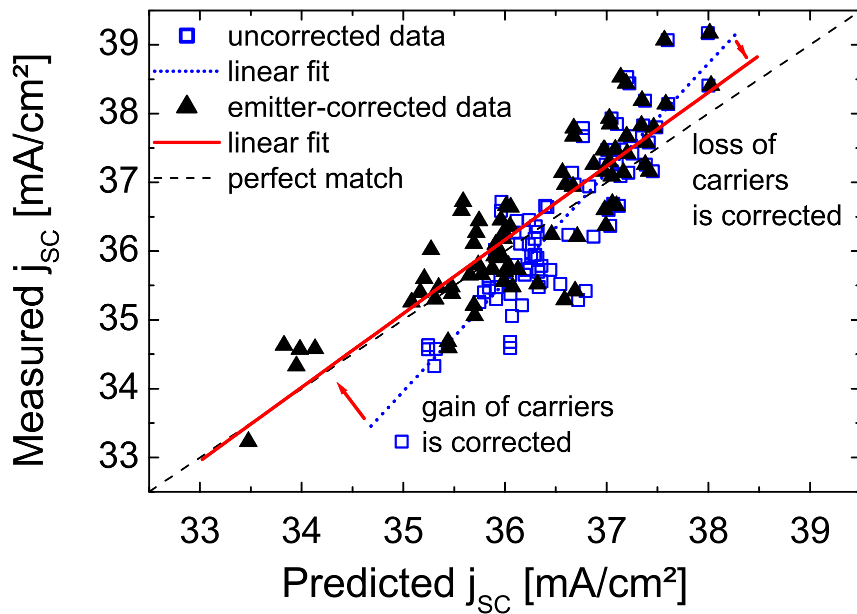

Fig. 7.16: Comparison of measured and calculated values for j_{SC} based on a sample with emitter on the front and thick thermal oxide on the rear. The linear fit of the predicted values based on the emitter-corrected data now matches the ideal case nearly perfectly. The current flow from good regions with high lifetime via the emitter to bad regions of low lifetime was successfully corrected.

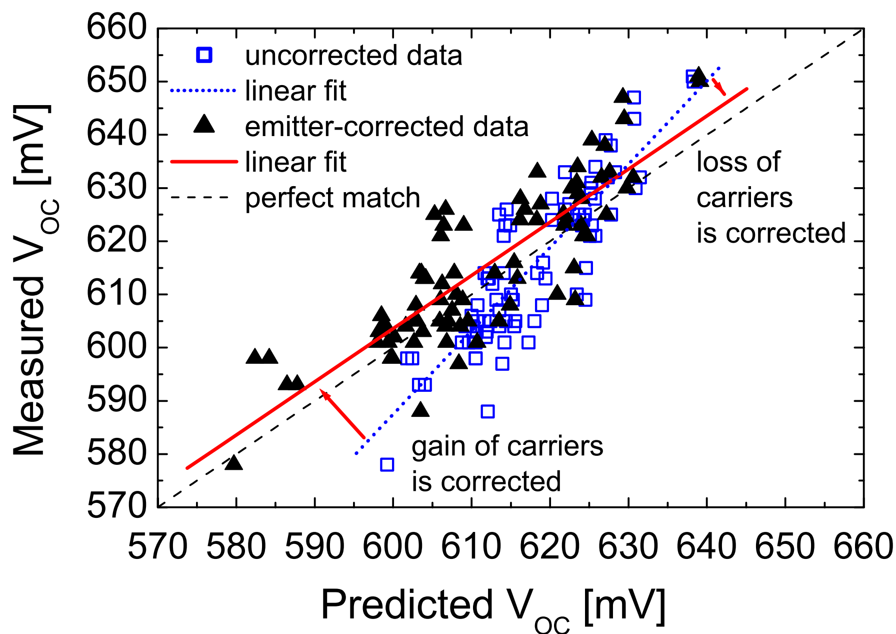

Fig. 7.17: Comparison of measured and calculated values for V_{OC} based on a sample with emitter on the front and thick thermal oxide on the rear. The linear fit of the predicted values based on the emitter-corrected data is now parallel to the ideal case. The current flow from good regions of high lifetime via the emitter to bad regions of low lifetime was successfully corrected.

This evaluation method was applied in further experiments to a total of 200 solar cells of different thicknesses and surface texture. The resulting graphs for j_{SC} and V_{OC} are presented in Fig. 7.18.

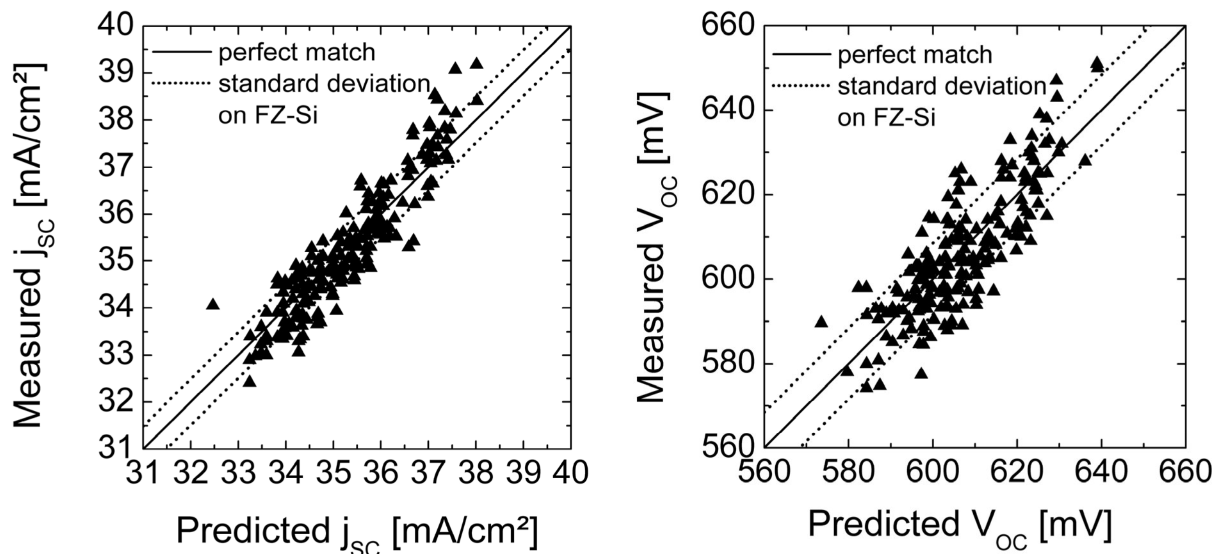

Fig. 7.18: Result of 200 solar cells modelled with the developed procedure based on carrier lifetime reference samples with emitter. The dotted lines represent the standard deviation of 140 solar cells which were processed on FZ-silicon (which possesses nearly ideally homogeneous material parameters).

In the same experiment 140 solar cells were processed on FZ-silicon which has nearly ideally homogeneous material parameters. The standard deviation from the corresponding mean value was $\sigma_{FZ} = \pm\, 0.49$ mA/cm^2 for j_{SC} and $\sigma_{FZ} = \pm\, 8.4$ mV for V_{OC} (the shading losses of different grid designs and whether the front was textured or not, was taken into account). This denotes the technological limit of the process reproducibility of this experiment and represents the limit of the achievable accuracy. For the multicrystalline silicon solar cells, the standard deviation from the experimental value was $\sigma_{mc} = \pm\, 0.54$ mA/cm^2 for j_{SC} and $\sigma_{mc} = \pm\, 8.4$ mV for V_{OC}. Hence the accuracy of the predicted values was (almost) within the technological fluctuation. In an error propagation analysis, the influence of an uncertainty of a 10 % of the CDI measurement (absolute deviation, not relative from one pixel to the other) resulted in an uncertainty of $\Delta j_{SC} = 0.02\text{-}0.16$ mA/cm^2 and $\Delta V_{OC} = 1.3\text{-}1.4$ mV for lifetime values between $\tau = 5$ µs and $\tau = 150$ µs. The higher deviations were obtained for the lower lifetimes due to the stronger

dependence of j_{SC} and V_{OC} on carrier lifetime for smaller values. Another factor which has to be taken into account is the base resistivity. For a nominally 1.5 Ω cm multicrystalline silicon the effect of $\sigma_\rho = \pm 0.2$ Ω cm on the short-circuit current density was calculated to be $\Delta j_{SC} = 0.04$ mA/cm^2 for low lifetimes (5 µs) and $\Delta j_{SC} = 0.02$ mA/cm^2 for high lifetimes (150 µs). For V_{OC} (rather independent of lifetime) the result was $\Delta V_{OC} = 3.7$ mV. In a future development of the modelling the spatial distribution of the base doping should be considered to further improve the accuracy.

7.6.3 Fill factor

For a complete modelling of the solar cells in addition to the values for j_{SC} and V_{OC}, the fill factor (FF) has to be calculated. However, the fill factor is nearly independent of carrier lifetime and the contact metallisation plays the major role. This is obvious for a possible shunting of the *p*/*n*-junction or for the series resistance which can easily limit the solar cell performance at the maximum power point. But also a metallisation penetrating the space-charge region can cause excessive losses in the fill factor. These parameters are mainly process-induced and therefore not directly determinable by carrier lifetime measurements prior to metallisation. This aspect lies beyond the scope of this study. In section 6.2.4 a closer look is taken at the dependence of the fill factor on material properties like grain boundaries or crystal orientation.

7.7 Chapter summary

In this chapter the influence of inhomogeneous minority carrier lifetime on the solar cell parameters j_{SC} and V_{OC} was investigated. It proved necessary to use a sample for carrier lifetime measurement which was exposed to all processes changing the carrier lifetime in multicrystalline silicon like emitter diffusion and oxidation. This caused the problem of the emitter providing the path for a current flowing from regions of high minority carrier density to regions of low minority carrier density. This effect obscured the locally determined minority carrier lifetime. Due to the loss of carriers via the emitter in the good regions, a lower carrier density (and thus a lower lifetime) was measured than the material quality

allowed, whereas in the bad regions a higher carrier density (and thus a higher lifetime) was measured.

A method was introduced to re-calculate this current flow and to determine the “real” lifetime. A simplified network model was applied in which a solar cell consists of numerous elementary cells/diodes. According to the resolution of the measurement set-up, individual dark saturation current densities were assigned to every pixel of the carrier density image. On the base of 200 independent solar cells it was shown that with the developed algorithm an accurate modelling of the solar cell parameters j_{SC} and V_{OC} is possible.

8 Summary

In this thesis multicrystalline silicon was studied with respect to its suitability for high-efficiency silicon solar cells. Since the minority carrier lifetime is the key parameter determining the efficiency of a silicon solar cell, it was investigated in detail throughout this work.

The application of the processes designed for high-purity monocrystalline silicon did not result in good solar cells because the material degraded during the high-temperature oxidations. Therefore new processes and process sequences had to be developed.

Special attention was paid to the **changes of the material quality** during solar cell production. Phosphorus diffusion proved a very efficient gettering process to remove impurities like iron, which act as recombination centres. Average minority carrier lifetimes of 100 µs after gettering were obtained on commercially available standard production material. However, the gettering efficiency was strongly dependent on crystallographic defects, i.e. gettering was very efficient in regions of low dislocation density whereas it did not work in highly dislocated areas. A microscopic model was discussed which explains the observed results.

The **oxidation** of the silicon surface is a multi-purpose tool for high-efficiency solar cell production because the oxide serves as a masking layer and simultaneously passivates the surface. The usual process temperatures of 1050 °C severely degrade the material quality of multicrystalline silicon by activating intrinsic defects. A wet oxidation process at 800 °C was developed in which steam increases the growth rate. The lower temperature reduced the dissolution of precipitated impurities. Thus, the degradation of multicrystalline silicon during oxidation was virtually eliminated. An understanding of the physical mechanisms was obtained and used for further process optimisation.

The concepts developed for monocrystalline high-efficiency silicon solar cells were adapted to the special demands of multicrystalline silicon. This included the **texturing** of the front surface. A method based on plasma technology and a mask deposited at low temperatures was developed. This process etches silicon

independent of the crystal orientation. Its application reduced the reflectance of the bare silicon surface (without additional antireflection coating) from 36 % to 14 % weighted with the solar spectrum AM1.5g. The **emitter diffusion** was adjusted to the new texture. The surface was successfully passivated with a single phosphorus emitter diffusion and a thin thermal oxide layer of about 15 nm. Open-circuit voltages of 660 mV were achieved for 1 Ω cm FZ material. The thin oxide layer allowed for the use of a double layer antireflection coating resulting in weighted reflectance values of 4 %. Together with a rear surface showing high internal reflectance, this structure provided very good **light-trapping** which was particularly important for thin solar cells.

The mirror-like **rear surface structure** was composed of a 100 nm thick silicon oxide and a layer of evaporated aluminium. To form the contacts, the aluminium was laser-fired through the oxide layer. The effective rear surface recombination velocity was determined for a wide range of base doping densities and contact spacing. Since the lateral conductivity is reduced due to grain boundaries, multicrystalline silicon requires a smaller distance between the contacts than monocrystalline references. For a typical contact spacing of 500 µm an effective surface recombination value of $S_{eff} \approx 120$ cm/s was measured for 1.5 Ω cm base resistivity.

The minority carrier lifetime of multicrystalline silicon increases by application of the developed process sequence. At the same time a cell structure is set up with well-passivated surfaces and excellent optical properties. **Multicrystalline silicon solar cells exceeding 20 % efficiency** were successfully produced on less than 100 µm thin wafers. Independently confirmed 20.3 % on 1 cm^2 (V_{OC} = 664 mV, j_{SC} = 37.7 mA/cm^2, FF = 80.9 %) and 19.8 % on 4 cm^2 (V_{OC} = 638 mV, j_{SC} = 38.8 mA/cm^2, FF = 80.0 %) are the highest efficiencies obtained on multicrystalline silicon to date. The average efficiencies of 18 % show the potential of the developed process on large area cells. Equally high values were achieved on boron-doped wafers produced by Kawasaki Steel (η = 20.3 %), ScanWafer (η = 20.1 %), Eurosolare (η = 19.3 %) and Dai-ichi Kiden (η = 19.9 %) as well as

on gallium-doped wafers from Dai-ichi Kiden (η = 19.5 %). This demonstrates the capability of multicrystalline silicon as a material for high-efficiency solar cells.

The efficiency of the solar cells was almost entirely limited by the material quality. This predestined them for **modelling of the influence of inhomogeneous carrier lifetimes** on solar cell parameters. Wafers with emitter on the front and oxide on the rear were used as lifetime measurement samples. They reflect the material properties better than the standard silicon nitride passivated samples, since the emitter diffusion and the oxidation during cell processing can change the material properties. The emitter present during minority carrier density measurements increased the current flow from regions of high to regions of low lifetime which blurred the results. These effective measurement data were deconvoluted using an analytical model in order to obtain the microscopic material quality at a particular position. A model of elementary solar cells connected in parallel was applied. The dark saturation currents of all elementary cells, calculated from the carrier lifetime measurements, were simply summed up. On the base of 200 solar cells, it was shown that an accurate modelling of the solar cell short-circuit current density and the open-circuit voltage was possible with the developed algorithm.

Deutsche Zusammenfassung

In der vorliegenden Doktorarbeit wurde multikristallines Silizium im Hinblick auf seinen Einsatz in hocheffizienten Solarzellen eingehend untersucht. Da die Lebensdauer der Minoritätsladungsträger der Schlüsselparameter ist, welcher die Effizienz einer Siliziumsolarzelle bestimmt, wurde die Messung dieser Lebensdauer während der gesamten Arbeit zur Beurteilung der Materialqualität und der Güte der Oberflächenpassivierung eingesetzt.

Die Anwendung der Standardprozesse, die für hochreines monokristallines Silizium entwickelt wurden, erbrachten auf multikristallinem Silizium keine guten Resultate, da die Materialqualität von den hohen Oxidationstemperaturen stark gemindert wurde. Deshalb mussten neue Prozesse und Prozessfolgen entwickelt werden.

Besonderes Augenmerk wurde hierbei auf die Veränderungen der Materialqualität bei der Anwendung verschiedener Hochtemperaturprozesse gelegt. Hierbei hat sich herausgestellt, dass eine Phosphordiffusion sehr effektiv Verunreinigungen wie z.B. Eisen aus dem Material entfernen kann. Auf handelsüblichem multikristallinem Silizium konnten mittlere Lebensdauern von 100 µs nach einem solchen sogenannten Getterprozess erreicht werden. Allerdings wies die Getter-Effizienz eine starke Abhängigkeit von kristallografischen Defekten auf, d.h. sie war hoch in Bereichen mit nur geringen Versetzungsdichten wohingegen in stark versetzten Gebieten keine Verbesserung zu erzielen war. Die Ergebnisse konnten anhand eines mikroskopischen Modells erklärt werden.

Die Oxidation der Siliziumoberfläche ist ein vielseitig einsetzbarer Prozess für die Herstellung hocheffizienter Solarzellen, da Siliziumoxid sowohl als Maskierungsschicht als auch zur elektrischen Passivierung der Oberfläche genutzt werden kann. Die üblicherweise eingesetzten sehr hohen Prozesstemperaturen von ca. 1050 °C aktivieren intrinsische Defekte und führen somit zu einer Degradation multikristallinen Siliziums. Deshalb wurde ein feuchter Oxidationsprozess bei 800 °C entwickelt, bei dem zugeführter Wasserdampf die Oxidationsrate deutlich erhöht. Diese verhältnismäßig geringe Temperatur reduziert die Auflösung präzipitierter Verunreinigungen deutlich, die Verschlechterung der Materialqualität wurde somit fast vollständig verhindert. Das erworbene physikalische Verständnis der Prozesse wurde dazu verwendet, zielgerichtet Herstellungsprozesse für multikristalline Siliziumsolarzellen zu entwickeln und zu optimieren.

Die Konzepte zur Herstellung hocheffizienter Siliziumsolarzellen wurden an die speziellen Bedürfnisse multikristallinen Siliziums angepasst. Hierzu zählte auch die Strukturierung der Vorderseite zur verbesserten Lichteinkopplung. Für diese sogenannte Texturierung wurde ein Plasma-Prozess für eine bei niedrigen Temperaturen hergestellte Maske entwickelt, der unabhängig von der Kristallorientierung die Oberfläche ätzt. Die mit dem Sonnenspektrum AM1.5g gewichtete Reflexion der blanken Siliziumoberfläche konnte somit von 36 % auf 14 % gesenkt werden. Die Emitterdiffusion wurde an diese Textur angepasst, somit konnte die Oberfläche mit einer einstufigen Phosphordiffusion und einem dünnen thermischen Oxid von ca. 15 nm Dicke effektiv passiviert werden. Dabei wurden offene Klemmenspannungen von 660 mV auf bordotiertem FZ Silizium mit einem spezifischen Basiswiderstand von 1 Ω cm erzielt. Die nur sehr dünne Oxidschicht ermöglichte das Aufbringen einer doppellagigen Antireflexbeschichtung zur weiteren Minderung der Reflexion auf 4 %. Zusammen mit einer sehr guten internen Verspiegelung wirkt diese Struktur als Lichtfalle, was besonders für dünne Wafer von Bedeutung ist.

Die verspiegelte Rückseite besteht aus einer 100 nm dicken Oxidschicht und aufgedampftem Aluminium. Zur Kontaktierung wurde das Aluminium lokal mittels eines Laserstrahls durch das Oxid gefeuert. Die effektive Rekombinationsgeschwindigkeit an der Rückseite wurde für einen großen Bereich von Basisdotierungen und Kontaktabständen ermittelt. Es wurde festgestellt, dass multikristallines Silizium aufgrund der durch die Korngrenzen reduzierten Querleitfähigkeit mehr Kontaktpunkte benötigt als vergleichbares monokristallines Material. Für einen typischen Kontaktabstand von 500 µm wurde auf Silizium mit einem spezifischen Widerstand von 1.5 Ω cm ein Wert von 120 cm/s gemessen.

Mit der neuen Prozessfolge konnte die Lebensdauer der Ladungsträger deutlich erhöht werden, während gleichzeitig eine Zellstruktur mit sehr gut passivierten Oberflächen und exzellenten optischen Eigenschaften aufgebaut wurde. Wirkungsgrade von über 20 % auf Scheibendicken von weniger als 100 µm wurden erreicht. Diese wurden in kalibrierten Messungen unabhängiger Labore bestätigt. Die Werte von 20.3 % auf Zellflächen von 1 cm^2 (V_{OC} = 664 mV, j_{SC} = 37.7 mA/cm^2, FF = 80.9 %) und 19.8 % auf 4 cm^2 (V_{OC} = 638 mV, j_{SC} = 38.8 mA/cm^2, FF = 80.0 %) sind die höchsten bis heute veröffentlichten Werte für multikristallines Silizium. Die Mittelwerte von kleinen Zellen auf einer großen Scheibe lagen bei 18 % und zeigen das Potential der entwickelten Struktur für großflächige Zellen auf. Die hohen Wirkungsgrade waren nicht auf ein

bestimmtes Material beschränkt. Es wurden vergleichbar gute Ergebnisses auf bordotierten Scheiben der Hersteller Kawasaki Steel (η = 20.3 %), ScanWafer (η = 20.1 %), Eurosolare (η = 19.3 %) und Dai-ichi Kiden (η = 19.9 %) sowie für galliumdotierte Scheiben von Dai-ichi Kiden (η = 19.5 %) erzielt. Dies erbrachte den Nachweis, dass multikristallines Silizium bei richtiger Prozessführung als Material für hocheffiziente Solarzellen eingesetzt werden kann.

Die Wirkungsgrade der Solarzellen waren fast ausschließlich durch die Materialqualität begrenzt. Diese sind somit ideal für die Modellierung des Einflusses inhomogener Lebensdauerverteilungen auf die Solarzellenparameter geeignet. Um die Verhältnisse in der Solarzelle möglichst genau nachzubilden, wurden für die Lebensdauermessung Proben eingesetzt, die auf der Vorderseite einen Emitter aufweisen und deren Rückseite mit einem Oxid passiviert ist. Die üblicherweise verwendeten Proben mit Siliziumnitridbeschichtung zur Oberflächenpassivierung bilden nämlich eine mögliche Materialverbesserung durch Emitterdiffusion oder eine Degradation durch Oxidation nicht ab. Zusätzlich kann es durch eine Wasserstoffpassivierung während der Abscheidung des Siliziumnitrids zu einer weiteren Veränderung der Materialeigenschaften kommen. Allerdings ermöglichte der Emitter durch seine hohe Leitfähigkeit einen teilweisen Ladungsträgerausgleich zwischen Bereichen hoher und niedriger Lebensdauer. Somit fielen die Messergebnisse in guten Bereichen zu niedrig und in schlechten Bereichen zu hoch aus, die lokale Materialqualität wurde bei einer solchen Probe nicht korrekt ermittelt. Mit Hilfe eines analytischen Algorithmus konnte jedoch die tatsächliche Lebensdauer berechnet werden, wie sie sich ohne Emitter darstellen würde. Diese lokal bestimmten Materialparameter wurden für die Modellierung von Solarzellen in einem einfachen Modell benutzt, welches aus parallel geschalteten Elementarsolarzellen besteht. Hierbei wurden die Dunkelsättigungsströme der Elementarzellen, die aus den Lebensdauern berechnet wurden, aufsummiert. Anhand von 200 Solarzellen wurde experimentell bestätigt, dass eine korrekte Modellierung des Kurzschlussstromes und der offenen Klemmenspannung mit diesem Verfahren möglich ist.

Appendix

A.1 Transient Photoconductance Decay (PCD)

A photoconductance decay measurement involves the generation of excess carriers by a short pulse of illumination which is rapidly cut off. The resulting decay of carriers back to their equilibrium concentration is monitored via the photoconductance. The net excess conductance $\Delta\sigma$ is given by:

$$\Delta\sigma = q\Delta n_{av}(\mu_e + \mu_h)W \qquad \text{A-1}$$

where q is the elementary charge, μ_e and μ_h are the electron and hole mobilities and W is the sample thickness. With a carrier mobility model (e.g. [134]) this allows for the calculation of the average excess carrier density Δn_{av} and therefore the effective carrier lifetime by differentiation of the trace:

$$\tau_{eff} = -\frac{\Delta n_{av}}{d\Delta n_{av}/dt}. \qquad \text{A-2}$$

In the case of μW-PCD the excess conductance $\Delta\sigma$ is determined by measuring the reflection of microwaves directed at the sample surface. Since this reflectivity is a highly non-linear function of the free carrier density, this method is restricted to small signals, a drawback which can be circumvented by using a steady-state bias-light generating a background carrier density on which the small transient light pulse is superimposed. Each bias-light setting will result in one value but the injection-level in the sample remains unknown. A further complication arises when the measured lifetime is injection-level dependent since the described set-up measures differential lifetimes instead of actual lifetimes. Taking many measurements at different bias light intensities and working back from the measured lifetime, the excess carrier concentration can be simulated and accurate results of actual lifetimes are obtained [85,86]. However, this method requires many time-consuming traces at each individual bias-light setting and therefore was used only once within this work (section 4.3.3) where the small sample size (4 cm^2) did not permit the use of the QssPC method which has a larger measurement spot (about 11 cm^2). The use of the CDI technique, which is an

optical measurement system, was not possible either because the surface texture could falsify the result.

A.2 Quasi-steady state Photoconductance (QssPC)

The inductively coupled QssPC technique is a commercially available system for the measurement of minority carrier lifetimes over a broad range of excess carrier densities [135]. It uses a flashlight for carrier generation and an inductively coupled coil for the measurement of the photoconductance of the sample wafer.

Under steady-state conditions the effective lifetime is given by the expression

$$\tau_{eff} = \frac{\Delta n_{av}}{G_L} \qquad \text{A-3}$$

where G_L is the generation rate produced by the incident light. If the light source is held at a steady illumination, the sample will be in truly steady state, but will also quickly be heated and change the lifetime. To avoid such heating, the generation light is slowly reduced to zero over several milliseconds (typically 2 ms). The decay is long enough to ensure that the sample remains in steady state except for very high lifetimes. The slowly decaying illumination provides the added advantage of a measurement covering a large range of carrier densities for which the lifetimes can be calculated. The average excess carrier density Δn_{av} is determined at each point of the decay by equation A-1, but in contrast to the µw-PCD the excess conductivity is measured by an inductively coupled coil at each point of the trace. The generation rate G_L is required at each point also and is determined by simultaneously measuring the intensity of the flash decay with a calibrated reference cell. This determines the flux of photons N_{ph} which reach the sample and can potentially generate electron-hole pairs. Any real sample will only absorb a fraction f_{abs} of these available photons, hence the bulk generation rate in the wafer is:

$$G_L = \frac{N_{ph} f_{abs}}{W} . \qquad \text{A-4}$$

For an accurate measurement of samples which might well differ in thickness and optical properties (antireflection coating, texture, etc.) the absorption factor f_{abs} needs to be determined for the individual sample. This problem is addressed in section A.3. The effective lifetime is proportional to the ratio of the

photoconductance to the reference cell signal. Fig. A.1 shows a typical QssPC measurement and the corresponding plot of lifetime versus excess carrier density.

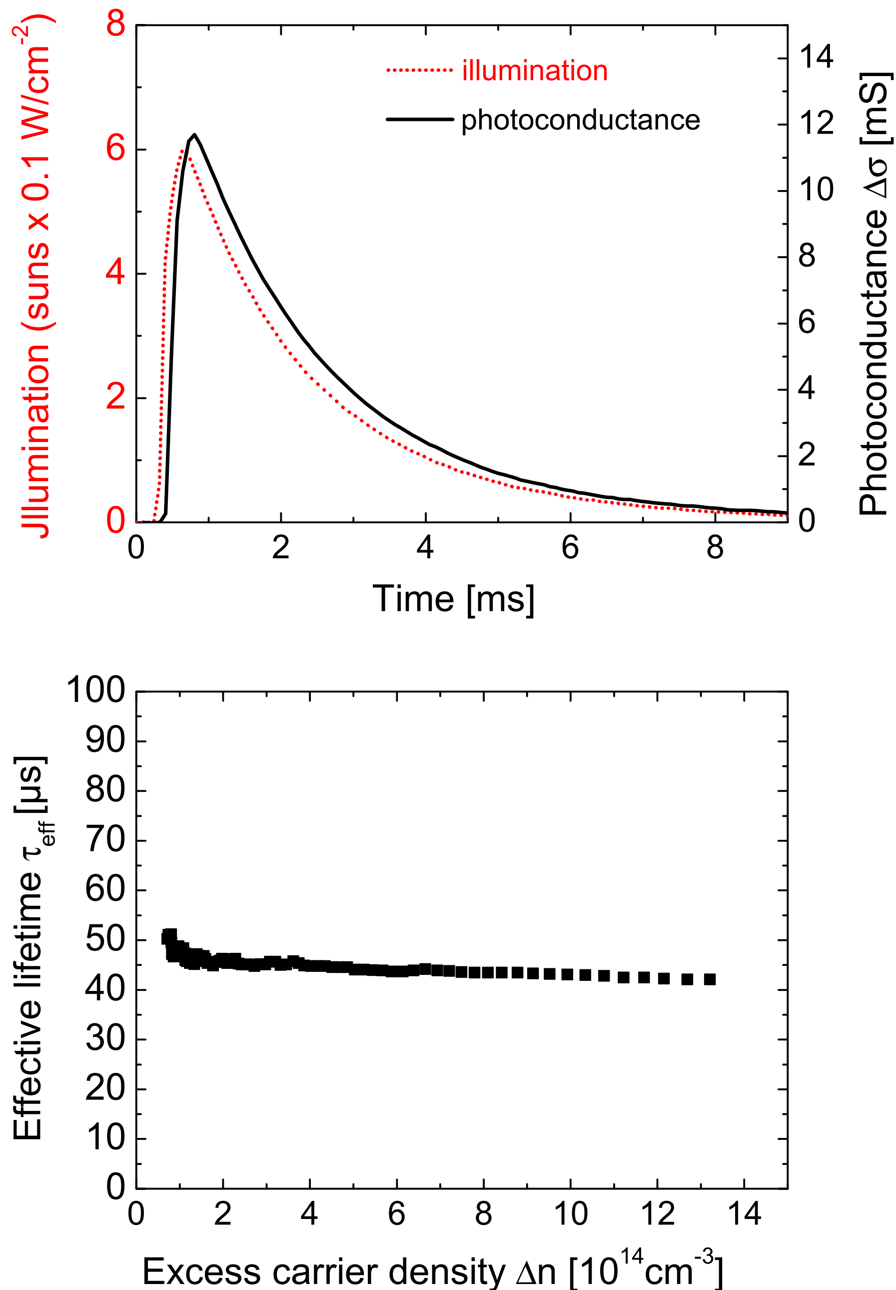

Fig. A.1: A typical QssPC measurement. Photoconductance and illumination are simultaneously measured over time (upper graph) and the effective carrier lifetime is calculated as a function of excess carrier densities (lower graph).

The QssPC method is especially well suited to measure low carrier lifetimes since the carrier statistics then are closest to steady state condition during the flash. In samples with high carrier lifetime (>100 µs for a flash decay of about 2 ms) the

steady-state assumption begins to break down and the analysis becomes more and more invalid.For those very high lifetimes the flash decay time can be reduced to 36 µs and a quasi-transient measurement may be taken. In 1999 Nagel et al. [136] showed that the two limiting cases of “quasi-transient” and “quasi-steady state” are in fact the limiting cases of a more general analysis method. They replaced equation A-2 and A-3 by the general expression

$$\tau_{eff} = \frac{\Delta n_{av}}{G - \frac{d\Delta n_{av}}{dt}} \quad \text{A-5}$$

which is valid for arbitrary generation conditions. This analysis was used throughout this thesis since the whole range of carrier lifetimes could be evaluated with the same algorithm.

Especially for low carrier densities care has to be taken when evaluating lifetime measurements: Trapping artefacts can pretend anomalous high lifetimes. The basic model for trapping was developed by Hornbeck and Haynes [137]. It describes trapping states as an extreme case of SRH recombination in which the cross-section for one type of carrier capture is so small that it is negligible. To maintain charge neutrality $\Delta n + n_T = \Delta p$. The trapped electrons n_T require an additional excess hole concentration since Δn is determined by carrier recombination which operates independently of the traps. The traps essentially remove some of the electrons from the recombination channels, allowing the photo-generated carriers to build up until steady-state is reached [31]. This trapping can be observed in QssPC measurements in the form of extreme rising of the trace when going to lower injection levels (see Fig. A.2).

Trapping is especially pronounced in multicrystalline silicon. This is due to the interaction of impurities with the boron doping atoms [138] and the correlation of trapping and dislocation density [139]. Although there are possibilities to correct the measured values [140], in this thesis the carrier lifetime was usually determined at an injection level of $\Delta n = 1 \cdot 10^{15}$ cm^{-3}. This is sufficiently high to remain unaffected by trapping but still maintain low-level injection conditions ($\Delta n / N_A \leq 0.1$) up to $\rho \approx 1.5$ Ω cm base resistivity material.

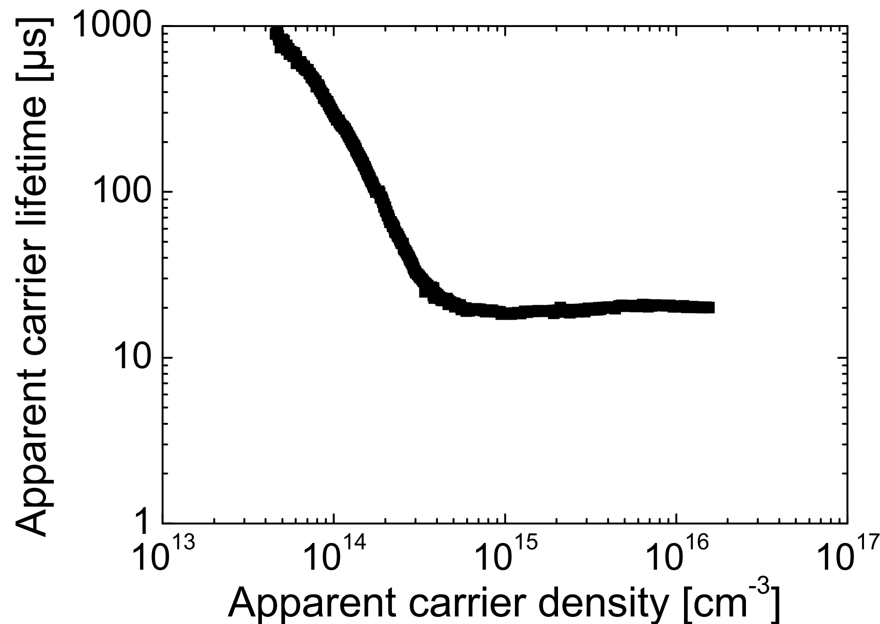

Fig. A.2: QssPC measurement of a multicrystalline silicon wafer. In this particular sample for an injection level below $\Delta n \leq 3 \cdot 10^{14}$ cm^{-3} excessive trapping is observed. The data read out at higher injection levels of $\Delta n \geq 5 \cdot 10^{14}$ cm^{-3} are not affected but still reflect low-level injection conditions.

A.3 Determination of the absorption factor f_{abs}

For an accurate determination of the carrier lifetime in a QssPC measurement, the generation G_L in the sample needs to be known. The generation is determined via a calibrated reference cell measuring the flux of photons N_{ph} which reaches the sample and can potentially generate electron-hole pairs. With the external quantum efficiency of this reference cell and the spectrum of the flash a mismatch-factor f_{mm} of the two spectra can be calculated as follows:

$$f_{mm} = \frac{j_{sc}(AM1.5g)}{j_{sc}(QssPC)} . \quad \text{A-6}$$

This is necessary to account for the significant shift to longer wavelengths in the flash spectrum (see Fig. A.3).

The mismatch-factor allows the determination of the intensity in terms of suns of the AM1.5g spectrum, relevant for solar cells for terrestrial application and used under standard testing conditions. In order to acquire the actual number of electron-hole pairs in the sample, the wafer geometry (surface texture, thickness) and optical properties (antireflection or passivation layers) were simulated with the

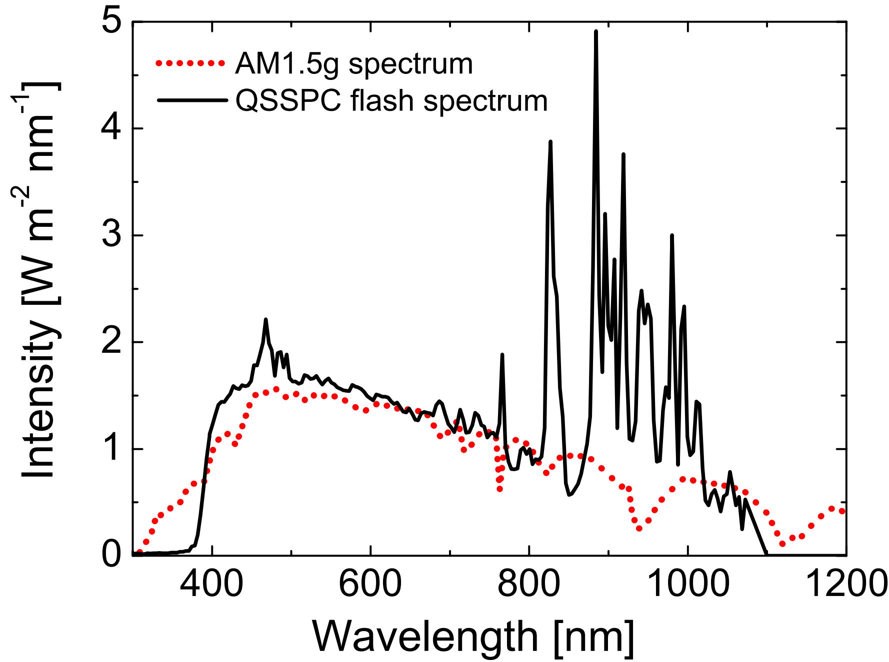

Fig. A.3: Spectrum of AM 1.5g and the QssPC flash.

ray-tracing program Sunrays [141] for the individual wafers which were measured in this thesis.Due to the Monte-Carlo method used in the software, the plot of the resulting data is not smooth and deviates randomly from the mean value. The refractive index, the absorption coefficient and the flash spectrum are taken into account. The generated electron-hole pairs are converted into a current j_{gen} and then normalised to 38 mA/cm^2, a value rather randomly chosen and implemented in the evaluation software. Then the absorption coefficient f_{abs} can be calculated:

$$f_{abs} = \frac{j_{gen}}{38\,mA/cm^2}\,. \qquad \text{A-7}$$

Since a sample with good texture and antireflection-coating can absorb more photons than this “standard” value, even factors in excess of unity are possible (see Fig. A.4). For the antireflection layers a monotonous increase of f_{abs} with thickness is simulated. This also holds true for the passivating silicon nitride layer, but the increment of the curve is significantly steeper for very thin wafers. This leads to a crossing with the curve of the thin thermal oxide. A further evaluation revealed that the reason for this is the increasing absorption in the silicon nitride when the sample thickness decreases (Fig. A.5), a result which highlights the importance of a correct determination of the absorption coefficient, especially for thin wafers (below 100 µm).

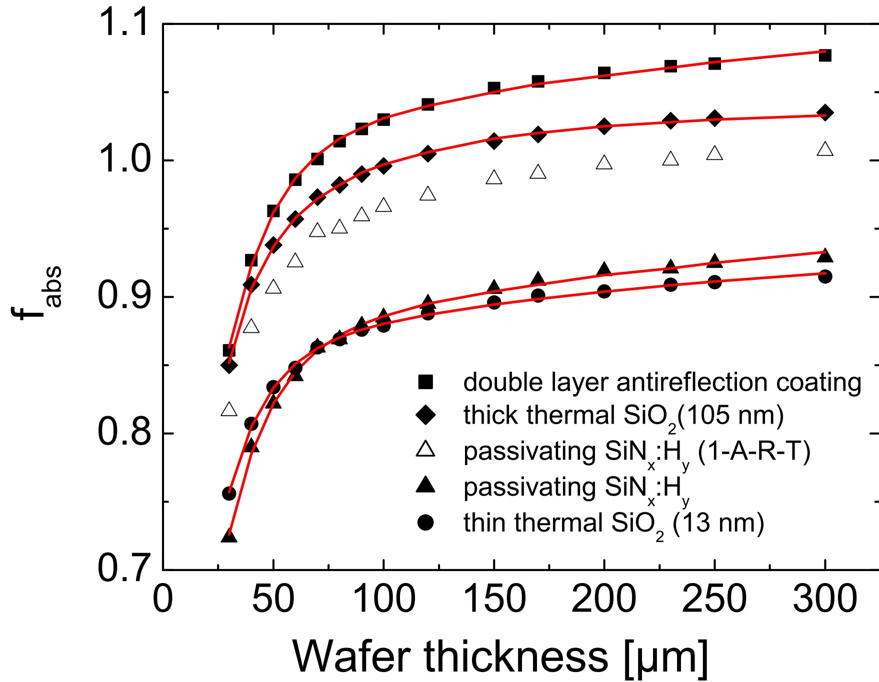

Fig. A.4: Calculated values for f_{abs} for a random pyramid textured wafer for thicknesses of 30-300 µm covered with different dielectric layers. The hollow symbols show the calculation when the parasitic absorption in the silicon nitride layer is (misleadingly) neglected.

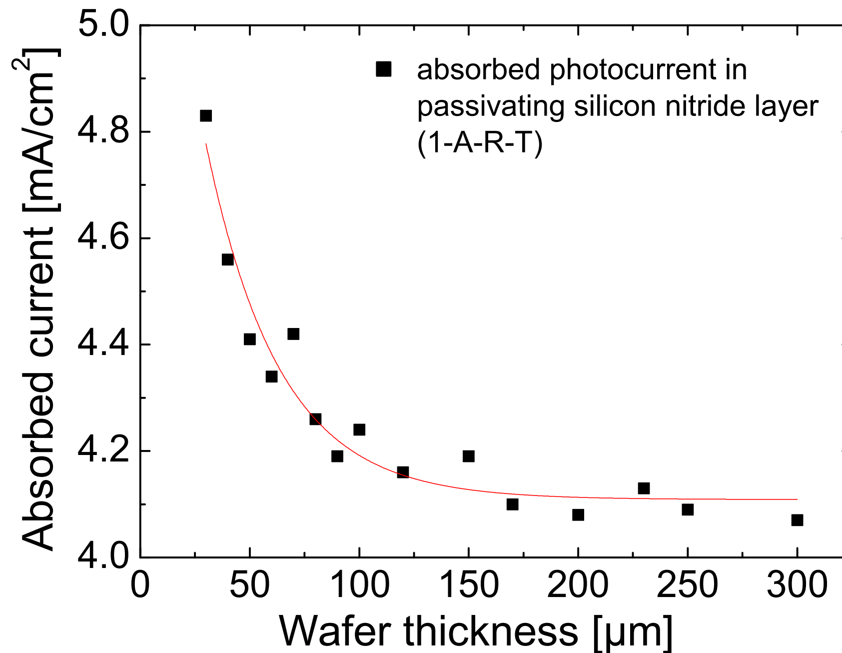

Fig. A.5: The parasitic absorption in the silicon nitride layer A_{layer} is calculated as the difference between unity and the absorption in the silicon, the reflection and the transmission $A_{layer} = (1-A_{Si}-R-T)$. Especially for thin wafers an accurate determination of the absorption coefficient is important. The line is a guide-to-the-eye.

A.4 Carrier Density Imaging (CDI)

Another and more recent measurement technique developed by Isenberg et al. [142,143] and Bail et al. [144] is the Carrier Density Imaging CDI, also called Infrared Lifetime Mapping ILM. The CDI method combines the advantages of high local resolution (which is usually obtained by mapping techniques only) with the benefit of measuring actual (as opposed to differential) lifetimes. These are measured under low-level injection which is the favourable measurement condition since solar cells usually operate in low-level injection, too.

The basic principal used for the lifetime measurements is the capability of free carriers to absorb infrared radiation with photon energies below the bandgap of silicon. An infrared camera measures the transmissivity of the sample in two different stages. In the first stage the sample is illuminated by a source with higher photon energy than the bandgap of silicon and free excess carriers are generated, then the transmissivity is measured without any illumination (Fig. A.6).

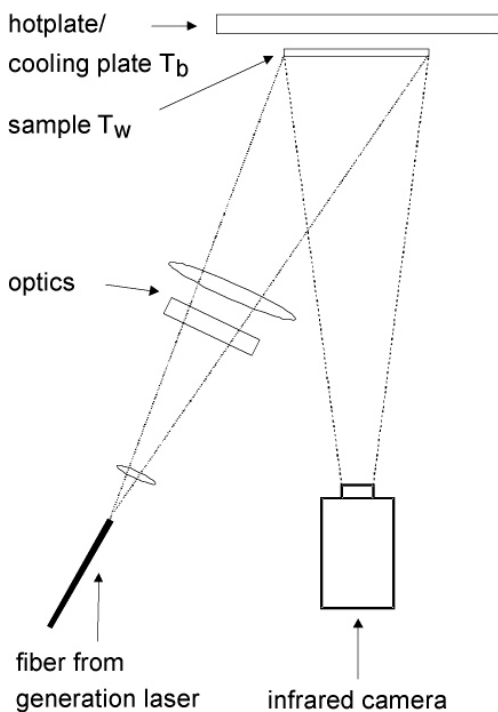

Fig. A.6: Measurement principle of CDI in emission or absorption mode [145].

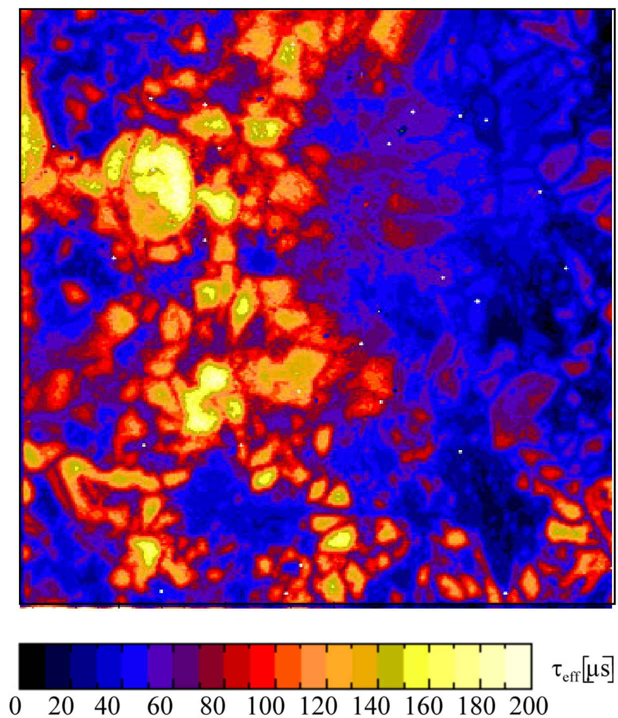

Fig. A.7: Typical CDI measurement of a multi-crystalline silicon wafer. The measured carrier densities are converted to effective carrier lifetimes.

The two transmission images taken by the infrared camera are subtracted from each other and the difference is proportional to the infrared absorption of the free carriers. All other parameters which influence the infrared transmissivity of the sample remain unchanged when the generation illumination is switched on and off. This method is called absorption CDI [142]. In the set-up developed at Fraunhofer ISE, a lock-in system is installed which is fast enough to change between illuminated and dark periods to suppress possible temperature drifts or other changes in the infrared background irradiation. This yields the total amount of free carriers under quasi-steady state conditions in the sample. Together with the generation per area G_L (which is derived from calibration of the illumination source and the optical properties of the sample) the effective lifetime can be calculated according to equation A-3. This is done for every pixel of the 288 ·288 array of the camera and depending on the optical set-up a high spatial resolution of about 350 μm can be obtained for a 10 ·10 cm^2 wafer or 50 μm for a sample area of 1.4 ·1.4 cm^2 (see Fig. A.7).

The complementary process to absorption is emission. In a slightly different set-up the hotplate is exchanged by a cooling plate to reduce infrared emission from the background. Again the carrier densities under illumination and in the dark are measured and the actual lifetime is calculated [145]. Heating of the sample on a plate of very low emissivity (like polished aluminium) is another way to realise suitable measurement conditions where the background radiation is suppressed to a low level in order to prevent superposition of the absorption signal and the signal coming from the wafer.

CDI measurements were used throughout the whole thesis for determination of actual carrier lifetimes of multicrystalline silicon with high spatial resolution.

List of Symbols, Acronyms and Constants

symbol	description	used unit
A	active area of a cell	cm^2
A	aspect ratio	
B	parabolic rate constant for oxidation	$\mu m^2\ h^{-1}$
B/A	linear rate constant for oxidation	$\mu m\ h^{-1}$
c	velocity of light	$cm\ s^{-1}$
C	factor for calculation of iron concentration	$\mu s\ cm^{-3}$
$C_{n,p}$	Auger recombination rate constants	$cm^6 s^{-1}$
d	thickness or distance	μm
$D(\varepsilon)$	density of allowed states	cm^{-3}
D_e	diffusion constant of electrons	$cm^2\ s^{-1}$
D_{it}	density of interface states	$eV^{-1}\ cm^{-2}$
$\Delta\varepsilon$	energy split of quasi-Fermi energy levels	eV
ε_C	energy level of conduction band edge	eV
ε	energy level	eV
ε_F	Fermi- energy level	eV
ε_{FC}	quasi-Fermi energy level of electrons	eV
ε_{FV}	quasi-Fermi energy level of holes	eV
ε_G	bandgap	eV
ε_t	energy level of the defect	eV
ε_V	energy level of valence band edge	eV
f_{abs}	absorption factor for QssPC measurement	
f_{mm}	mismatch factor of AM1.5g and QssPC flash spectrum	

symbol	description	used unit
F	generation rate (per area) during CDI measurement	$cm^{-2}s^{-1}$
φ	electrical potential	V
$F(\varepsilon)$	Fermi-Dirac distribution	
FF	fill factor	
G	generation rate	$cm^{-3}\ s^{-1}$
G_L	light induced generation rate	$cm^{-3}\ s^{-1}$
G_{th}	thermal generation rate	$cm^{-3}\ s^{-1}$
γ	eigenvalue of lifetime evaluation equation	cm^{-1}
Γ	recombination strength of dislocations	
h	height	µm
η	efficiency	%
η_e	electrochemical potential of electrons	eV
η_h	electrochemical potential of holes	eV
I	electric current	mA
I_0	dark saturation current	A
I_{0B}	dark saturation current in the base	A
I_{0E}	emitter dark saturation current	A
I_{SC}	short-circuit current	A
j_e	electrical current density of electrons	$cm^{-2}\ s^{-1}$
j_L	light-induced current density	$A\ cm^{-2}$
j_0	dark saturation current density	$A\ cm^{-2}$
$j_{01,}\ j_{02}$	dark saturation current densities in two-diode-model	$A\ cm^{-2}$
j_{0B}	dark saturation current density in the base	$A\ cm^{-2}$
j_{0E}	emitter dark saturation current density	$A\ cm^{-2}$

symbol	description	used unit
j_{SC}	short-circuit current density	A cm^{-2}
k	Boltzmann's constant	J K^{-1}
L	minority carrier diffusion length	µm
L_e	diffusion length for electrons	µm
L_{eff}	Effective minority carrier diffusion length	µm
L_h	diffusion length for holes	µm
λ	wavelength	nm
m	segregation coefficient	
μ_e	chemical potential of electrons	eV
μ_h	chemical potential of holes	eV
n	density of free electrons	cm^{-3}
n_1,n_2	diode ideality factors	
n	density of free electrons	cm^{-3}
$n^{(n,p)}$	electron density (in *n*-type region or *p*-type region)	cm^{-3}
Δn	excess carrier concentration	cm^{-3}
n_i	intrinsic carrier density	cm^{-3}
n_0	carrier concentration in equilibrium	cm^{-3}
n_S	concentration of electrons at the surface	cm^{-3}
ΔN	excess carrier density per area measured by CDI	cm^{-2}
N_A	concentration of acceptor atoms	cm^{-3}
N_C	effective density of states of conduction band	cm^{-3}
N_D	concentration of donor atoms	cm^{-3}
N_{dis}	dislocation density	cm^{-3}
N_S	concentration of donor atoms at the surface	cm^{-3}

symbol	description	used unit
N_t	density of recombination defects	cm^{-3}
N_V	effective density of states of valence band	cm^{-3}
p	density of free holes	cm^{-3}
$p^{(n,p)}$	hole density (in *n*-type region or *p*-type region)	cm^{-3}
p_0	equilibrium hole concentration	cm^{-3}
p_S	concentration of holes at the surface	cm^{-3}
P	electric power density	mW cm^{-2}
P_{mpp}	electric power density at maximum power point	mW cm^{-2}
$P_{photons}$	incident power density of photons	mW cm^{-2}
q	elementary charge	C
R	recombination rate	cm^{-3} s^{-1}
R_P	shunt (or parallel) resistance	Ω
R_S	series resistance	Ω
R_{sheet}	sheet resistance	Ω/sq
R_{th}	recombination rate compensating thermal generation	cm^{-3} s^{-1}
R_W	weighted reflectance	%
ρ	specific resistivity	Ω cm
S	surface recombination velocity	cm/s
σ_{mc}	standard deviation from mean value for multicrystalline silicon	var.
σ_{FZ}	standard deviation from mean value for FZ-Si silicon	var.
σ_e	conductivity caused by electrons	A V^{-1}m^{-1}
σ_h	conductivity caused by holes	A V^{-1}m^{-1}
σ_n	capture cross section for electrons	cm^2
σ_p	capture cross section for holes	cm^2

symbol	description	used unit
S_{eff}	effective surface recombination velocity	cm s^{-1}
S_{back}	surface recombination velocity on the rear	cm s^{-1}
S_{front}	surface recombination velocity on the front	cm s^{-1}
t	time	h
T	temperature	°C or K
τ	minority carrier lifetime; correction time for short thermal oxidation	µs; h
$1/\tau$	recombination activity	μs^{-1}
τ_{Auger}	minority carrier lifetime of Auger recombination	µs
τ_{bulk}	minority carrier lifetime in the bulk	µs
τ_{eff}	effective minority carrier lifetime	µs
τ_{n0}	fundamental hole lifetime	µs
τ_{p0}	fundamental electron lifetime	µs
τ_{SRH}	Shockley-Read-Hall recombination lifetime	µs
U	net recombination rate	cm^{-3} s^{-1}
U_S	recombination rate at surface	cm^{-2} s^{-1}
U_{SRH}	Net Shockley-Read-Hall recombination rate	cm^{-3} s^{-1}
V	voltage	mV
V_{bi}	built-in potential	mV
V_{MPP}	voltage at maximum power point	mV
V_{OC}	open-circuit voltage	mV
v_{th}	thermal velocity	cm s^{-1}
W	wafer thickness	µm
W_{Basis}	thickness of base	µm
$W_{Emitter}$	thickness of emitter	µm

X	oxide thickness	nm
X_0	initial oxide thickness	nm
x_j	depth of emitter	µm

acronym	description
AM1.5g	**a**ir **m**ass 1.5 global spectrum
CDI	**c**arrier density **i**maging (lifetime measurement technique)
Cz	monocrystalline silicon produced with the **Cz**ochralsky method
DCE	**dic**hloro**e**thylene
EFG	multicrystalline silicon produced with the **e**dge-defined **f**ilm-fed **g**rowth method
EPD	**e**tch **p**it **d**ensity
FZ	monocrystalline silicon produced with the **f**loating **z**one method
IDLS	**i**njection-**d**ependent **l**ifetime **s**pectroscopy
IPA	**i**so**p**ropyl**a**lcohol
LBSF	**l**ocal **b**ack **s**urface **f**ield
LFC	**l**aser-**f**ired **c**ontacts
MW	**m**icro**w**ave
PCD	**p**hoto**c**onductance **d**ecay (lifetime measurement technique)
PECVD	**p**lasma **e**nhanced **c**hemical **v**apour **d**eposition
PERC	**p**assivated **e**mitter and **r**ear **c**ell (solar cell structure)
PERL	**p**assivated **e**mitter **r**ear **l**ocally-diffused (solar cell structure)
PSG	**p**hosphorus **s**ilicate **g**lass
QE	**q**uantum **e**fficiency
QssPC	**q**uasi-**s**teady **s**tate **p**hoto**c**onductance (lifetime measurement technique)

acronym	description
RIE	**r**eactive **i**on **e**tching
RPHP	**r**emote **p**lasma **h**ydrogen **p**assivation
SEM	**s**canning **e**lectron **m**icroscope
SIMS	**s**econdary **i**on **m**ass **s**pectroscopy
SR	multicrystalline silicon produced with the **S**tring **R**ibbon method

constant	description	value
c	velocity of light	$299792458\ \mathrm{m\ s^{-1}}$
h	Planck's constant	$6.62608 \cdot 10^{-34}\ \mathrm{J\ s}$
k	Boltzmann's constant	$1.3806 \cdot 10^{-23}\ \mathrm{J\ K^{-1}}$
q	elementary charge	$1.602 \cdot 10^{-19}\ \mathrm{C}$
n_i	intrinsic carrier density	$1.00 \cdot 10^{10}\ \mathrm{cm^{-3}}$
N_C	effective density of states of conduction band	$2.84 \cdot 10^{19}\ \mathrm{cm^{-3}}$
N_V	effective density of states of valence band	$2.68 \cdot 10^{19}\ \mathrm{cm^{-3}}$

List of Publications

1 D. Biro, O. Schultz, R. Preu, C. Ballif, D. Zickermann, and R. Lüdemann, *Screen printed selective emitters prepared by fast and rapid thermal diffusion*, Proceedings of the 17th European Photovoltaic Solar Energy Conference, Munich, Germany, p. 1593-6 (2001)

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