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NEAR 13% EFFICIENCY SHUNT FREE SOLAR CELLS ON RGS WAFERS

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ABSTRACT

Direct casting of silicon into wafers allows to produce wafers much more cheaply than in traditional block casting methods. RGS (Ribbon Growth on Substrate) is such a method. In order for RGS to be cost effective sufficient cell efficiencies must be realized.

In this paper we present a 12.9% efficient screen printed RGS cell. This is an increase of 0.6% absolute compared to the best previous result reported in January 2005. The increase was achieved by reducing shunting in cells made on RGS material.

THE RGS PROCESS

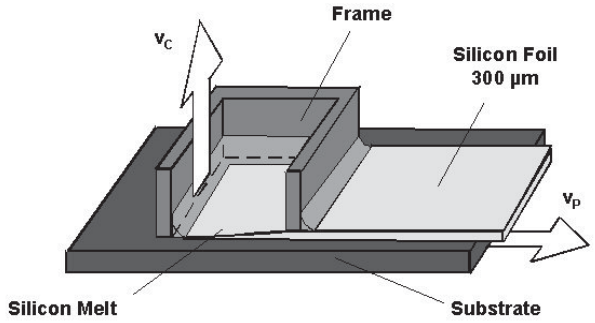

Figure 1: Principle of the RGS process. The crystallisation speed V_C is decoupled from the pulling speed V_P.

In the RGS (Ribbon Growth on Substrate) technology [1] wafers are cast directly on moving substrates. The principle is illustrated in Figure 1. Substrates move under a crucible containing molten silicon at a pulling speed V_P. The silicon crystallizes in a direction perpendicular to the direction of the moving substrates at a rate V_C. In this way the crystallization speed is decoupled from the pulling speed. Wafers are produced with a high throughput while maintaining a slow growth rate. This principle allows much faster manufacturing of wafers compared to other ribbon technologies such as EFG (Edge defined Film-Fed Growth) [2] and String Ribbon [3]. The RGS process can produce wafers at a rate of 1 wafer/second.

By direct casting the technology avoids kerf losses that occur during sawing of wafers from ingots. With the RGS technology the available silicon feedstock can be used much more effectively and wafers can be produced at a rate that is compatible with current processing speeds for silicon cell technology.

STANDARD PROCESS ON RGS

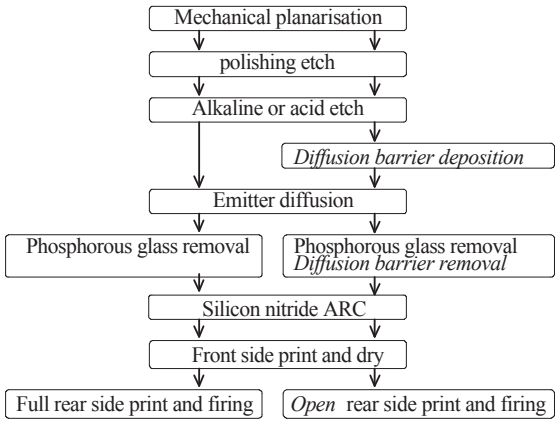

Figure 2: Standard process (left hand side) and RGS shunt free process (right hand side).

At ECN we aim to develop a process for RGS that is compatible with current industrial processes for multi-crystalline silicon. We therefore apply a basic screen printing process to the RGS wafers. The process sequence is depicted on the left hand side of Figure 2. After the mechanical planarisation step and polishing etch the process starts with an alkaline (non-texturing) etch or an acid texturing etch. Subsequently we have a doubly sided phosphorous diffusion, a PECVD silicon nitride AR coating, a front side silver print and a full rear side alloyed aluminum metallisation serving both as rear contact and back surface field (BSF). The phosphorous diffusion results in a 50 Ω/□ emitter. Front- and rear side metallisation are cofired in a single firing step.

During the phosphorous diffusion impurities present in the material are gettered. On the rear side the phosphorous doping is compensated during the aluminum alloying process that takes place during the cofiring. Also during the cofiring the hydrogen present in the Si_xN_y:H AR coating diffuses into the wafer and passivates crystal defects and impurities resulting in an increased minority carrier diffusion length. No additional hydrogen passivation step is used and also unnecessary with the current RGS material [4]. When applying this process to RGS wafers we find that some of the RGS cells are shunted, whereas multi-crystalline silicon references are shunt free.

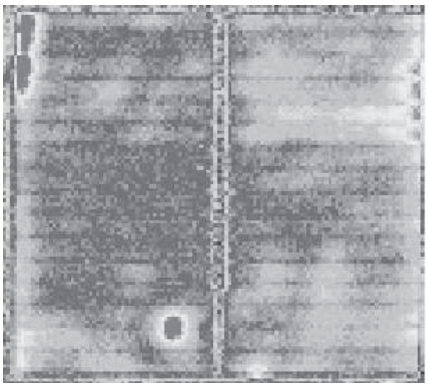

Figure 3 Shunt scan of RGS cells with standard process.

In Figure 3 a thermography scan (iLIT) of a shunted RGS wafer is shown. We observe areas of shunting (lighter colours), edge shunts (top left) and point shunts (lower half, slightly left of the centre). This pattern of shunting is comparable to what is observed by Seren et al. [4].

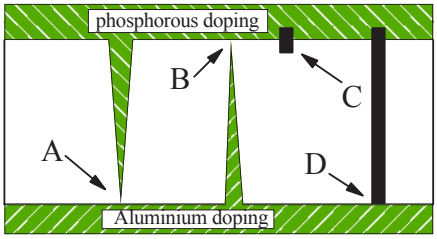

Figure 4: Cross-section of a p-type RGS silicon wafer showing four possible shunting mechanisms.

In Figure 4 four possible shunt mechanisms are shown. The shunting may be related to the phosphorous diffusion process (arrow A). It is known that phosphorous diffusion is faster along grain boundaries. The shunting may also be related to the diffusion process. Holloway et al. [5] observed diffusion up to 10 µm depth in multi-crystalline silicon wafers along the grain boundaries. The RGS wafers have crystal sizes of typically 100-500 µm. Hence compared to multi-crystalline silicon wafers there are many more grain boundaries. From a statistical point of view this means that even if very deep diffusions along grain boundaries are rare, they are more likely to occur in RGS wafers because of the high total length of grain boundaries. Deep diffusion along the grain boundaries might lead to the formation of n-type shunt paths.

Arrow B indicates shunting because aluminium possibly alloys through the wafer, maybe because of micro-cracks. Arrow C indicates shunting of the junction that might be caused by e.g. SiC precipitates. This mechanism has been suggested by Seren [4]. If there is some other shunting path (arrow D), it may be contacted by the full rear side aluminium metallisation. One mechanism that has been suggested to explain shunting on RGS material involves so called current collecting channels [6].

OPEN REAR SIDE PROCESS ON RGS

In order to eliminate the shunting we developed an alternative process. The main idea in this shunt-free process is to use an open rear side metallisation using an H-grid pattern.

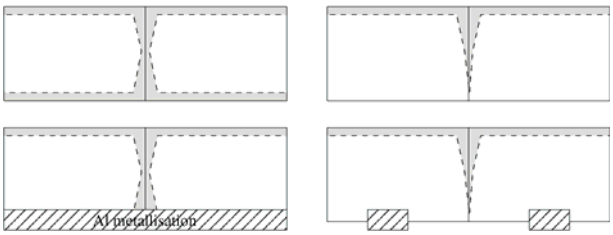

Figure 5: Shunt formation mechanism because of phosphorous diffusion. The left hand side applies to the standard process, the right hand side to the shunt free process. Top row is after phosphorous diffusion, bottom row after alloying the rear side metallisation.

In Figure 5 we show how the open rear side process can reduce phosphorous diffusion shunts -- if they are the cause of shunting. In the standard process the phosphorous is diffused from both sides of the wafer. On the front side the phosphorous diffusion forms the emitter. On the rear side the diffusion is compensated during the aluminum alloying process. If the diffusion extends through the wafer, a shunt may be formed at the intersection of the aluminum metallisation and the phosphorous diffusion. In the shunt free process illustrated on the right hand side we reduce the probability of a deep diffusion and even if shunt paths are formed we have less risk of contacting them because of the open rear side metallisation.

In general when we use an open rear side metallisation we have a lower probability of creating a shunt path. Secondly, even if a possible shunt path is created, it is less likely to contact it with an open rear side metallisation. If we use an open rear side metallisation, a single side diffusion must be applied because electrical contact between a phosphorous diffusion at the rear side and the aluminum metallisation at the rear would lead to problems.

In Figure 2 the two process sequences are compared. Before emitter diffusion we have an additional step in which we deposit a silicon nitride diffusion barrier. The diffusion barrier is deposited at the future rear side of the cell and is an extra safeguard to make sure we get a single side diffusion. After the emitter diffusion, the diffusion barrier can be removed without an additional process step because the diffusion barrier removal can be combined with the phosphorous glass removal in concentrated HF. The open rear side pattern is no problem since for the processing it makes no difference

whether we print a full rear side pattern or an open rear side pattern.

RESULTS

Table 1: Cell parameters of cells with standard and shunt free process. In brackets the standard deviation in the parameters is shown.

process	η (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF(%)
standard	9.8 (0.9)	27.6 (0.7)	556 (7)	63.4 (6)
shunt free	11.9 (0.4)	27.6 (0.2)	582 (2)	72.7 (2)
shunt free (mc-Si ref)	13.4 (0.2)	31.0 (0.2)	590 (1)	72.8 (2)

Table 1 shows cell parameters for the two different processes on RGS wafers. The fill factor of the shunt free process is much better and shows a much smaller standard deviation. This is reflected in the cell efficiencies. The difference in V_{oc} in these runs is caused by different casting conditions.

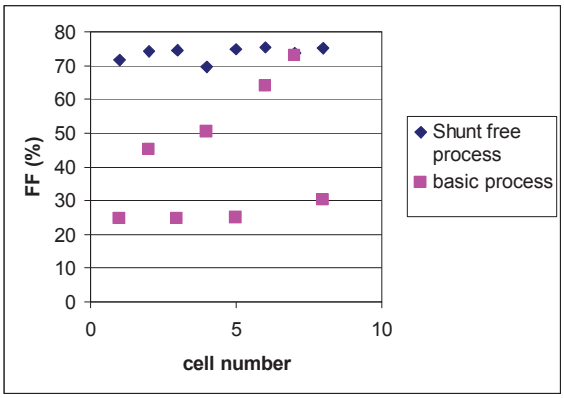

Figure 6: Fill factors for the basic process and the shunt free open rear side process.

Figure 6 shows individual fill factors for the two different processes on RGS wafers. The fill factor of the shunt free process is much better and shows a much smaller standard deviation. Taking into account observations on other experiments as well we are convinced that the shunt free process results in good shunt resistances and small spread in cell parameters.

Table 2: I-V results for individual cells.

cell	I_{sc} (mA)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	η(%)
377-4A	635	28.1	590	75.5	12.5
377-4B	658	29.1	590	74.6	12.8
377-5A	627	27.8	585	75.2	12.2
377-5B	647	28.6	586	74.1	12.4
383-5A	658	28.6	589	76.3	12.9

Table 2 shows the I-V results for different cells. The four cells marked 377 are alkaline etched (non-textured) cells. The cells received an additional MgF_2 coating to make a double layer ARC (DLARC). The I-V results on the 377 series of cells have been independently confirmed by the ESTI lab of the EC Joint Research Centre, Ispra, Italy.

The more recent cell marked 383 had an acid texture etch instead of an alkaline etch. No additional MgF_2 coating was applied. These are the best results obtained with a screen-printed process on RGS wafers to date and present a 0.6% absolute improvement over the results presented by Seren [4].

Figure 7: Shunt scan of a RGS cell with new process

In Figure 7 a shunt scan is shown of a RGS cell made with this process. No shunting is observed nor measurable in the I-V curve.

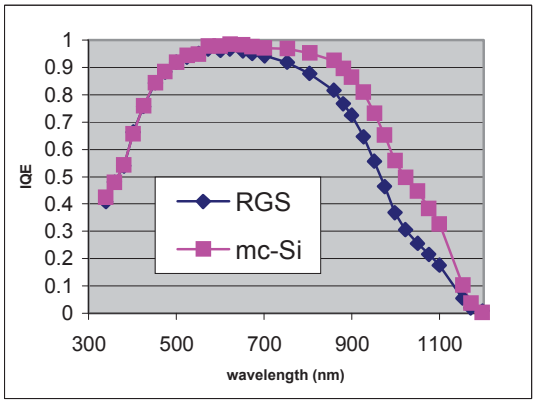

Figure 8: IQE of a RGS and a multi-crystalline cell.

In Figure 8 we compare the IQE of cells made on RGS and multi-crystalline silicon with the same open rear side process. From the lower IQE for the long wavelength light it is clear that the diffusion length for minority carriers in the bulk of the wafers is significantly shorter than on multi-crystalline silicon material. For RGS material we inferred from analysis of the spectral response a bulk diffusion length of about 100 μm. The short current density

of the RGS cells obviously is smaller than on multi-crystalline silicon references because of the smaller minority carrier diffusion length. Because the diffusion length is smaller than the wafer thickness, the absence of a BSF is not affecting efficiencies on RGS material adversely, though it does on multi-crystalline silicon references.

DISCUSSION AND OUTLOOK

Shunt free cells can consistently be made on RGS material with a process using a single side phosphorous diffusion and an open rear side metallisation. It is not clear at this point whether we avoid contacting shunts in the wafer with the open rear side metallisation or whether we avoid forming those shunts with either the single side phosphorous diffusion or the partial rear side aluminum metallisation. Since we have shunt free cells with a single side emitter it seems unlikely that the junction itself is shunted, e.g. by SiC precipitates.

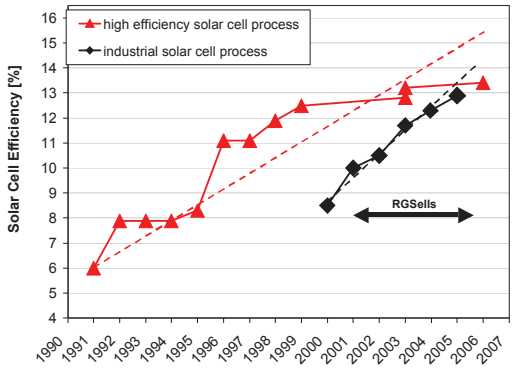

Figure 9: Efficiency development on RGS material since 1991.

In Figure 9 the history of efficiency development on RGS material can be seen. One curve represents the high efficiency solar cell process that has been applied mainly at the University of Konstanz. The second curve shows the development of the cell efficiency in the industrial process. This development has taken place at both ECN and the University of Konstanz and since 2002 within the framework of the EU co-funded RGSells project.

Due to improvement of the cast material and the processing experience we gained on the RGS material within the RGSells project we have been able to realise a spectacular improvement in efficiency with the screen printed process.

The main obstacle in improving cell efficiency with the current combination of material and processing is the limited bulk minority carrier diffusion length in the RGS material. By combining improvements in the casting process and the processing we aim to improve the bulk minority carrier diffusion length.

We aim to improve the blue reponse of the cells as well. ECN has a high efficiency process [7] for multi-crystalline silicon wafers using industrially viable process methods. This process results in higher efficiencies than the basic process we used so far. The improvement results from the combination of texturing by acid etching, a high resistivity 70 Ω/□ emitter and tuning the process. This process must be transferred to the RGS material.

In the current open rear side process we have no rear side passivation. Because of the limited diffusion length in the RGS material this is not a problem at the moment. In the future we hope to implement one of the rear side passivation schemes (e.g. based on SiC or SiN_x:H coatings) that are currently being developed for multi-crystalline silicon material.

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