Proceedings of the

2nd Workshop on Metallization for Crystalline Silicon Solar Cells

– Status, trends and new directions –

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FOREWORD

Gunnar Schubert, Jaap Hoornstra, Guy Beaucarne

Metallization is one of the key process steps to fabricate solar cells with high performance in a cost-effective way. More than 85% of the photovoltaic solar cell manufacturing uses thick film screen print metallization to produce solar cells, but a lot of research is also carried out on alternative metallization schemes and/or variations to screen-printing. The success of metallization technology development is crucial for the evolution of solar cell technology towards lower production costs and higher efficiencies.

Recognizing that existing photovoltaic events did not provide an ideal setting for experts to discuss these topics in detail, we decided to organize a dedicated and focused workshop on the topic of metallization of crystalline Si solar cells. The number of participants to this workshop is limited and much time is reserved for panel discussions, informal exchanges and networking.

The first Metallization Workshop held in Utrecht, The Netherlands, in 2008, turned out to be a great success, according to the participants (www.ipcrystalclear.info/events/agenda-and-slides.aspx).

The second edition was held in Constance, Germany on 14th and 15th of April 2010 (www.secondmetal.eu). Around 190 scientists and engineers from solar energy institutes, universities, and companies all over the world gathered in the "Konzil", a historical building facing the Lake of Constance, to share and discuss the latest developments in solar cell metallization. It was a very successful workshop, with outstanding talks and great discussions.

In this volume, selected contributions to the Second Metallization Workshop are published in scientific article form, enabling readers to obtain detailed information about specific contributions and to give proper reference to them. The articles were peer-reviewed by the members of the scientific committee of the workshop, consisting of well known and established experts in the field of metallization for crystalline silicon solar cell.
As you will read in these proceedings, the Second Workshop on Metallization of Crystalline Silicon Solar Cells provided excellent insights in the status and development of metallization technology. Although screen-printing has been around for a long time, it is efficient, quick and reliable, and its performance is being stretched by recent innovations, making it hard for alternative techniques to emerge. The hybrid Ag seed and plate approach is the only technique that could be introduced in the short term, but has lost some of its appeal because of improvements in traditional screen-printing. Metallization schemes based on Cu plating appear the ultimate solution in terms of line width, cell performance and material costs, but several hurdles need to be overcome before it can be widely adopted.

At the end of the workshop, the participants were requested to give their views on the development of metallization in a questionnaire. The results showed that screen-printing is expected to remain dominant in the next 10 years, but that emerging concepts will gain significant share within five years (see Figure 1 below). Comparing these results with the results of the first metallization workshop it is worth to have a detailed look on the expected shares in 2013. Screen-printing is seen to dominate longer than two years ago expected. The importance of the hybrid approach has decreased (Figure 2). More results of the questionnaire can be found on our homepage.

We would like to thank all the people who made the workshop possible, in particular our sponsors, all the members of the organizing team, the scientific committee and the contributors.

Gunnar Schubert (Sunways), Jaap Hoornstra (ECN) and Guy Beaucarne (Dow Corning)

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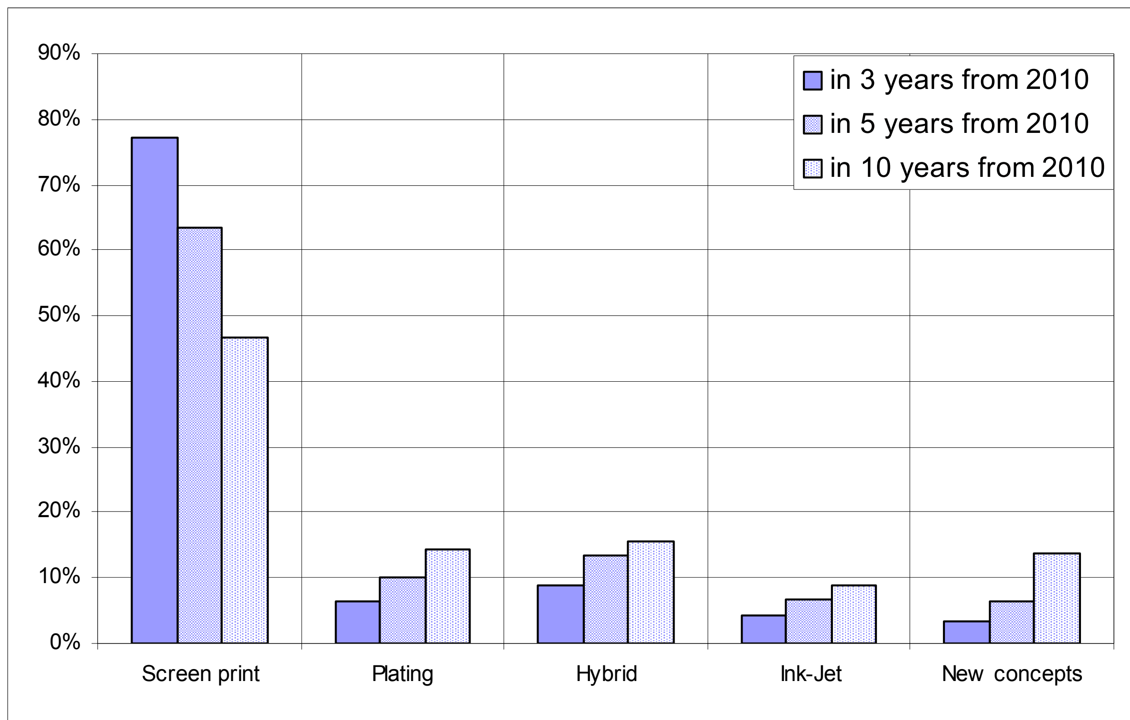

Figure 1: Anticipated share of the different metallization techniques in the coming years

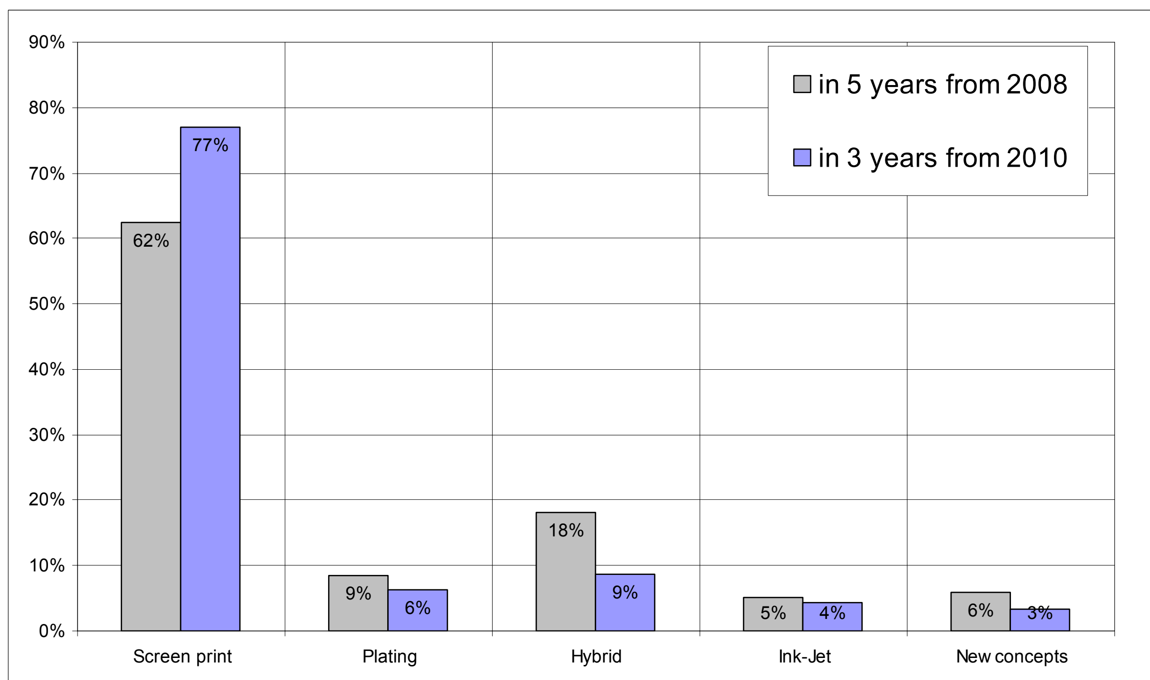

Figure 2: Comparison of anticipated share of different metallization techniques in 2013.

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FUNDAMENTAL REACTIONS DURING THE FORMATION OF FIRED SILVER CONTACTS AND SOLAR CELL RESULTS

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ABSTRACT: The contact formation on high efficiency solar cells using a high temperature process is the subject of this research. Thermal gravimetric analyses were used to study the chemical reactions between ink components and solar cell during the firing process. The mechanism behind the etching process and the opening of the dielectric layer are explained and the influence of the glass concentration on the contact quality is given. Based on these studies, a seed layer ink was developed, optimized and tested on silicon solar cells. The developed ink was applied on high efficiency solar cells with printed and fired front contacts and compared with photolithographically defined and evaporated front contacts. At the rear side, we used a firing stable passivation layer consisting of Al_2O_3 and SiO_x. After evaporation of aluminum and applying laser fired contacts at the rear and light induced silver plating at the front, cell efficiencies of $\eta = 21.5\%$ and fill factors of 81% could be measured.

1 INTRODUCTION

The main challenge for all printing technologies is to achieve finer metal lines with high lateral conductivity and excellent contact properties. This can be achieved by fine line printed and successively light induced plated contacts [1, 2]. The two layer approach has the advantage that expensive silver inks/pastes are only used as a seed layer and less expensive copper is used to build up the contact. The contact formation for a seed layer is more ore less the same as for a full printed contact, the contact materials are fired through the anti-reflection coating and a contact between emitter and front side grid is formed. The high temperatures are necessary to open the ARC and to support the reaction between contact ink and the silicon. Thus, the firing step is the most crucial part for the contact formation and thus for the ink development. In addition to investigation by other authors [3, 4] we have studied the chemical reactions occurring during the firing process between the ink components and the solar cell on a more fundamental level. The reactions are investigated by differential-thermo gravimetric analysis, bringing ink ingredients like lead oxide, bismuth oxide, glass frit, and silver in reaction with silicon and silicon nitride. The results were used to develop a seed layer ink which, first of all, allows the formation of a low ohmic contact on a lowly doped emitter in order to reduce the recombination losses and to increase the blue response and thus the efficiency potential of a solar cell. Additionally, the shading needs to be reduced by optimizing the front side grid, especially by using fine line printed contacts in combination with plating. The seed ink, developed at Fraunhofer ISE – which is called SISC (**s**eed layer **i**nk for the metallization of **s**olar **c**ells) - was already tested on emitters with a sheet resistivity up to $R_{SH} = 130\ \Omega/\text{sq.}$ [5] and successfully applied on a high efficiency solar cell where cell results up to $\eta = 20.3\%$ were achieved [2]. In this paper we present the fundamental investigations upon which the ink development is based. Additionally, we combined our optimized front side, emitter and metal grid, with an advanced rear side passivation. The rear side dielectric in this cell concept needs to meet two demands. The passivation should resist high temperatures; the solar cell is exposed during the firing step. It could be demonstrated that a stack system of ALD-Al_2O_3 and SiO_x is not influenced by a firing step and keeps its passivation quality. Results with passivated and full printed solar cells are presented elsewhere [6].

2 EXPERIMENTAL

2.1 Thermo-gravimetric differential thermal analysis

Thermo-gravimetric differential thermal analysis (TG-DTA), see Fig. 1, was used to study the reaction mechanism behind the front-contact formation in a firing step.

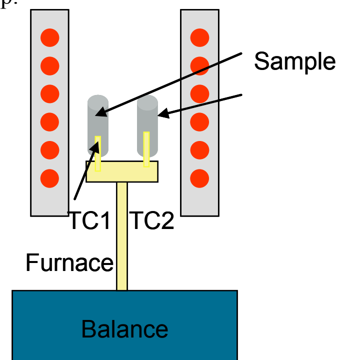


Figure 1: Setup for the differential thermo analysis (DTA).

The TG-DTA uses the temperature difference between the sample and a reference during a controlled-temperature program. A DTA sample holder consists of two ceramic cups, each connected to a thermocouple (TC1, TC2). The sample holder is placed in a furnace on a sensitive balance. During the controlled-temperature program, the measured temperature of the reference, usually an empty cup and the sample can be different, which is dependent on the chemical reactions or phase changes of the studied samples. It can distinguish between exothermic reactions, where additional reaction heat is produced (such as due to condensation energy), and endothermic reactions, where reaction heat is ‘‘consumed’’ (such as during melting). The difference in the thermal voltage, as measured by the thermocouples, is plotted as a function of time, which reflects the time-dependent temperature evolution. In addition the mass

signal is monitored. The offset in all DTA-signals during changes in the temperature profile are related to different thermal masses of sample and reference and can be neglected. In our experiments we used a TG-DTA from Netzsch STA 409C, an alumina sample holder, and type-S thermocouples. All reactions were studied using Ag-, Si-, PbO- and glass powders which were placed in the crucible on top of each other, e.g. PbO on top of Si-powder.
After one temperature cycle, the resulting products were analyzed using SEM-images and EDX-analysis.

2.2 Ink preparation

The silver based ink was manufactured using spherical silver powder with a size distribution of below 1 µm and a glass system based on a leaded glass frit. The fritted glass was milled in a ball mill until the particle size was also reduced below 1 µm. The solid ingredients are than mixed with a solvent system based on glycol ethers and homogenized on a three mill chair, see Fig.2. The ink is than treated for 5 min with an ultrasonic horn in order break up remaining agglomerated. The viscosity consequently drops to values below η_{vis} = 1 Pas (measured at a sheer rate of 1/s, with a cone – plate geometry) and the resulting ink can directly be used for printing in our case for aerosol printing.

Figure 2: Three roll mill on which an ink is homogenized by successively reducing the distance between the single rolls.

2.3 Solar Cell structures

The used cell structure is shown in Fig. 3. We used 0.5 Ωcm p-doped FZ-base material. The front side has a shallow emitter with a sheet resistance of R_{SH} = 110 Ω/sq. on a randomly textured surface, which was passivated with a PECVD-nitride layer. The front side grid was jet printed with our homemade Ag seed layer ink. The ink consists of silver particles with a size distribution below 1 µm and a glass system based on lead oxide glass [7]. The printed seed layers, featuring a width of w_c = 25 µm, were subsequently fired in an RTP-furnace. The seed contacts were then further subject to light induced silver plating, resulting in a total finger width of w_f = 45 µm. The optimum finger distance was calculated using the simulation tool Gridsim to d = 1.3 mm [8]. The rear side is passivated by a layer of 10 nm atomic layer deposited (ALD) Al_2O_3 covered with a layer of 90nm PECVD SiO_2, metalized by thermal high rate deposition of aluminum [8] followed by LFC-contacts. The reference sample has the same solar cell structure apart from the front side which is photolithographically structured and metalized by the evaporation of Ti-Pd-Ag.

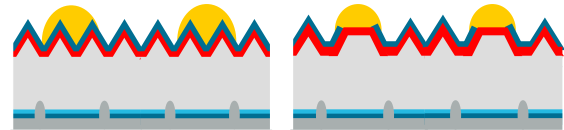


Figure 3: Schematic of the used solar cell structure, printed, fried and plated contacts (left) and evaporated and plated contacts (right)

3 BASIC REACTIONS BETWEEN INK COMPONENTS AND SILICON

Inks or pastes for the front side metallization of silicon solar cells consists besides organic components of silver particles as a conductive metal and a glass frit based on lead oxide or bismuth oxide. The glass frit opens the anti reflection coating, reacts with silicon and is responsible for the actual contact formation. To study the reaction between ink components and the solar cell, we simplified the ink by using only Lead (II) oxide (PbO) powder (representing the glass frit) or the combination with silver powder (representing the silver ink). For a more distinct DTA-Signal the Si-wafer was milled to Si-powder. The reactive component in an Ag paste is the glass frit, in particular the lead oxide or bismuth oxide, incorporated in a glass matrix (glass frit). The idea to transfer the reactive oxides into a glass frit, instead of using the oxide directly, has several advantages. The glass melts at a lower temperature than the pure oxide, wetting the entire contact area homogenously, and the reactive oxide is brought in close contact with the wafer surface. In Fig. 4 the DTA measurement between lead oxide (PbO) and silicon shows a significant peak at 650°C. The reaction between silicon and the oxide is an abrupt exothermal reaction, which would not be easy to control during the fast firing step of a solar cell. However, if a glass frit is used, there is not a sharp peak in the DTA-signal. Instead the exothermic redox reaction given in Eq.1 occurs over a broad temperature range, between 520°C and 760°C. This allows for better control during the fast firing contact formation step. That is the main reasons why lead or bismuth oxides are incorporated into a glass frit. The redox reaction is moderated and the process window for contact firing is increased.

Fig. 6 (top) shows the reaction products after thermal treatment. During the redox reaction (1) the glass frit, or more correctly its reactive components like lead oxide (PbO), is reduced to elemental lead and at the same time silicon is oxidized. Lead precipitates, embedded in glass and not reacted Si-particles are visible. The oxidized silicon is solved in the liquid glass phase (for the reaction glass frit + Si) or it forms a leaded glass (for the reaction PbO + Si). This means for a real contact the formation of glass during contact firing. The formed glass is usually present at the contact interface as an isolating layer[9, 10]. Additional glass is formed during the opening of the antireflection or passivation layer. The reaction mechanism between SiN_x and the glass frit (Eq.2) is similar to (1). With other words, a glass frit (lead oxide) is necessary to promote the contact formation, but too much of it is detrimental to the electrical contact, more details are given in [11].

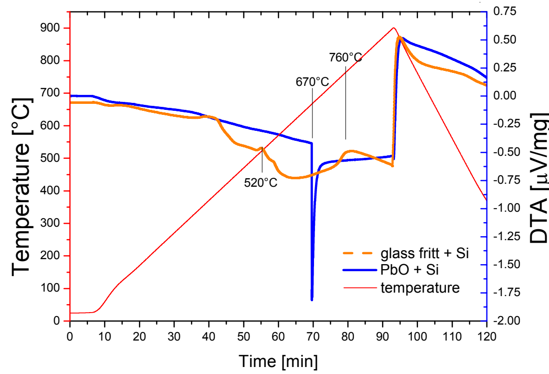
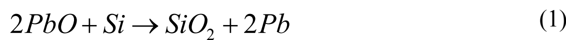
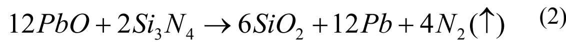


Figure 4: Reaction between silicon and lead oxide and glass frit and silicon. The temperature profile and the two DTA-signals are shown.



$$2PbO + Si \rightarrow SiO_2 + 2Pb \qquad (1)$$



$$12PbO + 2Si_3N_4 \rightarrow 6SiO_2 + 12Pb + 4N_2(\uparrow) \qquad (2)$$

In a further experiment, silver is added and the reaction of the simplest contact ink (silver and lead oxide) with silicon is studied. The DTA signal is similar to the one shown in Fig. 4 apart from the cooling sequence, see Fig. 5. During cooling, two further exothermic peaks are visible, at $T = 300°C$ and at $T = 600°C$. Corresponding phases can be found in the Ag-Pb phase diagram. After cooling, the reaction products are analyzed by SEM images and EDX. The products in the crucible are separated into two phases, a silicon-glass phase Fig. 6 (top) and a metal phase shown in Fig. 6 (bottom). The metal phase consists of an Ag-rich and a Pb-rich phase. It is noticeable that all the silver has been molten even if the temperature was kept below the melting point of silver and below the silver-silicon eutectic. The silver rich phase re-crystallizes in the form of silver crystallites, which are interconnected with the lead-rich Ag-Pb eutectic. The EDX analysis of the reaction products is in good agreement with the expected Ag-Pb phase according to the Ag-Pb phase diagram. For the silver-rich phase, a content of 98.1at% Ag is found and for the Pb-rich eutectic, a composition of Ag:Pb of 3.9:96.1at%.

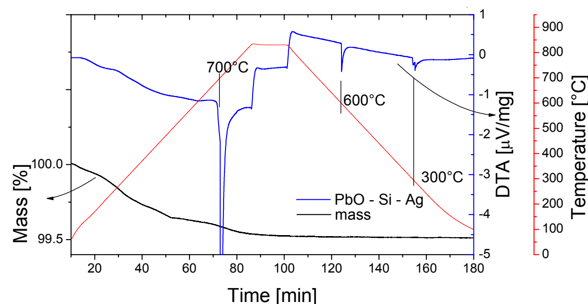


Figure 5: DTA-signal for the reaction between PbO, Si, Ag during cooling. The two peaks during cooling are characteristic for condensation of silver, lead alloy.

The silicon-glass phase, see Fig. 6 (top) is characterized by silicon particles embedded in a glass matrix. A layer of small metal precipitates is found in the glass layer, especially in the vicinity of silicon particles; quite large Ag-Pb precipitates are additionally homogenously distributed over the glass phase. Glass close to silicon particles has a low lead content and increased silicon content, whereas glass distant from Si-particles contains a higher lead content. During the redox reaction, silicon is oxidized to silicon dioxide, which is incorporated into the already existing glass layer (increased Si content). At the same time, lead oxide is reduced to lead and forms an Ag-Pb phase. The Ag-Pb melt condenses in the form of silver crystallites and as a lead-silver eutectic.

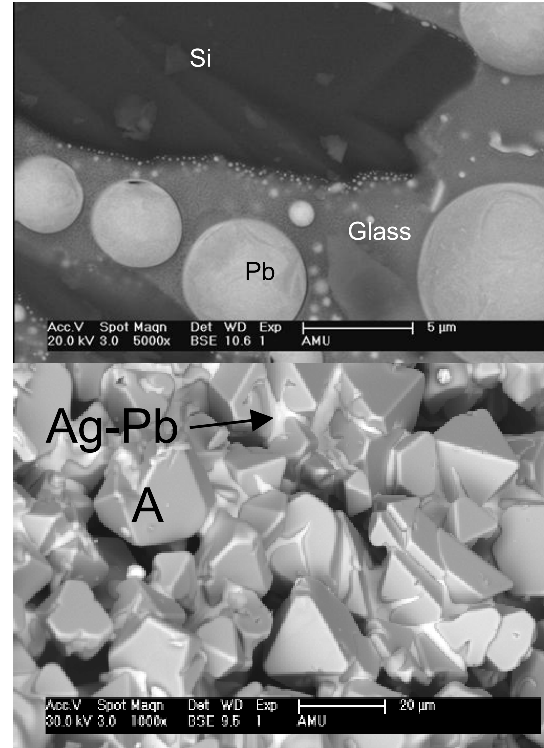


Figure 6: SEM images of the reaction products after thermal treatment of the reaction participants: PbO, Si, Ag). The reaction products are separated in two phases; (top) silicon-glass phase and (bottom) Ag-Pb phase.

The reaction and therefore the contact formation can be influenced by process parameters like temperature, time, amount of reactive oxides (glass), and the process atmosphere. All these parameters influencing the trade off between glass layer thickness and density of Ag-crystallites. For example the higher the firing temperature and the longer the wafer is kept at peak temperature, the more and the larger Ag-crystallites are formed. However, this does not necessarily mean that with increasing crystallite density the electrical contact will be automatically improved. That is because at the same time a glass layer is formed at the contact interface. The larger the Ag-crystallites, the more silicon is oxidized and dissolved in the glass matrix, which may form an insulating layer between Ag contact structure and Ag crystallites in the Si surface.

In Fig.7 the contact resistance is shown as a function of the initial glass content in the contact inks together with SEM images of the contact interface. If the glass content is too low (<1 weight-% of the total ink), no crystallites are formed, the SiN_x-layer is hardly opened and the TLM-measurement (transfer length method) gives a high contact resistance. For inks with more than 30 weight-% of glass the SiN_x-coating is totally removed, a high number of large Ag-crystallites are found which

are separated from the bulk Ag contact lines by a thick glass layer, and again, high contact resistances are measured. The optimum glass content is somewhere in between resulting in a sufficiently large number of Ag-crystallites and thin glass layers. No significant difference in the contact resistance is observed when either 2 or 10 weight-% glass is used. This is a remarkable broad range in which the glass content can be varied. This can be explained by the total amount of glass at the contact interface and the contact formation. For low glass contents the nitride layer is only opened locally whereas for high glass contents a lateral opening was observed. The measured contact resistance in both cases was almost constant. The increased glass layer thickness (with increasing glass content) seems to be overcompensated by an increased number of current paths. The same behaviour was observed when the printing height of the contacts was varied [12].

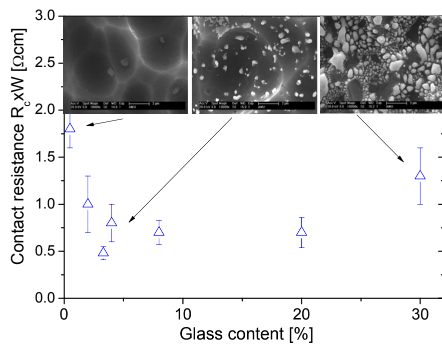


Figure 7: Contact resistance to an n-type emitter with a sheet resistance of 65 Ω/sq. using silver inks with various glass contents

4 RESULTS ON HIGH EFFICIENCY SOLAR CELLS

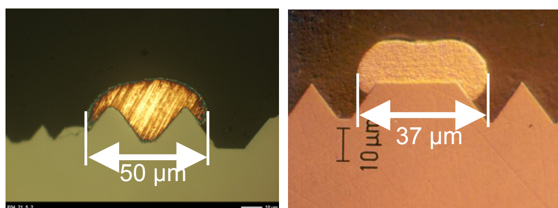


Figure 8: Cross sections of front side contacts; (left) printed, fired and plated contact and (right) evaporated and plated contact

For the solar cells presented in this work, we used 4” FZ-material with a base resistivity of 1 Ωcm. The cell size is 2x2 cm², the front side is randomly textured and has a shallow emitter with a sheet resistivity of R_{SH}=110 Ω/sq. which is passivated by a PESVD-SiN_x layer. The front side grid was adapted to the emitter according to contact parameters like contact resistance ρ_c = 2-3 mΩcm², line conductivity $\rho_f = 2.0\times10^{-8}$Ωm, and finger width w_f= 45 µm (the fired seed layer has a width of w_c = 20 µm). The seed layer was deposited using aerosol jet printing. The optimum contact distance for the given parameters was calculated, using the simulation program Gridsim, to l = 1.3 mm which results in a shaded area fraction of only 3.3%. The passivation layer of 10 nm aluminium oxide at the rear side was deposited with an plasma assisted atomic layer deposition (PA-ALD) Al_2O_3 and thickened by a 90 nm thin layer of PECVD SiO_x. The rear side was metalized with a 2 µm thin layer of thermal high rate evaporated aluminum [13] and contacted by laser fired contacts [14].

This relatively simple solar cell structure (called industrial type) with printed contacts and a shallow emitter was compared to a solar cell with a more advanced front side in order to evaluate the potential for further improvements. The high efficiency type solar cell features inverted pyramids, a deep emitter with a sheet resistivity of R_{SH}=120 Ω/sq. and a surface concentration below N_D < 1×10^{19} cm^{-3}, see Fig.9. This emitter is passivated by a thick thermal oxide and metalized by evaporation of Ti-Pd-Ag. Therefore, several photolithography steps are necessary. The contact fingers have a spacing of only $d=0.8$ *mm* and a width after plating of $w_f = 37$ *µm* resulting in a shaded area of 5%.

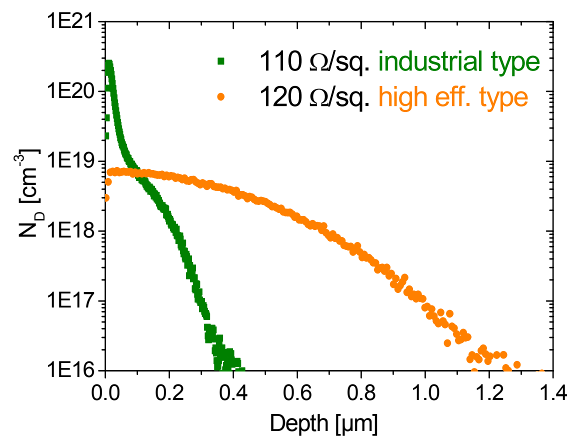


Figure 9: Phosphorous depth profiles for the two different emitters

Even if the IQE of the high efficiency solar cell for the short wave length region is higher compared to the industrial type cell, see Fig.10. a gain in j_{sc} is not visible. The higher *jsc* value for the industrial type solar cell can be explained by the smaller shaded area and the use of SiN_x as passivation and anti reflection coating. The main advantage of the high eff. front side is the combination of a reduced surface doping concentration with an effective passivation which leads to an increased value in *Voc*. Here, the industrial type solar cell has still some room for further improvements. All IV-parameter are summarized in Table1 for an industrial and high efficiency type solar cell. The fill factor of more than 80% in case of the printed solar cell indicates an low ohmic contact between paste and emitter and proves the effective contact formation on emitters with a sheet resistance as high as R_{SH}=110 Ω/sq. even if the contact area on the front side is reduced to only 2-3%.

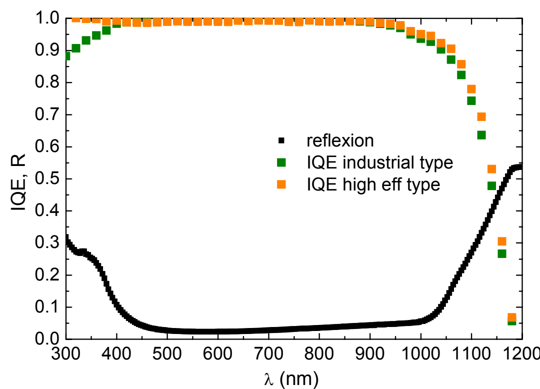


Figure 10: Quantum efficiencies and reflectance measurements for the "industrial type" and "high efficincy type" solar cell

Table 1 *IV*-parameters for the best industrial type and high eff. type solar cell. The solar cell material is FZ-Silicon and the solar cell size is 4 cm².

Font side	V_{OC} [mV]	J_{SC} [mA/cm²]	*FF* [%]	η [%]
Photo lithography	684	39.8	79.8	21.7*
Printed and fried	663	40.4	80.4	21.5 *

***All results were independently confirmed by CalLab ISE.**

5 CONCLUSION

The fundamental reactions between a silver contact ink and an n-type silicon surface were investigated by thermo-gravimetric differential-thermal analysis. The reaction mechanism between lead oxide and silicon in the presence of silver were clarified. Lead oxide reacts exothermically with Si at a temperature of 680°C; the contact formation with silicon is actively promoted and silver contact crystallites are formed from a liquid Ag-Pb phase. The measurements together with results on solar cells were used to develop a seed layer ink that was applied to high efficiency solar cells with an Al_2O_3-passivated rear side. Efficiencies close to high eff. Solar cell structures using a photolithographically defined front side were achieved. The best printed and fired solar cell achieved an efficiency of η = 21.5%.

ACKNOWLEDGEMENT

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AL-SI ALLOY FORMATION IN NARROW P-SI CONTACT AREAS

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ABSTRACT: Solar cells with dielectrically passivated rear side and screen printed local rear contacts combine the high performance potential of the PERC (passivated emitter and rear cell) concept with the well-established metallization method of nowadays industrial solar cells. This article presents a specific analysis of the formation of such localized screen printed Al-Si contacts. We observe that the contact resistivity depends on the width of the contact openings, and decreases when reducing the contact area. The optimal contact formation is observed for lateral contact widths smaller than 50–80 µm. Analysis of the Al-Si alloy formation by scanning electron microscopy (SEM) and energy dispersive X-ray spectrometry (EDS/EDX) analysis shows that the alloy formation below the contacts is more homogeneous in such small openings than in larger ones.

1 INTRODUCTION

Several papers have been already published in the field of Al-Si contact formation and solar cells with passivation on front and rear side. This work will give at the beginning a brief review.

Al-Si alloy formation. Many publications are focused on Al contact formation of solar cells. An extended analysis of local Al contacts has been done for example by Uruena *et al.* with the result that after the opening of the dielectric barrier by laser the formation of up to 60 µm long Al-Si pyramids into the Si-bulk are seen [1]. More specifically is the analysis of the Al-Si alloy formation by Bock *et al.* [2], which gives an understanding of the high positive concentration (i. e. increased doping) normally found at aluminium-doped regions. A nice model of the Al-Si alloying process, including the composition of the microstructure, has been given by Huster [3] and Popovich *et al.* [4], based on the discussion of the equilibrium phase-diagram of Murray and McAllister [5]. Some of these results are also demonstrated and thus verified within our work. Recently, Lauermann *et al.* [6] analysed the cross-sectional junction of Al-Si alloying. Furthermore, recent publications are dealing with the characterization of laser fired contacts [7] and the optimization of rear patterns for low-cost and high-efficiency PERC solar cells [8].

Passivated emitter and rear cell (PERC). The PERC solar cell (Figure 1(a)) was first presented by Blakers *et al.* [9]. A reduction of the Si-material thickness and an improvement of the rear contact are for the PERC a design consideration. Including a passivation layer at the rear side together with local back surface contact formation, a further increasing of the solar cell efficiency has been already demonstrated [9-14]. The rear surface passivation improves the internal charge carrier reflection into the Si-bulk, compared to a standard fully covered Al-area. Another impact is the minimizing of the rear surface recombination velocity, by a reduced Al metallization.

Contact resistance. The electrical contact resistance has been defined by Windred [15] as the resistance offered to the flow of current during its passage across the interface between two conducting materials which are in contact with each other. Its properties are strongly influenced by the state of the contact surface and its shape. The contact resistivity is defined as the reciprocal of the derivative of current density with respect to voltage. It is the contact resistance normalized by the area. Berger [16] and later also Schroder and Meier [17] have given useful definitions and explanations of many methods to determine the contact resistivity. They have shown measurements for contact resistivity of Al-Si contacts depending on surface doping concentration. A spatial variation of the contact resistivity was already found and explained by taking into account the inhomogeneity of the contacts. A variation of the contact resistivity was found from the middle to the edges of the contact area.

Contact resistance measurement. One method to determine the contact resistivity from the geometry of planar contacts, the sheet resistance of the semiconductor beneath the contact, and the contact resistivity is called transmission line method (TLM, [16-18]). Melczarasky *et al.* [19] found a variation in the contact resistance of screen-printed Ag fingers, and discussed the findings as a result of the inefficiency of the method.

This article presents a specific analysis of the formation of localized screen printed Al-Si contacts that are applicable to industrial production of rear-passivated solar cells. We observe that the contact resistivity depends on the homogeneity of the alloy formation.

2 EXPERIMENTAL PART

We use *p*-type multicrystalline silicon wafers with a size of 156x156 mm^2 and a resistivity of 1-3 Ωcm. The samples are etched in a sodium hydroxide (NaOH) bath, in order to remove the wire saw damage from the surface. After a hydrochloric and hydrofluoric acid (HCl, HF) cleaning step a dielectric layer is deposited as a barrier against the Al-paste on the back of the *p*-type Si wafers.

The barrier is selectively opened by screen printing an etching paste, which contains phosphorus acid, a useful etchant of silicon nitride films. The activation of the etching properties is done by drying the wafers slowly on a belt furnace. The wafers are cleaned in an ultrasonic bath with deionised water and 0.2% potassium hydroxide (KOH) after etching and fired in a lamp-heated conveyor belt furnace.

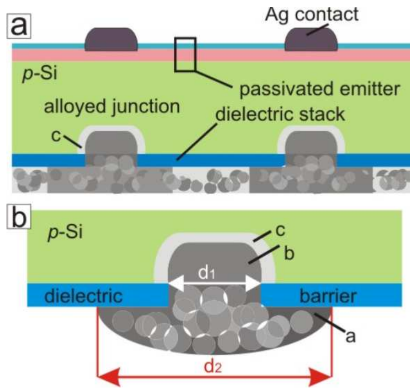

Figure 1: (a) PERC structure (texture not shown). (b) Al-Si alloy contact structure at the rear of the PERC cell.

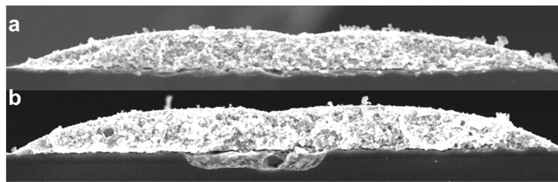

Figure 2: (a) Al finger alloyed on the same *p*-Si width. (b) Al finger alloyed on a narrow dielectric open area.

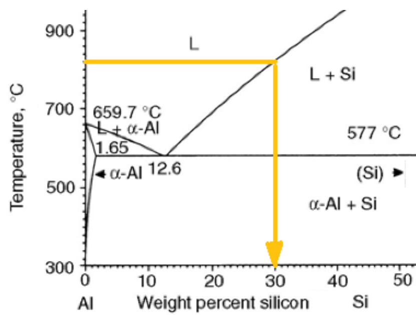

Figure 3: Al-Si alloy phase diagram [5] .

Our PERC cells (see Figure 1(a)) feature screen printed openings through the rear passivation layer, covering about 9% of the rear surface. The contact of the Al paste is made to the Si-substrate via these fine opening lines. The contact formation takes place only in the fine dielectric barrier openings, where the Al-Si alloy is formed.

Four different widths d_1 of the contact openings are chosen, 50, 75, 100 and 125 µm. Smaller openings than 50 µm are hard to realize by using common screen printed technology Wider openings than 125 µm would decrease the total passivated area of PERC cells too much, since the contact spacings are typically smaller than 1 mm.

Variable Al finger widths are screen printed on these dielectric openings, in order to analyze the effect of the contact geometry on the contact resistance. The main goal of this work is to explain the Al-Si alloy formation under local contacts for PERC solar cells and to clarify its influence on the minimization of the contact resistivity. The SEM-identification of the structure and geometry of the samples is obtained after special laser cutting and cleaning.

2.1. The Al-Si alloy junction

Figure 1(b) shows our cross-sectional model of the alloyed contact structure at the rear of the PERC cell. In the figure, d_1 represents the dielectric barrier opening width (the contact surface), and d_2 represents the screen printed Al finger width that corresponds to the amount of Al mass. Due to the spreading of the etching paste during drying, the real values for d_1 are 80, 110, 135 and 170 µm, as measured by optical microscopy. The screen printing of the Al-fingers on the openings is achieved by optical alignment. The width of the Al fingers is d_2=700 µm.

2.2. Contact formation

After the drying of the Al paste most of the organic binders are burnt out. During increasing the temperature the alloying process starts with the melting of the aluminum at 660°C (see Fig. 3). At the peak temperature almost 30% of the liquid phase consists of silicon [3]. On cooling down, the silicon is rejected from the melt and builds up the high *p*-doped layer called the back surface field (BSF [20]). Below the temperature of 577°C [21] the remaining liquid phase solidifies and forms the eutectic layer.

A micrograph of the different layers (compare the sketch of the layers a, b, c in Fig 1(a) respectively) as formed after the alloying process and measured by SEM is shown in Figure 4:

Layer a: The porous Al-matrix layer (Al-17%Si) formed by Al-spherical particles, Si, Al_2O_3, and other lower concentrated defects.

Layer b: The strong Al-Si alloy formation (eutectic composition of Al-12.6%Si [21]).

Layer c: The highly doped *p*-layer or BSF formed by the aluminium containing interface (Si-1%Al).

The concentration of Si is higher in the Al-matrix than in the eutectic-layer (17% compared to 12.6% of the eutectic), maybe because the remaining Si in the Al matrix is not driven back completely during the fast cooling down.

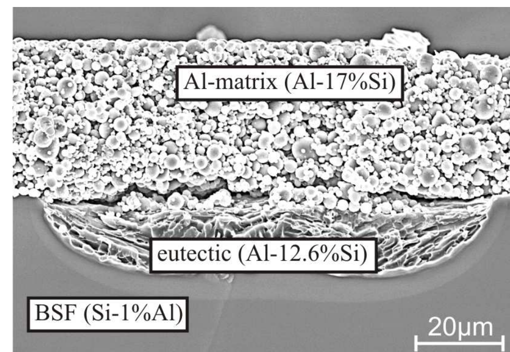

Figure 4: SEM Al-Si alloyed junction with different layers.

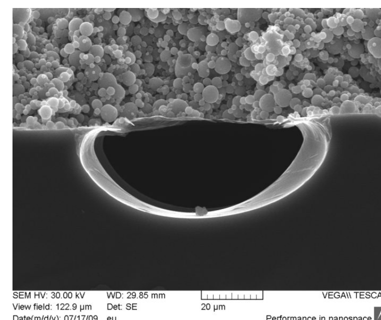

Figure 5: Cavity below the Al-matrix, with thin BSF formed.

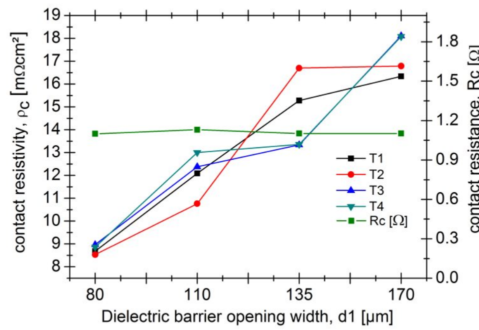

Figure 6: y-axis left: contact resistivity of a 700 µm Al finger width versus four different dielectric barrier opening widths, for different firing conditions (i. e. T1<T2<T3<T4). y-axis right: absolute constant resistance.

Sometimes cavities below the contact openings are found (Figure 5). One explanation may be that the Al-Si alloy is formed and a thin BSF is established, but depending on the contact surface, the firing temperatures and the fast cooling down, the alloy is decomposed before reaching the eutectic temperature of the Al-Si alloy and finally Si and Al are driven back into the Al-matrix.

3 RESULTS AND DISCUSSION

Figure 2(a) shows a 700 µm Al finger alloyed on a *p*-type silicon surface, representing a standard alloying process. The 10 µm deep eutectic formed all over the *p*-Si surface is normally found at the rear of standard solar cells. By reducing the contact area a strong Al-Si alloy formation is found in the bulk (20 µm) below the contacts (Fig. 1(b)). During the alloying process of Al on Si [3,5], the solid Al particles change to liquid state above the eutectic temperature, starting to alloy locally on the Si surface (also indicated by our pre-experiments, and by [1]). When d_1 is reduced and d_2 is constant, more Al material is available for alloy formation within the dielectric opening (Figure 2(b) compare to Figure 2(a), also Figure 4). Since our Al-paste does not fire through the dielectric barrier, the Al present on top of the dielectric in the vicinity of the opening is attracted towards the Si substrate (also observed by [1]). Consequently, the liquid Al penetrates into the openings, alloying deeply with the Si substrate (Figure 4). This explains why, after the cooling down of the material, a strong Al-Si alloy formation is found below the contacts, which is much deeper than a standard full-area Al BSF.

Results of the measured contact resistivity ρ_c versus dielectric barrier opening width are shown in Figure 6, for different firing conditions. The Al finger width (d_2) is 700 µm, and four different dielectric barrier opening widths (d_1 = 80 to 170 µm) are prepared. Similar results were found for different Al finger widths between 300 and 1000 µm on mc-Si and CZ-Si material, respectively. In Figure 6 also the total contact resistance R is plotted which is constant for all different opening widths. However, there is a strong dependency of the contact resistivity on the dielectric barrier opening widths but only a weak one on the firing temperature.

Already Berger [16] found a lateral variation of the measured resistivity for Al-Si contacts. The contact resistivity seems to depend on the homogeneity of the surface. Theoretically the dependency of the contact resistivity should be only on the doping and temperature [16, 20]; therefore we expected to observe no dependency of the contact resistivity on the contact area. The lateral and vertical formation and expansion of the alloy in the confinement of the barrier opening depends on dielectric barrier opening width. The Al/Si-alloy penetrates deeper into the Si bulk material when reducing the width $2r$ (Figure 7(a)), and at the same time also the contact resistivity is reduced. Then, a homogeneous alloy of Al-Si and BSF are formed across the entire barrier opening, for narrow dielectric openings with a BSF of 8 µm depth, extending underneath the dielectric layer. By increasing the dielectric openings (2r), we find inhomogeneous alloy geometries as manifested by two deeper indentations at the edges and an inhomogeneous planar surface in between.

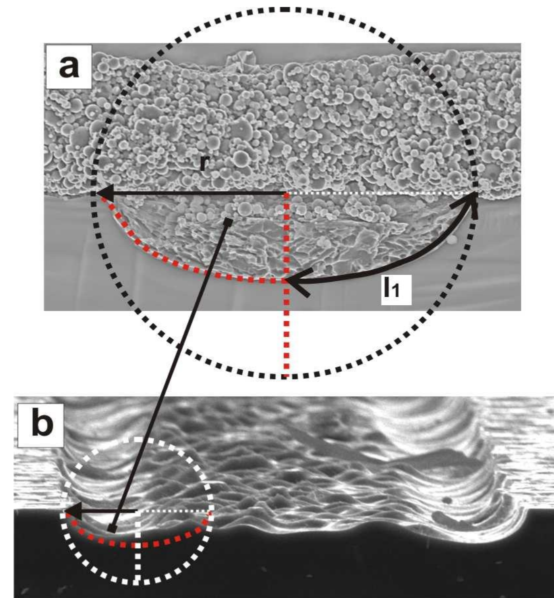

Figure 7: (a) model to calculate the real contact surface $2l_1$. (b) for broader openings a plateau appears between the two deep indentations at the edges. Its width increases the dielectric opening width.

By further increasing of the barrier opening the Al-Si alloy separates further into two identical indentations at the open edges, thus $r < d_1/2$. Figure 7(b) shows the shape of the alloy formation, of the two alloy indentations as separated by a plateau in the Si substrate after HCl etching of the Al matrix.

As shown in Figure 7(a) a real contact surface should be taken into consideration for the TLM calculations. The real contact surface is not two times the radius r of the circle, but two times the large l_1. From the figure we see that

$$l_1 > r\,.$$

Experimentally we have found that,

$$l_1 \approx 1.3r\,.$$

During the TLM measurement, the surface $2r$ should be replaced by $2l_1$ for the calculation of the contact resistivity, where $2l_1$ is the real surface of contact for the Al-Si alloy. Now the real contact surface for a narrow opening of 80 µm (r=40 µm) is:

$$2l_1 = 2*1.3r = 104\mu m$$

Assuming that the entire contact length $2l_1$ contributes to current transfer [17], we get:

$$\rho_c = R*A_c = 1.1[\Omega]*(1[cm]*2*l_1[\mu m]) = 11.4m\Omega cm^2\,,$$

with a sample width of 1 cm. The contact resistivity of a 700 µm Al finger contacted on an 80 µm dielectric barrier opening is 11 mΩcm^2, where the real contact surface is 104 µm. The two alloy-forms found at the edges of broader openings present similar geometry (Figure 8, red lines). The real surface of contact ($2l_1 \approx$ 104 µm) remains constant and does not change for wider dielectric openings. Just the inhomogeneous and planar surface in between (Figure 8, black dashed line) is changing and its width varies proportional with the dielectric opening width. The two separated Al-Si alloy indentations appear at the edges of dielectric openings broader than 80-100 µm.

Comparing our analysis with the contact resistance result leads to the conclusion that the planar surface (dotted line in Figure 8) does not contribute to reduce the contact resistance. If we take into consideration just the real contact surface $2l_1$, and remove the variable planar surface from the calculations, the contact resistivity of screen printed Al fingers on *p*-Si areas should be constant. We assume that the contact resistivity should remain constant when the same Al amount is printed on even narrower contact openings than the ones presented in this work.

4 CONCLUSION

We demonstrated that the contact resistivity depends on the contact surface area, where the Al-Si alloy is formed. This is found only for wide screen printed Al fingers on narrow dielectric barrier openings (i. e. of widths below 100 µm).

The analysis of the Al-Si alloy junction showed a dependency of the Al-Si alloy formation on the Al amount per opening. Similar alloying structures (indentations) are found at the edges of the wider openings, where the real contact is formed. Thus, very narrow openings are required for the design of the back contacts of PERC cells.

The results can be directly applied to optimize the Al-Si alloy formation for advanced back-contact solar cells, where the minimization of the contact resistance losses and the overall improvement of the back-side passivation are mandatory.

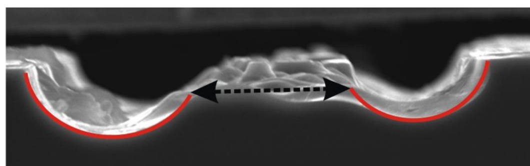

Figure 8: Real contact area (red). Inhomogeneous surface of contact (black), increasing the contact resistivity.

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CHARACTERIZATION OF ALUMINIUM SCREEN-PRINTED LOCAL CONTACTS

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ABSTRACT: The formation of a Back Surface Field (BSF) during the alloying of a screen-printed aluminium paste with the silicon substrate is a critical step for the performance of solar cells. In this study, wafers with a locally contacted structure at the back side are investigated with Scanning Electron Microscope (SEM). An industrially feasible contacting technique is considered and a variation of the contact structure has been investigated. Moreover, a variation in the amount of screen-printed paste is proposed. Additionally, the effect of the crystallographic orientation of the grains on the electrical contacts is evaluated by investigating both mc and FZ samples. In conclusion, a model of the local contact formation is proposed. The understanding of the alloying dynamics allows the adaptation of the process in order to control the formation of the BSF layer.

1 INTRODUCTION

Currently, silicon is the most common material used for the large-scale production of solar cells, but wafers still represent a significant part of the costs of current solar modules. According to [1], lower W_{peak} prices can be achieved by increasing the performance of the cells and, simultaneously, by decreasing the consumption of silicon in the manufacturing of the wafers. In this context, Passivated Emitter and Rear Cells (PERC) represent a very promising technology since they are industrially feasible on thin wafers [2]. Anyway, PERC cells can become an alternative to the standard solar cells only if their improved performances are obtained at comparable production costs.

At their state of the art, standard industrial cells and PERC cells present a similar front side but a different rear side. Local contacts are realized on the back surface of PERC cells to allow a significant amount of surface to be passivated.

So far, the dynamic of the formation of the back contact has been largely investigated for standard cells. For screen-printed pastes, which are fired in a high temperature furnace with a Rapid Thermal Process (RTP), a model of the contact formation is largely detailed in [3]. According to this model, the rear contact of standard cells consists of a stratification of three different layers: fired paste, eutectic alloy and an underlying silicon layer. This latter is highly doped with aluminium. Hence, a high-low junction (p^+–p) [4], better known in the literature as Back Surface Field (BSF), is formed at the back side. This built-in field, when properly formed, behaves like an electrical mirror for the minority carriers and can reduce the surface recombination velocity (SRV) at the contact ([5] and [6]).

This work concentrates on the formation of local contacts. The analysis is carried out on silicon substrates. These are treated with the same techniques used for the realization of solar cells.

In the present study, the rear side of the wafer is properly structured in order to realize point like contacts at the back side. Three main contacting techniques are industrially feasible: Laser Fired Contacts (LFC) [7] and structuring by means of Inkjet (IJ) [8] and Laser Ablation (LA) [9]. Earlier studies concerning the formation of local contacts have already been detailed for LA in [10] and [11]. Specific investigation on contacts are also present for the laser fired contact case [12].

2 PREPARATION OF THE SAMPLES

The Inkjet technique is the focus of this work. Two variants are explored; they are referred to as “hollow configuration” and “flat configuration”. Below the preparation procedure is described. The main steps proper of the local contact techniques mentioned above are shown in Figure 1.

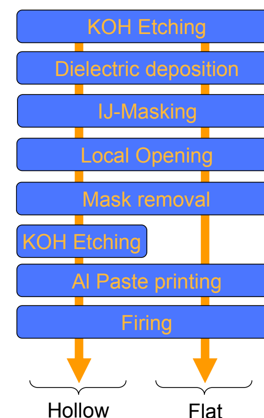

Figure 1: The process flow of the two different configurations is depicted here.

The investigation is carried out in parallel on mc and FZ-Si wafers. Both substrates are p-type doped with a starting thickness of 200 µm. The mc-Si wafers have a resistivity of ρ=0.5÷2.0 Ω·cm and are fully squared with a 125 mm side. FZ-Si wafers have a resistivity of ρ=0.8÷1.2 Ω·cm and are pseudo square shape with a radius of 150 µm and an edge length of 125 mm. The surface of the samples is KOH etched in the case of mc-Si wafers and shiny etched for the FZ-Si wafers.

The back surface is ready for the deposition of the rear passivation. This latter consists of a SiN_x layer deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD)

After depositing the passivation layer, both surfaces of the wafers are covered with an inkjet-printed wax. The front side is fully masked whereas, on the rear side, the mask presents windows with a well-defined geometrical pattern, optimized for the IJ-printing process [8]. Then the wafers are dipped in a 20% HF solution which is able

to etch locally the passivation wherever the wax is not protecting the SiN_x layer.

After removing the masks in a bath of solvents, the wafers are split in two groups. These will represent the two configurations hollow and flat.

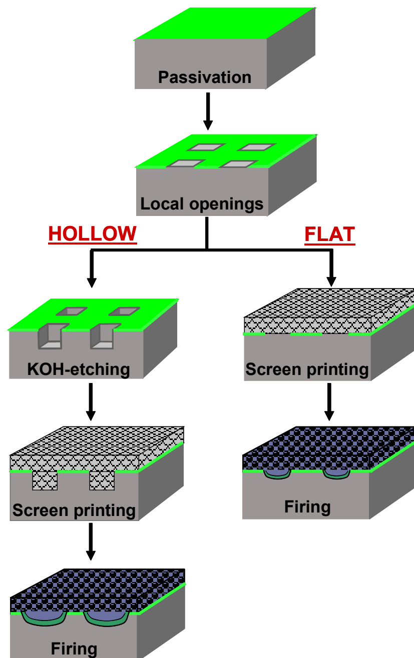

Figure 2: Sketch (not in scale) of the back side processing for the realization of local contacts with both Inkjet flat and hollow configurations.

The first configuration is achieved by hollowing out silicon wherever the passivation is locally open. A 5-minute-long dip in 30%-KOH solution at 80°C ensures the etching of silicon in correspondence of the openings.

On the other hand, the second configuration does not need this additional processing.

Figure 2 shows sketches of the back side structure achieved with the two different configurations after each step of the process.

The wafers are metallised with a screen printing process. The aluminium paste used consists mainly of pure-Al-spheres with a diameter of ~10 µm spread in a matrix of solvents which does not contain glass frits or any special compound useful to enhance the mechanical properties of the fired paste.

After screen printing, the paste is dried in a thermal process in order to remove the solvents and then it is addressed to the firing in a RTP furnace. The peak firing temperature is set at $T_{peak} = 900°C$.

The alloying process and, thus, the electrical quality of the formed contact are strongly affected by the oven firing process. More precisely, the peak temperature and both heating and cooling ramps can be critical for the contact formation as well as the amount of paste screen-printed [13]. In this regard, both heating and cooling ramps have been adopted from the thermal profile which is optimized for the processing of standard cells.

Moreover, different wet amounts of paste have been screen printed. Hence, information on the influence of this latter parameter on the BSF formation can be gathered.

3 POST-TREATMENTS AND CHARACTERIZATION

The investigation of the local contact formation is carried out on post-treated samples. Top views and cross sections of the local contacts have been prepared and characterized. For the preparation of the cross sections, different post-treating steps are needed as indicated in Figure 3.

3.1 Top view preparation

The sintered samples are dipped in an HCl solution to remove the paste and the formed alloy.

To ensure the complete removal of the layers mentioned above, the HCl-etching has been extended to a dozen of minutes.

3.2 Cross section preparation

Small specimens are cut from the samples with a dicing saw but, since it was observed that such a mechanical process can locally damage the metallic layer, the metallization had been previously covered with a polymeric resin. This latter is spread on the top of the metallization first and is then cured in an oven at 120°C. After sawing of the specimen, the cross section is polished by means of argon ion beams in order to achieve a flat and even surface.

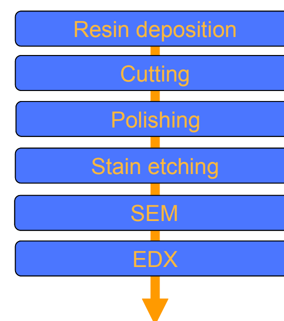

Figure 3: The process flow shows the sequence of the post-treatments. These additional steps allow displaying the whole stratification of the contact.

Then the specimen is dipped and etched in a solution of HF-HNO_3-CH_3COOH (1:3:6). This treatment is referred to as stain-etching in the literature. The effect of this post-treatment on the cross section is shown in the sketch of Figure 4. After stain-etching, a new layer is engraved right below the alloying region.

Similar methods, closely related to this argument, are used in literature [14]. In particular, since such stain-etching solution is able to etch selectively p^+–doping regions in the silicon substrate [15], the etched area indicates the formation of a p^+–doped layer.

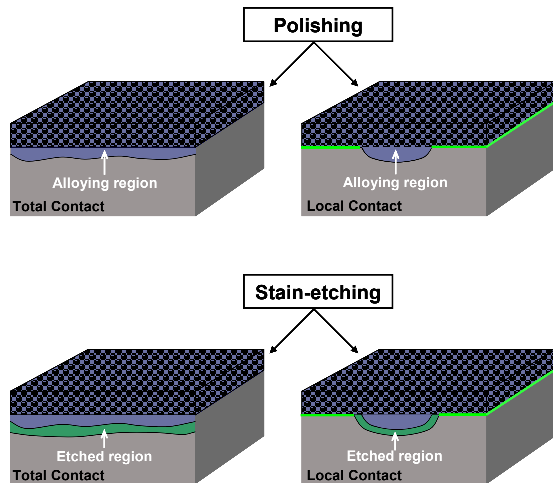

Figure 4: Sketch not in scale of the cross sections of total and local contacts. After polishing, an alloying region is visible at the microscope. Stain-etching reveals the presence of a new layer in the substrate.

The doping is expected to be a consequence of the aluminium in the system. This presence is due to a mechanism which can be described with existing models [3].

Previous investigations on aluminium doped regions revealed that the amount of Al-doping reaches its maximum value at the interface with the Si-bulk and decreases towards the surface of the wafer ([6] and [16]). Therefore, within SEM the observation of a stain-etched contact leads not only to the identification of the doping region but especially to the measurement of both its maximum depth and its thickness. The effectiveness of the present investigation is based on testing and optimizing the method on samples where no local opening confinement is made. The correspondence of the results achieved with the data acquired from literature ensures the calibration of the method.

3.3 Characterization

For a better understanding of the characterization a process flow is sketched in Figure 5.

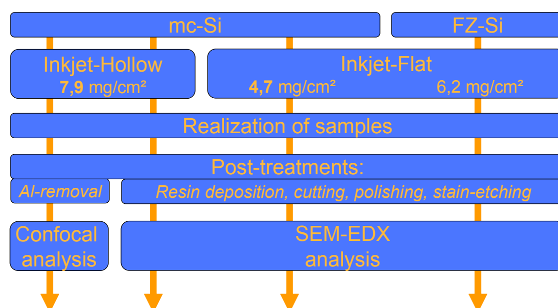

Figure 5: Process flow of the characterization.

According to Table 1, materials, processes, amounts of paste, post-treatments and type of characterization are indicated with symbols. Typically 4 to 6 different contacts from each sample have been investigated.

The top view relief has been characterised with a confocal microscope. The tool allows the study of surfaces.

The scanning electron microscope was used due to its high magnification. Furthermore, energy-dispersive X-ray spectroscopy (EDX) was used to identify the composition of the observed material.

Table 1: A list of the symbols adopted in the following section is shown.

Feature	Identification
Material	-
mc-Si	a
FZ-Si	b
Process	-
Hollow configuration	I
Flat configuration	II
Amount of paste	
4,7 mg/cm²	α
6,2 mg/cm²	β
7,9 mg/cm²	γ
Post-treatments	-
Resin deposition, cutting, polishing, stain-etching	s
Paste removal after firing	c
Characterization	-
SEM/EDX analysis	S
Confocal analysis	C

4 RESULTS AND DISCUSSION

This study aims to understand not only the dynamics of the contact formation but also how it is possible to influence the process in order to improve the electrical quality of the contacts. The enhancement of the electrical performances at the back side is expected to be achieved by forming an even BSF layer which is homogeneously surrounding the local contact. This argument is pointed out in the literature for the case of laser fired contacts [17].

Two configurations were performed. The flat configuration is an opening procedure with an Al-Si interface as large as the contact opening. On the other hand, the hollow configuration is proposed to increase this interface during the firing.

4.1 Hollow configuration

Figure 6 shows the image of a local contact with hollow configuration.

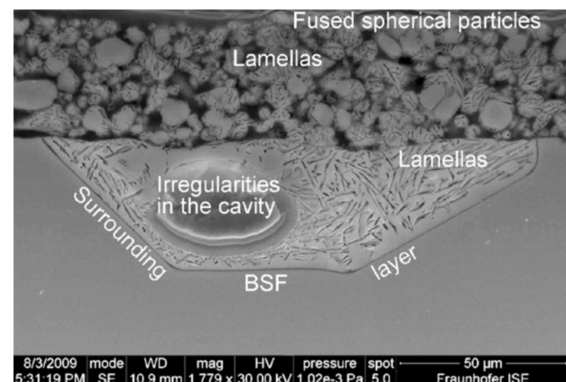

Figure 6: SEM image of a local contact (Material “a”, Process “I”, Amount of paste “γ”, Post-treatment “s” and characterization “S”).

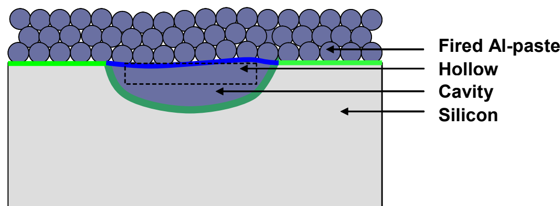

Figure 7: Sketch not in scale concerning the image shown in Figure 6. This image represents how the hollow enlarges during the firing to form a cavity. A new interface is formed between paste and cavity (blue line).

The main features concerning the formation of the contact shown in Figure 6 are listed below:

- The Al-spheres present in the fired paste can locally fuse together. In previous analysis, oxide shells were allowing only a weak bond between the particles [14];
- The original 10 µm-deep hollow enlarges to form an almost 40 µm-deep cavity below the paste (Figure 7). An analysis carried out by means of Energy Dispersive X-ray spectroscopy (EDX) revealed that it is filled with Al-Si alloy;
- Lamellas, which are largely present in the cavity, are visible even in the fired paste. In this regard, traces of lamellas are found far away from the contact at distances of more than 20 µm from the opening. This is a consequence of the strong Al-Si interaction occurring during the high-temperature firing. Further on, the lamellas are random oriented;
- A void region is present in the cavity but its origin is uncertain;
- Despite the pre-firing paste-silicon interface (hollow), a new interface, even with the remaining wafer surface, is formed after firing (Figure 7). This change reflects that a very strong interaction between the Al-spheres inside the hollow and the underlying silicon bulk occurs. In fact, during the alloying process, the Al-particles present in the hollow melt together completely. This creates a homogeneous aggregation of matter within the whole cavity. Nevertheless, in Figure 6, in the area right above the void the original spherical shape of the particles can be distinguished;
- A very thin BSF layer surrounds evenly the cavity at its interface with the silicon bulk;
- Since the cross section of a cavity is not hemispherical, the crystallographic orientation of the grains plays an important role in the alloying process.

To further support this final remark, confocal measurements have been performed after removing sintered paste and formed alloy from the back side in a hot HCl etching solution.

Figure 8 shows the top view of a local contact with hollow configuration at the confocal microscope after etching the specimen in an HCl-bath.

Figure 9 shows the measurement of the profile of the cavity-silicon interface along the direction indicated in Figure 8 by the red line.

Such an extreme profile is chosen in order to emphasize the influence of the crystallographic orientation of the grains on the contact formation.

Anyway, although an optical measurement with a confocal microscope is particularly useful to characterize the maximum depth of the cavity, it does not give any information concerning the stratification of the contact and the eventual formation of irregularities inside the cavity.

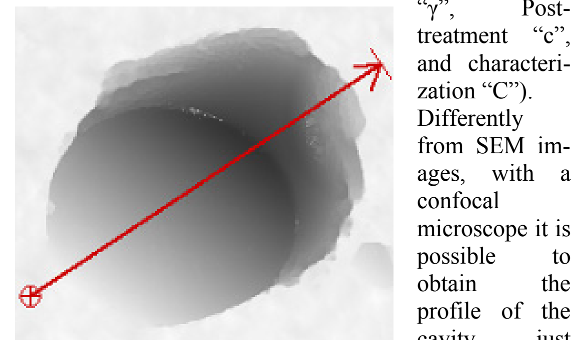

Figure 8: Top view of a local contact at the confocal microscope (Material “a”, Process “I”, Amount of paste “γ”, Post-treatment “c”, and characterization “C”). Differently from SEM images, with a confocal microscope it is possible to obtain the profile of the cavity just along the desired plane (red line). For the depth and size evaluation refer to the scale shown in Figure 9.

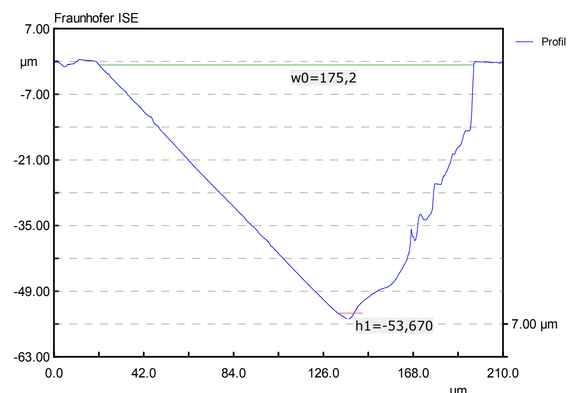

Figure 9: Depth profile of the cavity-silicon bulk interface concerning the plane indicated in Figure 8.

4.2 Flat configuration

On the other hand, when a lower amount of paste is screen printed on a flat local opening, some irregularities are noticed as shown in Figure 10.

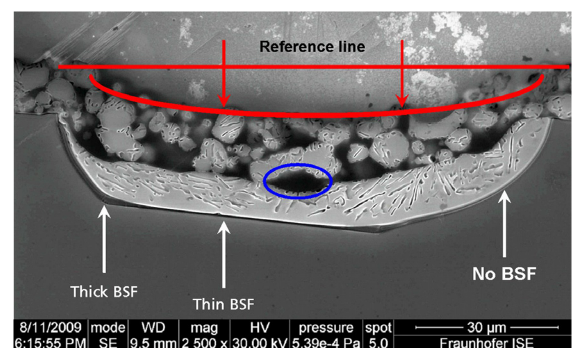

Figure 10: SEM image of a local contact (Material “a”, Process “II”, Amount of paste “α”, Post-treatment “s” and characterization “S”). The formation of a non-closed BSF is observed.

The main results concerning Figure 10 are:

- During the firing, the metallic paste on top of the opening collapses slightly towards the Si-bulk as indicated by the red arrows;
- Voids are formed between the fired paste and the alloy in the cavity (blue circle);
- An irregular BSF is formed as indicated by the white arrows. The BSF is not surrounding completely and homogeneously the cavity;
- Though uneven (non-closed), the BSF can be locally thicker than the one observed for the hollow configuration shown in Figure 6;
- As well as for the specimen with a hollow configuration, planes of slower interaction between aluminium and silicon are observed.

The collapse of the paste is not due to a local effect since this phenomenon was noticed in all the contacts with a flat configuration and with a reduced amount of screen-printed paste (α). The explanation of the collapse is due to a limited number of spherical particles on the wafer surface. Because of that, the native oxide surrounding the paste spheres (Al_2O_3 shells) can only form weak bonds amongst particles. Hence, when the paste melts during the firing, these bonds are not able to keep the particles in a steady position and, as a consequence, the collapse occurs.

Another drawback which depends on the reduced amount of screen printed paste is the presence of voids at the paste-cavity interface.

In conclusion, during the liquid phase of the firing, very low amounts of paste cannot provide the silicon surface with a sufficient amount of aluminium atoms. A non-closed BSF is the result of an insufficient aluminium deposition. This happens also for standard cells [3]. Relevant local losses are expected at the back side of a solar cell, especially when a positively charged layer like the SiN_x passivation is deposited [18].

Now, in order to achieve results which depend on a known grain orientation, FZ mono-Si wafers are processed. Such a local contact (Figure 11) is compared to a previously described implementation (Figure 10). Increasing the amount of paste from α to β brings about:

- The formation of a deeper cavity;
- The absence of a collapse of the paste towards the wafer surface;
- The formation of an even, though very thin, closed BSF layer (540 nm).

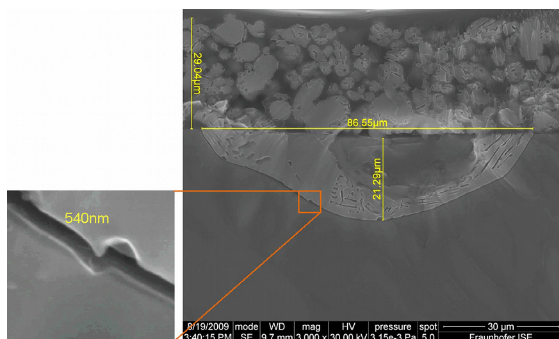

Figure 11: SEM image of a local contact (Material “b”, Process “II”, Amount of paste “β”, Post-treatments “s” and characterization “S”).

4.3 Alloying model

In conclusion, from the information gathered with these observations on the samples, it is possible to resume the ideas in a contact formation model which is based on the dynamic of Al-Si alloying for contacts with no geometrical constraints [3]. The binary phase diagram of Al and Si (Figure 12) is very helpful to understand how the observed sintered contact is achieved.

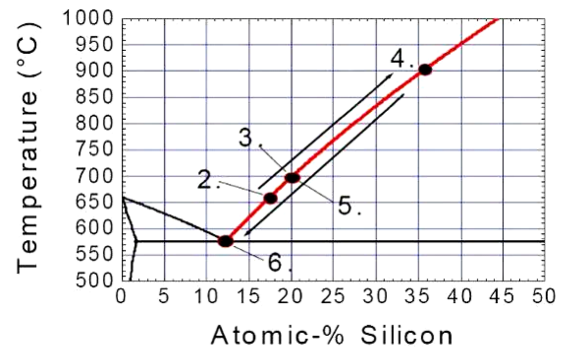

Figure 12: Al-Si phase diagram sketch. The numbers indicated in the image refer to the steps of the alloying (from [3]).

The model (Figure 13) explains the evolution of the system at the starting interface between silicon and aluminium.

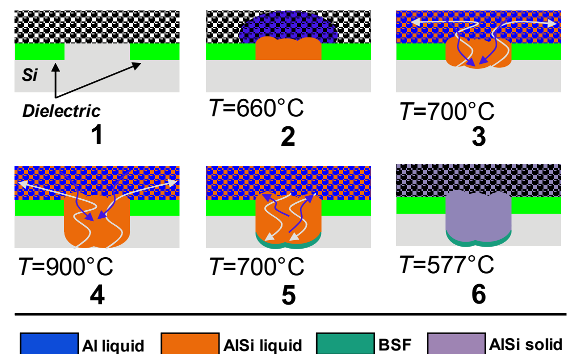

Figure 13: Sketch of the local contact formation during a RTP. The dynamic of Al-Si alloying consists of six different steps.

In particular, the alloying process can be summarized in six main steps:

1. Before the firing starts (step 1), the wafer is at room temperature and aluminium above the opening is silicon-free;
2. A steep increase in temperature leads the aluminium to melt (660 °C, 0% Si) and to start the alloying process with silicon (AlSi liquid). The situation moves from the ordinate towards point 2 on the phase diagram (660 °C, 17% Si). This volume contains liquid Al-Si alloy, and expands farther in the aluminium matrix and in the unprotected substrate;
3. By increasing the temperature further, the alloying process can drive more silicon in the melt. The native aluminium oxide keeps the volume of the paste particles constant, so an exact quantity of aluminium (equal to the volume of silicon incorporated in each particle) is driven towards the wafer surface. Blue and white arrows indicate Al and Si transport of matter respectively. This physical process is

completely ruled by diffusion. In fact, gravity can play a significant role in the alloying only when the two components of the melt are not soluble and differ strongly in density, which is not the case;

4. Stepping from point 3 to 4 (T_{peak} = 900°C), it is possible to observe that the only source of silicon is the substrate through the opening; for this reason, the digging can reach several tens of micrometres. According to the phase diagram, the percentage of silicon in the molten alloy increases up to 35% in normal firing conditions;
5. During the cooling down step, the mechanism of matter transport described at step 3 is reversed and silicon segregates from the melt and grows epitaxially on the substrate. Since this segregation is not perfect, few Al impurities remain incorporated in the Si lattice and dope the material. A local BSF is built up. However, this transport is not fast enough to bring all the excessive silicon back to the wafer surface before solidification. As a consequence, a significant amount of silicon, expelled from the Al-Si melt, curdles into several clusters, which are referred to as lamellas in the literature;
6. At the eutectic temperature (577°C) the remaining liquid phase solidifies in an Al-Si alloy of nearly eutectic composition.

Similar conclusions have been achieved by other institutes even though for a different local contacting technique and within a different characterization (see [10] and [11]).

5 CONCLUSIONS

The preparation of high-quality cross sections leads to the preservation of the stratification of the local contacts, whereas the stain-etching is a worth trusting method for characterizing the BSF layer.

According to the information gathered from the SEM observations of the local contacts, an alloying model has been proposed.

In particular, the final configuration of an IJ-local-contact shows a large cavity which is filled with an Al-Si eutectic layer very rich in lamellas. At the cavity-silicon interface a thin BSF layer is formed and for standard paste deposition it was measured to 540 nm. This latter layer is surrounding evenly the cavity as long as a sufficient amount of paste is screen-printed. In fact, a non-closed BSF has been observed for contacts with a flat configuration with 4.7 mg/cm² of paste.

The orientation of the crystals is significantly affecting the shape of the edge of the cavity. In this regard, planes of interactions have been observed at the confocal microscope and the hollow configuration turned out to be very helpful for achieving this latter result.

The importance of laying out a model is related to the possibility of modifying the process in order to achieve the desired structure for the contact.

Experiments with modification of temperature profiles are now ongoing. Consequences are expected in the epitaxial growth of the p^+–type region.

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UNDERSTANDING AND IMPLEMENTING HIGH QUALITY CONTACTS TO HIGH SHEET RESISTANCE EMITTERS FOR HIGH EFFICIENCY SOLAR CELLS

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ABSTRACT: The requirements for high efficiency solar cell include: high quality material, transparent emitter, excellent surface passivation and antireflection coating (ARC), and high quality contacts. In addition, fine and tall gridlines must be implemented in order to decrease shadowing and increase the short circuit current. However, it is challenging to contact homogeneous transparent emitters (~100-Ω/sq) with the manufacturing screen-printed fire through silver paste. This is because there is no silver paste that can make low resistance contact to the underlying silicon after firing through the SiNx ARC. More so, the shadowing associated with the 90-100 µm line width of the screen-printed cells will always limit the short circuit current and the efficiency. Therefore, in this paper we investigated screen-printed and inkjetted contacts to homogeneous transparent 100 Ω/sq emitters after light induced plating. The results showed that although 60-65 µm lines can be printed with the screen-printed pastes, the fingers grew to 90-100 µm with only 76-77% fill factor and efficiency of 17.8%. Whereas, the inkjet machine jets seed layers of ~38 µm linewidth, which grows to ~65 µm after plating to achieve >79% fill factor. The fine line seed layer and plated silver produced efficiency of 18.7% with 79.2% fill factor on 2.6 Ω-cm, 239-cm^2 Cz silicon with 100 Ω/sq emitters.The open circuit voltage of 633 mV and short circuit current of 37.5 mA/cm^2 is a fingerprint of high sheet resistance emitter.

1 INTRODUCTION

Solar cell efficiency is one of the key parameters to reducing the levelized cost of electricity (LCOE) associated with solar power to less than 10¢/kWhr. The key to increaseing the efficiency is to increase the three parameters: open circuit voltage (V_{oc}), short circuit current density (J_{sc}) and fill factor (FF). The high sheet resistance emitter with low phosphorus surface concentration can achieve high V_{oc} and J_{sc} but lacks the FF because of the accompanying high contact resistance at the semiconductor/metal interface. That is why the selective emitter approach, where the contact region is heavily doped to produce low contact resistance and low contact recombination is important. However, this requires the alignment and second diffusion steps, which adds to the process cost without any significant efficiency improvement. To avoid the additional steps, Hilali et al [1] used forming gas anneal to decrease the contact resistance for cells fabricated with 100 Ω/sq emitter and achieved 19% efficiency. Forming gas anneal, however, compromises the contact adhesion, and therefore is not suitable for manufacturing. Also, Mette et al [2] showed that the contact quality of screen-printed contacts to homogeneous high sheet resistance emitter can be improved by light induced plating of silver without interfering with the adhesion. Noted with the plated screen-printed contact is the linewidth, which increases with plating time. Thus, while gaining in FF, the overall efficiency is not better than cells with 60 Ω/sq emitter.

Because the efficiency gain with the plated contact in conjuntion with screen-printed contact is not high enough other low cost approaches to implementing the selective emitter are being investigated. For example Innovalight [3] is investigating the all screen printed technology, Rena [4] - the plated contacts, Suntech [5] - the Pluto technology and UNSW [6] - the laser diffused and plated contacts. So far efficiency of >19% on commercial substrates have been demonstrated by these technologies. Although >19% is demonstrated, the cost of additional steps is not commensurate with the slight improvement and will not lead to the achievement of <10¢/kWhr LCOE. Therefore there is need to investigate and understand how to form high quality contacts to homogeneous emitters without any additional step. In this study, we used a two step contact approach to achieve high quality contacts to 95-100 Ω/sq emitter. Through contact firing optimization of seed layer and plating, the contact and line resistances were decreased to achieve FF of 79.2%.

2 METAL CONTACTS TO SEMICONDUCTOR

Contacts to semiconductors have been studied in great details as in Schroder [7]. Fig.1 shows the ohmic and non-ohmic contacts to n-type semiconductor with ~1x10^{19} atoms/cm^3 and less than ~1x10^{19} cm^{-3}. The screen-printed emitters usually have phosphorus concentrations in excess of the ~1x10^{19} cm^{-3} to achieve low contact resistance and high FF. The high phosphorus surface concentration reduces the depletion width between the metal/semiconductor, thus increasing the tunneling probality of carriers from semiconductor to metal and vice versa, while the barrier height is invariant. To realize high quality contacts using the screen-printed technology requires understanding of the front silver paste and the cell technology. Most front silver pastes today can make high quality contacts to 65-70 ohm/sq emitters with average efficiency of ≥17% in production. However, the road map for achieving <10¢/kWhr LCOE calls for ≥20% module efficiency, which translates to ≥22% efficient solar cells. To achieve this efficiency target, we need to achieve V_{oc} of ≥650 mV, J_{sc} of ≥39 mA/cm^2, and FF of ≥79%. The emitter sheet resistance of

65-70 Ω/sq still limits the efficiency because of <80% blue response and high emitter dark saturation current. Computer modeling shows that the emitter sheet resistance of >100 Ω/sq with <4% shadowing and >90% blue response can achieve ≥20% efficiency. This will require a front silver paste that can form high quality contacts to achieve ≥79% FF. Although it is challenging to achieve high quality contacts to such emitters, we have attempted in this study to contact emitters with 95-100 Ω/sq sheet resistance using a combination of paste firing and plating.

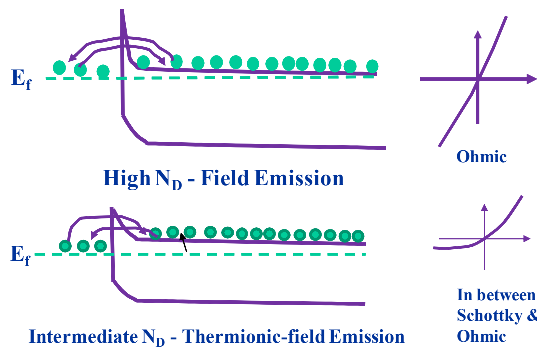

Figure 1: Depletion-type contact to n-type substrate with decreasing doping concentration

3 IMPACT OF GRID LINE WIDTH AND HEIGHT ON CONTACT RESISTANCE AND EFFICIENCY

The line width and height are the two most important parameters for a screen-printed contact. As the line width increases J_{sc} decreases because of the increased shadowing loss. The decrease in J_{sc} is accompanied by lower cell efficiency. However, by reducing the line width without the increase in the line height, shading is decreased but the series resistance increases because of the decrease in grid line cross-sectional area. To raise the J_{sc} and keep low series resistance, we need metal grid lines with high aspect ratio (height to width).

Fig. 2 shows the effect of finger height on the finger resistance for various finger widths. Note that Rf55 refers to a line width of 55 µm in the figure. For a given finger width there is a specific finger height that will produce low finger resistance, high FF and J_{sc}. To achieve high FF the finger resistance should be less than 0.1 Ω-cm as predicted by the model calculation shown in Fig. 2. As the finger series resistance increases the total series resistance increases and the FF decreases.

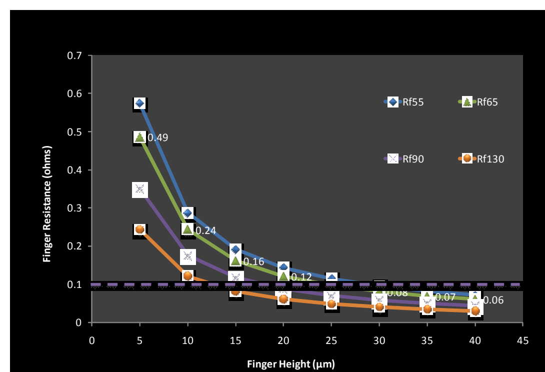

Figure 2: Effect of finger height on line resistance

Fig. 3 shows the effect of line width on J_{sc} and efficiency for cells made on 45 and 100 Ω/sq emitters. In these calculations, we assumed average FF of 79.0% and V_{oc} of 625 mV for the 45 Ω/sq emitter and 79.0% FF and 632 mV V_{oc} for the 100 Ω/sq emitter. J_{sc} decreases with increased linewidth and so does the efficiency. This trend is true for both emitters. However, because of high V_{oc} for cells with 100 Ω/sq emitter, higher efficiencies can be achieved over the low sheet resistance counterparts. That is why it is important to have high sheet resistance emitters to take advantage of the high V_{oc} while maintaining high FF to achieve high efficiency.

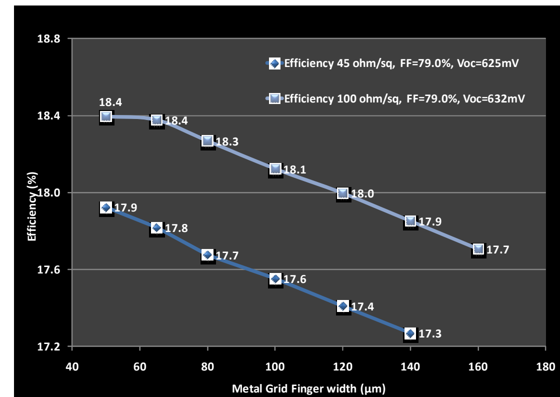

Figure 3: Effect of metal grid line width on effieicncy

4 SCREEN PRINTED TECHNOLOGY LIMIT AND ADOPTION OF INKJET PRINTING

Based on our calculations in Fig. 3, it is evident that the solar cell industry routinely prints linewidths of >100 µm. That is why the average efficiency today is only ~17.2-17.4% even with emitter sheet resistance of 65-70 Ω/sq. However, with some improvement in the print width and higher emitter sheet resistance, average efficiency >17.5% can be achieved. However, at Georgia Tech, we have demonstrated efficiency of 18.4% with line widths of <100 µm and height of 25-35 µm. The metal coverage on these cells, despite these line widths is still high at ~7.8%. This is ~3.8% greater than the required metal coverage to attain the ≥20% efficiency mark. Therefore, there is need for a new technology that can achieve <45 µm line width and ~45 µm tall fingers.

Inkjet is one of the technologies that can deliver this specifications but requires the ink development to contact high sheet resistance emitters. Xjet's inkjet machine is capable of producing fine lines and tall fingers as shown in Fig. 4. Fig. 4 shows a line width and height of 45 µm after firing but the solar cells produced with these finger parameters were not good. The ideality factor was high on all the cells suggesting either the contact firing or the ink was not optimized

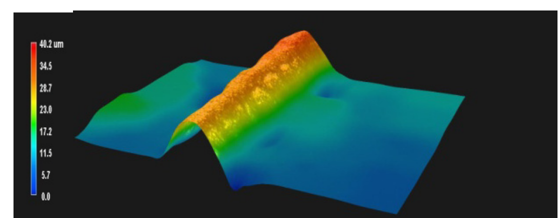

Figure 4: Full ink jetted finger after firing with line width and height of 45-µm.

5 DEVICE FABRICATION

Large area (239 cm^2) commercial Cz silicon wafers of 2.6 Ω-cm resistivity were textured both sides, rinsed in dilute HCl before cleaning in H_2SO_4:H_2O_2:H_2O for 5 minutes, followed by a 3 min rinse in deionized (DI) water. A final dip in 10% HF for 2 minutes was performed, followed by a 30-second rinse in DI water. After the cleaning, the emitters were formed in conventional tube furnace using $POCl_3$ at a set temperature of 855°C, which resulted in a 100 Ω/square emitters. After the edge isolation, the phosphorus glass was removed in dilute HF followed by a DI water rinse. A single layer low frequency PECVD SiN antireflection coating was deposited on the front at 400°C.

The samples were divided into two sets, A and B. Set A was shipped to Xjet Solar for finger seed layers. After the set A cells were returned to Georgia Tech the two sets were printed with an Ag/Al stripes on the back and dried at 200°C followed by a screen-printed Al and dried at 200°C. Next, set B front Ag grid was printed and dried at 200°C. The samples were all co-fired in the IR belt furnace at peak firing temperature of 740-750°C. This was followed by light I-V measurements before LIP. The jetted finger seed layer cells were plated for 10-15 minutes while the SP finger cells were plated for 4-5 minutes in Ag chemistry from Rohm and Haas.

6 FIRING OPTIMIZATION OF THE SEED LAYER

It is important to understand the chemistry of the front metal ink in order to optimize the co-firing process to achieve high quality contacts. The glass frit transition temperature plays a role in setting the peak firing temperature as well as the silver particle morphology. The silver particle can be spheres or flakes or a combination thereof. Depending on the ratio of each silver type, the peak temperature can be low or high (737-746°C). Most importantly, for the homogeneous and shallow 95-100 Ω/sq emitter, silver particles must not diffuse close to the junction. Thus the co-firing process must be such that there is a balance between grid line sintering and dissolution of silver to form the silver crystallite in a very short time (1.5-3 seconds). The contact resistance relies on the uniform wetting and etching of the silicon nitride, and formation of a thin glass layer at the interface of silicon and grid line.

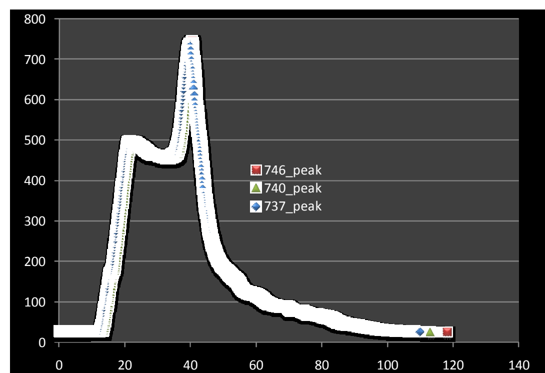

Figure 5: Co-firing profiles showing three peak temperatures

For the seed layer grid lines, the adhesion is affected if etching of the silicon nitride is not complete. Furthermore, during the light induced plating step, when the hydroxyl ions in the presence of water reduce the glass layer at the silicon and grid line interface before Ag is plated to the seed layer, the finger adhesion will be weakened. The fingers will peal because the weight of the plated silver cannot be supported by the dielectric alone without the anchor in silicon, which is either due to the silver crystallites or the glass. Thus, finding the right peak firing temperature is critical. Fig. 5 shows the firing profiles used for contact. Note that the same peak temperature applies to both jetted and screen-printed cells.

7 RESULTS AND DISCUSSION

7.1 Screen-printed and plated solar cells with ~100 Ω/sq emitters

Table 1: Electrical parameters for 2.6 Ω-cm, 239 cm^2 Cz screen-printed finger and plated solar cells with 100 Ω/sq emitters

Cell Name	Area (cm²)	Voc (mV)	Jsc (mA/cm²)	FF	Eff (%)	n factor	Rseries (ohmcm²)	Rshunt (ohmcm²)
100-1	239	631	36.2	0.760	17.4	1.09	1.188	2469
100-2	239	632	36.3	0.767	17.6	1.06	1.119	8564
100-3	239	631	36.3	0.761	17.4	1.06	1.242	4401

Table 1 shows the solar cell results for screen-printed finger and plated solar cells with ~100 Ω/sq and lower phosphorus surface concentration. The V_{oc} of 632 mV shows the effect of emitter sheet resistance as predicted by model calculations. Higher V_{oc}'s, >640 mV, can be achieved with excellent surface passivation. The J_{sc} of 36.3 mA/cm^2 is somewhat low, despite the transparency of the emitter, due to higher shading resulting from plating. However, the FF was only 76-77% because of high contact and line resistances, which were measured as ~15 $m\Omega cm^2$ and ~22 mΩ-cm^2, respectivley.

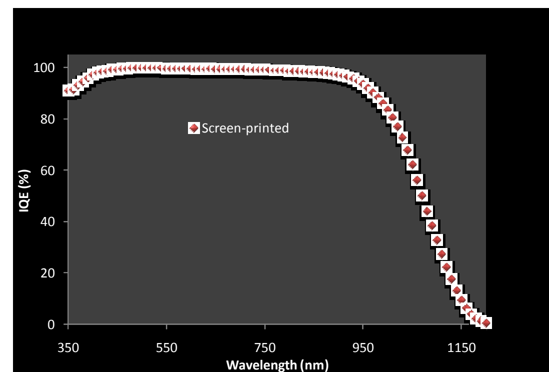

Figure 6: Measured IQE for screen-printed and plated finger solar cells

Figure 6 shows the experimental internal quantum efficiency (IQE) of the 17.6% cell. We used this data in conjunction with PC1D to simulate the front (FSRV) and back (BSRV) surface recombination velocity for this cell. The FSRV of 35000 cm/s and BSRV of 300 cm/s were extracted. Despite the 90% response at short wavelength, J_{sc} is only 36.3 mA/cm^2. This can be attributed to higher shading that result from the non-optimum finger widths after plating.

7.2 Ink jetted seed layer and plated solar cells

Table 2: Electrical parameters for 2.6 Ω-cm, 239 cm^2 Cz jetted seed layer and plated solar cells with 100-Ω/sq emitter

Cell ID	V_{oc} mV	J_{sc} mA/cm^2	FF %	Eff. %	R_{series} (Ω-cm^2)	R_{shun}Ω cm	Comment
38C	**633**	**37.3**	**79.2**	**18.7**	**0.540**	**2438**	**Best***
C	631	37.2	78.5	18.4	0.548	1788	Av. of 12 cells

Table 2 shows the best and average efficiencies for the jetted seed layer and plated solar cells with 100 Ω/sq emitters. Table 2 shows best efficiency of 18.7% and average efficiency of 18.4% compared to only 17.6% shown in Table 1 for the screen-printed and plated finger solar cells. The 1% higher absolute efficiency difference is due to higher J_{sc} (1 mA/cm^2) and FF (2.5%). The higher J_{sc} can be attributed to lower shading by 1.4% resulting from narrower line widths after plating the jetted seed layer and plated cells. The FF difference of ~2.5% in favor of the ink jetted and plated cells confirms the lower contact and line resistance for this contact compared to the screen-printed counterpart. The V_{oc} in both cases are similar confirming the efficacy of high sheet resistance emitter.

In the case of ink jetted seed layer and plated finger, the FF of 79.2% for such high sheet resistance emitter is quite high. This is because both the contact and grid line resistances are quite low. Note that this contact works because of the reducing action of the silver plating solution, which penetrates the entire contact region underneath the grid and reduces the metal oxide glass to metal in addition to plating. In the case of the screen-printed and plated grid lines, the solution can only partially penetrate the contact regions before plating to cover the the screen-printed contact and form a new conduction path.

CONCLUSION

The cost of processing a solar cell can impact the LCOE and therefore the approach to improving the efficiency is important. By using the seed and plate method, high sheet resistance emitters can be contacted with no additional cost. Thus, the gain in efficiency can lead to achieving the <10 ¢/kWh LCOE. However, this requires balancing the understanding of the front silver paste and co-firing conditions in addition to plating to reduce the glass layer and decrease the contact and line resistances. The results shown confirm the efficacy of high sheet resistance emitter with V_{oc} in excess of 630 mV. The short circuit current for the ink jetted and plated finger cells are higher than the screen-printed counterpart because of the increased shadowing resulting from plating of the later. Fill factor of 79.2% suggests the usefulness of very thin lines where the hydroxyl ions in the presence of the plating solution can reduce the glass and decrease the contact resistance before plating to decrease the line resistance.

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SEED LAYER PRINTED CONTACT FORMATION FOR HIGHLY DOPED BORON EMITTERS OF *N*-TYPE SILICON SOLAR CELLS WITH FRONT SIDE JUNCTION

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ABSTRACT: Seed layer printed, fired and plated front side contacts are an industrial feasible high-efficiency technique for *p*-type silicon solar cells with a front side phosphorous-doped emitter. In this work we studied such a contact formation for boron-doped emitters of *n*-type silicon solar cells by applying a jet printed silver seed layer. The contact formation was investigated on shallow, industrial-type as well as on deep, high-efficiency-type emitters by means of specific contact resistance measurements for different firing conditions. Moreover, the emitter shunting has been studied by firing p^+nn^+ test structures at temperatures between 700 and 850 °C. Based on the observed results, p^+nn^+ solar cells have been fabricated, featuring the shallow boron emitter and an unpassivated, fully metalized phosphorous-doped back surface field. Conversion efficiencies up to 20.5% and fill factors of 80.8% could be achieved, demonstrating the effective contact formation to the boron-doped emitter on the device level.
Keywords: *n*-type silicon solar cell, boron emitter, front contact

1 INTRODUCTION

Currently, the PV industry tends to introduce high-efficiency solar cell concepts, including passivated rear surfaces, selective emitters, etc.. However, for high-efficiency solar cell concepts the quality of the base material is becoming more and more important [1]. Hence, phosphorous-doped *n*-type silicon seems to be the material of the choice to benefit the most from the high-efficiency techniques, due to physical advantages of *n*-type silicon compared to boron-doped *p*-type silicon. This advantages are: (i) *n*-type was found to be more tolerant to common metal impurities than *p*-type silicon [2] and (ii) *n*-type silicon does not suffer from the light-induced degradation (LID), which is known for *p*-type Cz silicon due to boron-oxygen complexes [3-5]. With conversion efficiencies of 23% and above the potential of *n*-type silicon has been demonstrated at the device level over years [6-8]. However, *n*-type silicon solar cells with a boron diffused front side emitter have not yet been realized in industrial production, as industrial feasible technologies for their fabrication are still needed. One key issue in this respect is the solar cells' front side passivation and metallization. The current industrial standard front side metallization is based on printing technologies, which usually require a high temperature process for the contact formation. During this high temperature process, the metallization is fired through the dielectric front side coating at temperatures above 650 °C. This implies that a firing stable passivation of the boron emitter is a basic requirement for combining the boron front side emitter with printed contacts.

Thin layers of aluminum oxide (Al_2O_3) grown by atomic layer deposition (ALD) are known to provide an outstanding level of surface passivation on lowly doped *p*-type surfaces [9] as well as on highly boron-doped p^+ surfaces [6, 10]. It was already shown by different authors that the passivation of the Al_2O_3 layers remains relative stable after a typical contact firing processes [11-13], especially on p^+ surfaces [11]. More recently, we have developed a firing stable passivation applicable to front side boron emitters, consisting of a thin Al_2O_3 passivation layer covered by a SiN_x anti-reflection coating [14]. With that layer stack J_{0e} values in the range of 45 fA/cm^2 have been achieved on shallow, industrial-type boron emitters for firing temperatures between 750 and 850 °C. Such low J_{0e} values would allow for open-circuit voltages V_{OC} above 700 mV.

To benefit from that high quality firing stable boron emitter passivation for *n*-type silicon solar cells, a front side metallization is needed that features a low contact resistance to the boron emitter, a high lateral conductivity and very finely structured fingers. In this respect a promising approach is a two-step process [15], where in a first step a fine-line seed layer is produced on the anti-reflection coating (ARC). After firing this seed layer through the ARC for contact formation to the emitter, the seed layer is thickened by a plating step in order to attain the high lateral conductivity. The main advantage of such a two-layer concept is that each layer can be optimized individually. Fine-line printed seed layers in combination with silver plating have been proven to allow for very narrow contact fingers in the range of 50 µm featuring a high aspect ratio [16]. On laboratory *p*-type solar cells, fabricated with this front side metallization technique, conversion efficiencies above 21% have been achieved [17].

The focus of this work is to investigate such a seed layer printed, fired and plated contact formation on Al_2O_3/SiN_x coated boron emitters as a front side metallization for *n*-type silicon solar cells. Therefore, the contact formation of an aerosol jet-printed silver seed layer ink was studied for different firing processes on two different boron emitters: (i) a shallow, industrial-type and (ii) a deep, high-efficiency-type boron emitter. Based on the results, laboratory *n*-type silicon solar cells have been fabricated, featuring a full-area phosphorous-doped back surface field (BSF) on the rear.

2 EXPERIMENTAL

To investigate the seed layer printed, fired, and plated contact formation on boron emitters, the specific contact resistance was measured according to the transfer-length method (TLM) [18]. The contact formation was studied on planar and textured as well as on coated and uncoated emitters. Coated stands for the firing stable Al_2O_3/SiN_x passivation stack [14]. Therefore, samples with TLM structures were fabricated on planar (shiny etched) and

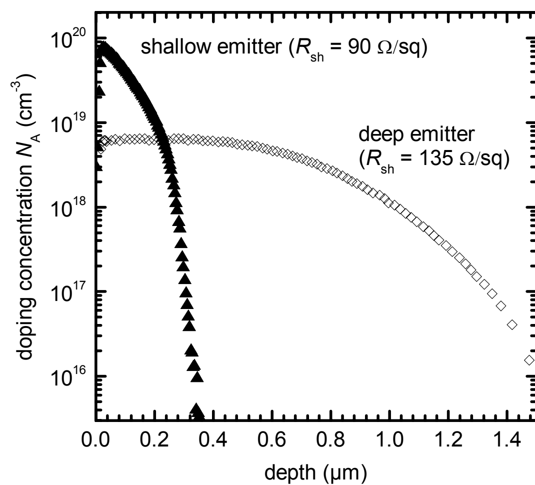

Figure 1: Boron doping profiles of the shallow emitter with a sheet resistance R_{sh} of 90 Ω/sq as well as of the deep emitter (R_{sh} = 135 Ω/sq).

alkaline textured (random pyramids) *n*-type Si wafers with a (100)-oriented surface. Two diffused emitters were applied: (i) a shallow emitter with a high surface doping concentration N_A of ~8×10^{19} cm^{-3} and a sheet resistance R_{sh} of 90 Ω/sq and (ii) a deep boron emitter with N_A of ~6×10^{18} cm^{-3} and R_{sh} of 135 Ω/sq (Figure 1). In the following these emitters are referred to as "shallow" and "deep" emitter, respectively. The boron diffusion was performed in a tube furnace using BBr_3 as diffusion source. The deep emitter was formed by an additional drive-in process. Some of the samples were coated with the passivation stack consisting of 10 nm Al_2O_3 and 60 nm SiN_x. The Al_2O_3 layer was deposited by plasma-assisted ALD, while the SiN_x deposition was performed in an in-line PECVD reactor. After being coated, the TLM structures were printed via aerosol jet-printing of the silver seed ink (developed at Fraunhofer ISE). The contact distances for the TLM structures have been varied between 50 µm and 5 mm. The contact firing was performed in a rapid thermal processing furnace, applying a typical, industrial-like temperature profile with wafer peak temperatures between 700 and 850 °C. Finally, the seed layer was electro-plated with ~10 µm silver.

In order to study the emitter shunting characteristics

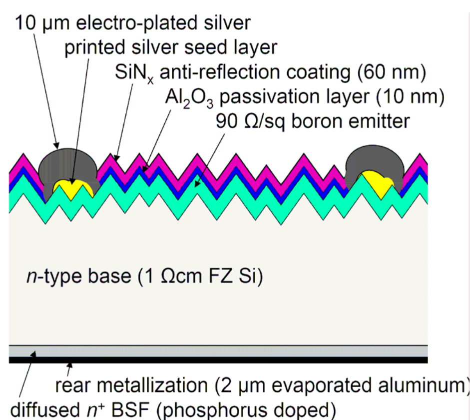

Figure 2: Schematic cross-section of the p^+nn^+ solar cell structure based on *n*-type Si featuring a full-area, phosphorous-doped BSF on the rear.

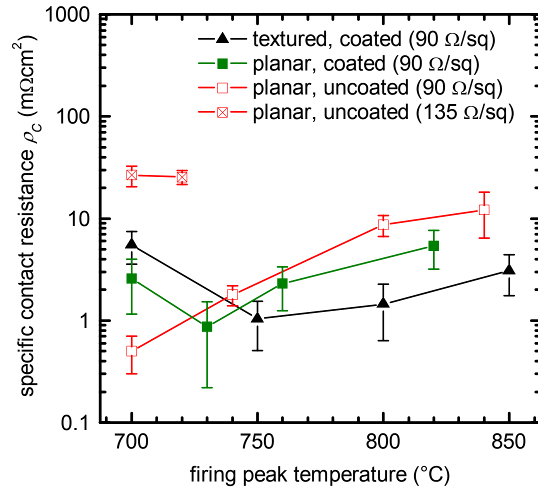

Figure 3: Measured specific contact resistances ρ_c as a function of the wafers firing peak temperature, determined by means of TLM measurements. The TLM measurements were performed on planar (shiny etched) as well as on alkaline textured (random pyramids) surfaces, all diffused with the shallow 90 Ω/sq emitter. Some of the samples are coated with 10 nm Al_2O_3 and 60 nm SiN_x. Besides, measured ρ_c values are shown for the uncoated deep 135 Ω/sq emitter.

of the contact formation, p^+nn^+ test structures were fabricated on *n*-type FZ Si wafers with a thickness of 200 µm and a resistivity of 1 Ωcm. Figure 2 depicts a cross-section of the applied p^+nn^+ cell design schematically. The back side of the test structures was passivated by a Gaussian-shaped, ~2 µm deep phosphorous diffused ($POCl_3$) BSF with a surface doping concentration of ~3×10^{19} cm^{-3}. The BSF was contacted on the whole area by evaporated aluminum. The front side of the p^+nn^+ test structures was fabricated analogously to the TLM structures, featuring alkaline textured surfaces (random pyramids), the shallow emitter diffusion (90 Ω/sq), and the Al_2O_3/SiN_x layer stack. On these test structures the pseudo fill factor *PFF* and the open-circuit voltage V_{OC} was determined for different firing temperatures via the Suns-V_{OC} technique [19].

Finally, 2×2 cm^2 *n*-type solar cells were fabricated analogously to p^+nn^+ test structures featuring the same cell design, see Figure 2. The base material was again 1 Ωcm *n*-type FZ Si wafers with a thickness of 200 µm. The front side grid was adapted to the emitter sheet resistance of 90 Ω/sq as well as the respective contact parameters (e.g. specific contact resistance, finger width, etc.) by using the software Gridsim (developed at Fraunhofer ISE). Thus, on the final solar cells a finger distance of 1.25 mm was applied.

3 CONTACT FORMATION ON BORON EMITTERS

As the reaction energy for the contact firing is primarily adjusted by the firing peak temperature, this temperature is one of the most crucial process parameter for the contact formation. Thus, the specific contact resistance ρ_c was studied for different firing peak temperatures between 700 and 850 °C. Figure 3 shows the ρ_c values obtained on both, the shallow and the deep emitter for the different surface structures. As can be seen, by applying the silver ink on the shallow 90 Ω/sq

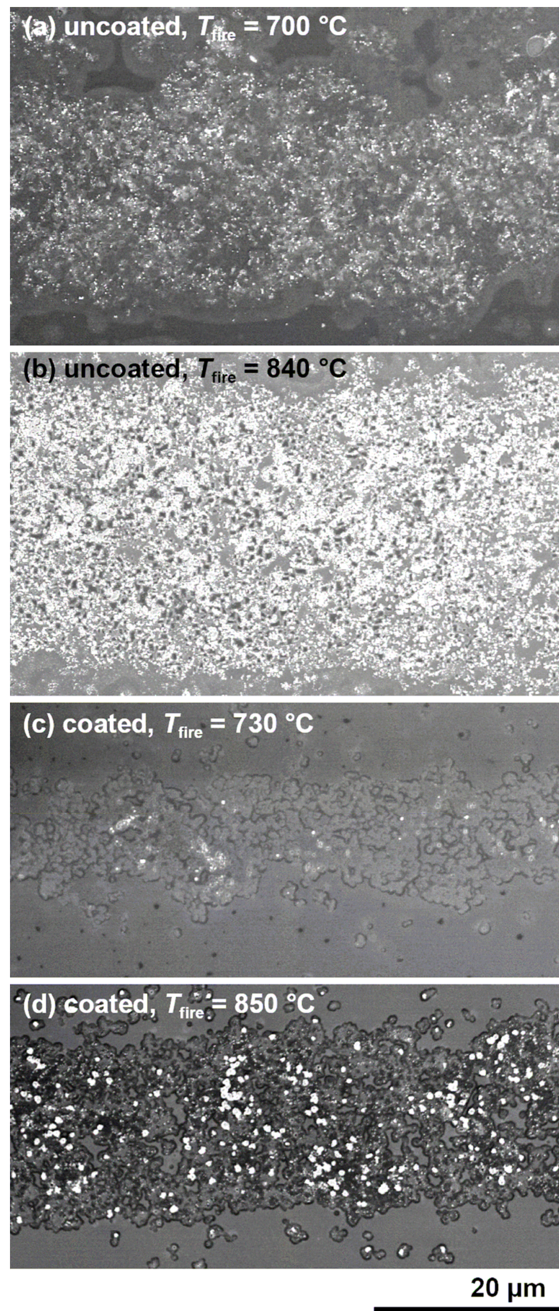

Figure 4: SEM top view on the contact interface of seed layer lines on uncoated [(a) and (b)] and coated [(c) and (d)] emitters, after contact firing at low temperatures in the range of 700-730 °C [(a) and (c)] and at high temperatures in the range of 840-850 °C [(b) and (d)]. Coated stands for the 10 nm Al_2O_3 and 60 nm SiN_x layer stack. The samples feature a planar, (100)-oriented surface, all diffused with the shallow 90 Ω/sq emitter. The SEM micrographs were taken after etching back the contact metallization and subsequently the glass at the contact interface. The bright areas are the Ag crystallites.

emitter (surface concentration N_A of ~8×10^{19} cm^{-3}), very low ρ_c values in the range of 1 mΩcm² and below were achieved for all surface structures. In the case of the coated emitters an optimum firing temperature at about 750 °C was observed. By applying the silver ink on the deep 135 Ω/sq emitter featuring a low surface

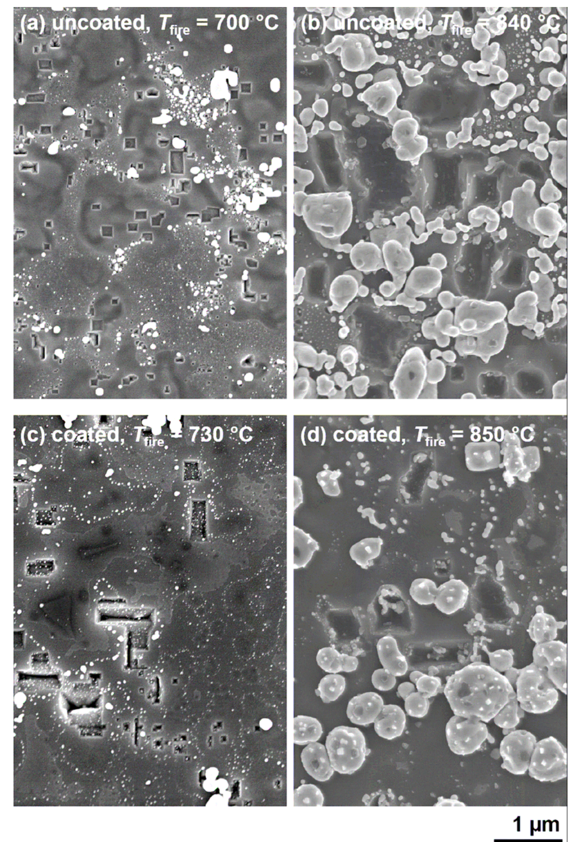

Figure 5: Detail SEM top view micrographs of the contact interface for the same samples shown in Figure 4. Again, the bright areas are Ag crystallites whereas the dark, rectangular-shaped regions are the imprints of missing Ag crystallites. Especially in the case of (c), the micrograph was taken from an Ag crystallite rich part of the seed layer.

concentration of ~6×10^{18} cm^{-3}, a rather high ρ_c of 25 mΩcm² was obtained. Since no adequate ρ_c was achieved for the deep emitter, the following work is focused on the shallow emitter.

In order to attain a microscopic view of the contact formation, scanning electron microscopy (SEM) images have been taken from fired contact interfaces. For that purpose the metallization as well as the glass layer, which is present at the fired contact interface, were removed from the TLM structures by wet-chemical etching. Figure 4 shows overview SEM micrographs from the contact interface of seed layer line sections with either an uncoated or coated emitter, each fired at a low firing temperature in the range of 700-730 °C and a high firing temperature in the range of 840-850 °C. All micrographs were taken on samples, featuring a planar surface and the shallow emitter diffusion (90 Ω/sq). Detail SEM micrographs of the same samples are shown in Figure 4. The bright areas in the micrographs are Ag crystallites whereas the dark, rectangular-shaped regions are imprints of missing Ag crystallites. From the overview SEM micrographs it can be seen, that the widths of the seed layer lines of the different samples ranges from 15 µm to 30 µm due to slightly differing printing parameters. However, the printed seed layer thickness was not affected significantly by the slightly differing printing parameters and thus the observed crystallite formation

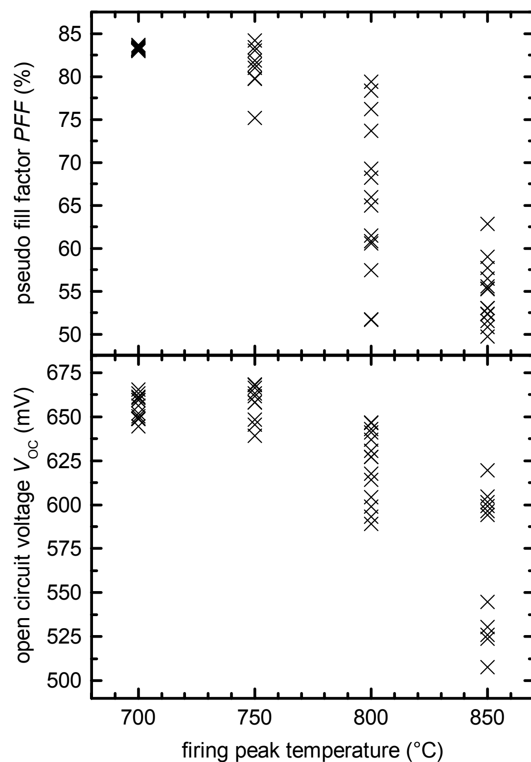

Figure 6: Open-circuit voltage V_{OC} and the pseudo fill factor *PFF* as a function of the firing peak temperature measured at the p^+nn^+ test structures. The values were measured with the Suns-V_{OC} technique.

should not be affected, too. The overview SEM micrographs show the distribution of the Ag crystallites over the fired seed layer. A homogenous distribution was obtained for the uncoated samples (Figure 4a and b), where especially for the high firing temperature of 840 °C almost the hole seed layer area is covered by Ag crystallites. The same firing temperature dependent Ag crystallite formation on planar uncoated samples was found for the deep boron emitter. In contrast to the uncoated emitters, the coated sample fired at 730 °C (Figure 4c) shows only very few clusters of Ag crystallites, whereas the coated sample fired at 850 °C (Figure 4d) shows a higher crystallite density.

The fact that on the coated emitter the crystallite formation tends to be much weaker for decreasing firing temperature explains the increased contact resistance obtained on the coated emitters for low contact firing temperature. The reason for that weak crystallite formation is, that the reaction between the ink, in particular with the glass frit, and the SiN_x was found to start at temperatures of ~680 °C [20] and hence, the low firing temperature of 700 °C is most likely not sufficient to fire the seed layer through the Al_2O_3/SiN_x stack adequately. However, for the coated TLM sample fired at 730 °C a ρ_c of 0.9±0.7 mΩcm² was measured, which seems to be rather low for the very low density of Ag crystallites observed from Figure 4c. To get a more quantitative view, a rough estimation of the Ag crystallite coverage was made by taking the total contact width after plating of ~35 µm into account, which was also used for evaluation of the TLM measurements. The Ag crystallite coverage was estimated to be ~1% by pixel counting at the SEM images. Such a low Ag crystallite coverage is a typical value for printed and fired Ag contacts to phosphorous-doped emitters [21, 22]. The low Ag crystallite coverage indicates that the real contact resistance of the rather small contact area of the Ag crystallites is about two orders of magnitude lower than the measured value. According to the calculations of Schroder *et al.*[23], the specific contact resistance of an ideal Ag / p^+ Si contact is around 1×10^{-4} mΩcm² for $N_A = 1\times10^{20}$ cm^{-3} and a barrier height φ_b of ~0.5 eV, which is even lower. It is worth mentioning, that for the estimation of the coverage the vertical component of real contact interface area of the pyramidal-like shaped Ag crystallites was neglected. Even if a rough estimation was made, this very low specific contact resistance of the Ag crystallites shows that with Ag as contact metal an excellent low-resistive contact to the highly doped boron emitter is possible for firing through the Al_2O_3/SiN_x layer stack.

From the detail SEM micrographs of Figure 5 it can be obviously seen that the higher the firing temperature the stronger is the reaction, which leads to more and larger Ag crystallites. Concerning the contact resistance, which was found to increase with increasing firing temperature, this seems to be a surprising result. However, this behavior can be explained by having a closer look at the chemical reactions involved in the contact formation [16, 20]: during the firing process, oxygen from glass frits (PbO) and silicon from the SiN_x layer react to glass (SiO_x). This glass forms an insulating layer at the contact interface, which insulates silver crystallites (metal / semiconductor interface) from the bulk silver of the contact. With increasing firing temperature the amount of generated glass increases too since more SiN_x is opened (see Figure 4c and d) and hence more Si from the SiN_x reacts with the glass frit to SiO_x. This could mean that the insulation of the silver crystallites is increased as well. If so, there are two contrary reactions, the formation of Ag crystallites simultaneous to their insulation due to the formation of glass. This reaction characteristic would describe the existence of an optimum contact firing temperature between 700 and 800 °C as observed.

As can also be seen from the detail SEM micrographs of Figure 5, the firing temperature has a strong impact on the lateral size of the Ag crystallites. Even if it is not possible from the SEM micrographs to determine a penetration depth of the Ag crystallites into the emitter, shunting could be assumed to be an issue for the high firing temperatures. Therefore open-circuit voltage V_{OC} and pseudo fill factor *PFF* were studied as a function of the firing peak temperature on the p^+nn^+ test structures. As can be seen from Figure 6, for firing temperatures of 750 °C and below, V_{OC} values up to 660 mV were achieved. Those values are close to the maximum V_{OC} of ~665 mV that can be reached with this type of full-area BSF cell structure (Figure 2). The maximum V_{OC} of the cell structure was simulated by the use of PC1D [24] assuming an ideal front side passivation. From the reduced *PFF* values for firing temperature of 800 °C and above, it can be concluded that a significant emitter shunting occurs at those temperatures. The emitter shunting also affects the V_{OC} above 750 °C, which is reduced strongly. Nevertheless, at firing temperatures of 750 °C, which were found to be well suited for solar cell fabrication due to the low contact resistance, no significant shunting was observed.

4 SOLAR CELL RESULTS

Based on the results described in the previous section p^+nn^+ solar cells have been fabricated by applying the shallow 90 Ω/sq emitter, on which low specific contact resistances have been achieved. For that emitter the lowest contact resistances were achieved at firing temperature around 750 °C and emitter shunting was found to begin at 800 °C. Therefore, the contact firing of the solar cells was performed with peak temperatures between 720 and 780 °C. Table 1 summarizes the *I-V* parameters of our most recent cell batch [25]. Listed are the results for the best solar cell of each firing temperature. Besides the *I-V* parameters, the pseudo fill factors *PFF* measured with the Suns-V_{OC} technique are also listed. The achieved conversion efficiencies η in the range of 20%, with a maximum of 20.5% for the cell fired at 720 °C, have reached very high values for the applied p^+nn^+ cell design. Most important, however – with respect to the fired surface passivation as well as the fired front side contact formation – are the high values achieved for V_{OC} and *FF* at the device level. The V_{OC} of about 654 mV is close to the maximum achievable V_{OC} for this cell design (compare previous section). Moreover, the high *FF* of 80.8% demonstrates the excellent contact formation of the silver seed layer ink to the highly doped boron emitter. That high *FF* values came along with low series resistances $R_{s,light}$ in the range of 0.5 Ωcm², determined by comparing the one-sun with the dark *I-V* curve [26]. For the *PFF*, which is a good measure for the junction quality after firing, values above 83% independent of the applied firing temperatures between 720 and 780 °C were observed. This reveals that the shallow boron emitter was not shunted during the contact formation for all applied firing temperatures. That wide range of applicable firing temperatures indicates a wide and stable process window for the contact firing process.

5 CONCLUSIONS

Concerning an industrial feasible front side metallization for *n*-type silicon solar cells with front side junction, the contact formation of a printed, fired and plated silver seed layer ink to boron emitters was studied. The specific contact resistance ρ_c was measured as a function of the contact firing temperature for both, a shallow as well as a deep boron-doped emitter. For the deep emitter (surface concentration N_A of ~6×10^{18} cm^{-3}) a rather high ρ_c of 25 mΩcm² was obtained, whereas very low ρ_c values in the range of 1 mΩcm² were achieved for the shallow emitter (N_A of ~8×10^{19} cm^{-3}), even for firing through the Al_2O_3/SiN_x passivation stack. The emitter shunting was studied on the shallow emitter as a function of the firing temperature with p^+nn^+ test structures. Considerable shunting has been observed for firing temperatures of 800 °C and above. Finally, p^+nn^+ solar cells (2×2 cm²) have been fabricated on 1 Ωcm, phosphorous-doped FZ silicon. Conversion efficiencies up to 20.5% and fill factors of 80.8% have been achieved, which is a very high level for solar cells with an unpassivated, fully metalized phosphorous-doped back surface field. The high fill factor level demonstrates the potential of the investigated front side metallization at the device level.

Table 1: One-sun *I-V* parameters of the fabricated 2×2 cm² p^+nn^+ solar cells for the different firing peak temperatures T_{peak}, measured under standard testing conditions (AM1.5g, 100 mW/cm², 25 °C). In addition, the pseudo fill factor *PFF*, measured with the Suns-V_{OC} technique, is also given. Tabulated are the results of the best cell for each firing temperature. The solar cells were fabricated on 1 Ωcm phosphorous-doped FZ Si wafers with a thickness of 200 µm.

T_{peak} (°C)	*PFF* (%)	V_{OC} (mV)	J_{SC} (mA/cm²)	*FF* (%)	η (%)
720	**83.7**	**654.3**	**38.7**	**80.8**	**20.5**
740	**83.7**	**654.2**	**38.8**	**78.8**	**20.0**
760	**83.6**	**653.6**	**38.8**	**80.6**	**20.4**
780	**83.7**	**652.2**	**38.2**	**79.5**	**19.8**

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COPPER AS CONDUCTING LAYER IN THE FRONT SIDE METALLIZATION OF CRYSTALLINE SILICON SOLAR CELLS – CHALLENGES, PROCESSES AND CHARACTERIZATION

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ABSTRACT: The use of copper for silicon solar cell front side metallization has been investigated, focusing on the use of printed silver seed layers to contact the substrate. Screen-printed and aerosol-printed seed layers have been used, in order to keep the overall process close to the current industrial standard. Suitable plating processes, using techniques such as electroless or light-induced nickel plating for diffusion barrier formation, and light-induced copper plating for conducting layer formation, have been identified. Solar cell efficiencies of 20.3% on FZ-laboratory cells (2x2cm²) and 17.2% on Cz industrial-type material (5x5cm²) have been achieved. The long term stability of the solar cells has been evaluated, particularly regarding the requirements on the barrier layer deposition process. The corresponding estimations gave expected solar cell long term stabilities of more than 100 years with less than $5\%_{rel}$ performance loss for the most promising metal stack systems.

1 INTRODUCTION

Besides the silicon wafer, the metallization of solar cells is the most important cost factor in today's industrial solar cell production (~30% of the total cell processing cost) due to the use of expensive contact pastes, particularly silver-containing pastes for the front grid.

In order to reach grid parity for photovoltaic solar energy conversion, combined efforts are made to reduce the manufacturing costs for crystalline silicon solar cells while at the same time increasing their efficiency. In this context, increasing the typical cell size has led to a demand for an advanced front side metallization, in order to keep series resistance losses at a low level. A two-step concept, similar to the front side metallization of high-efficiency laboratory solar cells has been shown to exhibit various advantages [1]. Process schemes with fine line printed seed layers and light-induced plating (LIP) of silver are already close to industrial introduction [2].

Table 1: Properties of different metals considered for solar cell metallization

	Silver	Copper	Nickel
Conductivity [10^6 S/m]	61,39	59,1	13,9
ρ [g/cm³]	10,49	8,92	8,9
Costs (2 year mean) [€/kg]	388,8	4,1	12,8

While these approaches mainly address an increased efficiency, an advanced front side metallization may additionally lower the cell production costs. Many efforts have been made to replace the relatively expensive silver by cheaper and almost equally conductive copper (see table 1). The major disadvantage of copper is its high mobility in silicon, combined with its property as a highly active recombination centre (as copper containing precipitates) in solar cells [3]. Therefore, its penetration into the solar cell must be prevented with a diffusion inhibiting intermediate layer. The functionality and industrial viability of such a contact system has been proven in a cell process by BP solar with laser grooved buried contacts consisting of a nickel layer (seed and barrier) and a copper layer (main conducting layer) [4].

In order to enable the use of copper as main conducting material and thus reduce the cell manufacturing costs, processes need to be developed and evaluated. The resulting contacts need to exhibit good optical, electrical and mechanical properties and the cells need to be long term stable. Therefore, metal layers with suitable thickness have to be deposited homogenously and by an industrially viable route. Also, other cell properties (e.g. anti-reflexion coating, edge isolation) or the corresponding process steps may be required to be optimized if copper is introduced.

All different routes to create solar cell front contacts have certain characteristics in common: A penetration of the anti-reflexion coating (ARC) is needed, in order to form an electrical contact to the emitter. On top of this contact area, a metal layer of sufficient lateral conductivity is required. In standard solar cells with silver screen printed front side metallization, the printed paste fulfils both, the conducting and opening (during contact firing) task. Advanced metallization techniques separate these steps in order to allow an optimization regarding different desired solar cell properties. An ARC-ablation step is followed by the application of a metal layer (e.g. by evaporation or direct plating) and a subsequent thermal treatment. While these techniques have a very high potential regarding cell efficiency, they are currently not elaborated as far as to allow for an extensive industrial introduction due to economical or technological constraints. One step in between is the combination of both, a fine line printed and fired seed layer, plated with nickel as a diffusion barrier and copper as a cost effective alternative to silver. Here, the ablation and contact formation steps are done in one single process, during contact firing. The main advantages of this seeding technique are the simplicity of the process, together with the knowledge and robustness which has been gained in years of industrial experience. Therefore, a working process with such a seed layer is believed to have a very high potential to be accepted and introduced into industrial lines. If novel printing techniques like aerosol-printing [5] or metal inkjet-printing are used, the amount of silver can be kept very low (compare Fig. 7).

A schematic image of such a contact structure is shown in Fig. 1.

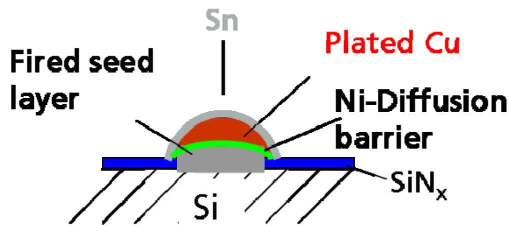


Figure 1: Schematic image of the solar cell front contact structure discussed in this paper.

2 EXPERIMENTAL

For the plating experiments, we used different solar cell substrates with either aerosol-printed seed layers [5] or screen printed seed layers. For most experiments, solar cell test structures as described in [6] were used. The plating of nickel and copper was carried out in an experimental setup as schematically shown in Fig. 2 and which is described in more detail elsewhere [6]. Separate setups were used for the different metals and deposition methods (light-enhanced electroless nickel deposition, light-induced electrolytic nickel deposition, light-induced copper deposition, light-induced silver deposition). The cells used in our experiments were fabricated with a PECVD SiN_X-ARC. It is worthy to mention that we did not experience any problems with "background"-plating on the ARC, which has been reported especially in the context of nickel plating.

The used electrolytes are commercially available silver, copper and electroless nickel plating solutions, and a simple Watts type nickel electrolyte for LIP set up in our labs. Temperature and electrolyte properties were kept constant between all experiments and according to the manufacturer's specifications. Potentials and currents were applied and measured by either using a versatile multichannel potentiostat (VMP, Bio-Logic) for the silver deposition experiments, or a programmable source measure unit (Keithley) with a coupled power amplifier. Temperature stress experiments were carried out using an ordinary hotplate with programmable control unit. The pseudo fill-factor (pFF) measurements were made with the Suns-V_{OC} technique as described by Sinton and Cuevas [7], using the generalized analysis type with temperature correction to 25°C.

3 CHARACTERIZATION OF BARRIER LAYERS

In order to enable an interpretation of the long term stability investigation, the diffusion barrier layer properties were evaluated by SEM imaging prior to copper deposition. Similar investigations were made for aerosol-printed and screen printed seed layers, the images shown in this paper are all on aerosol seeds for comparability. The results obtained on screen print are similar.

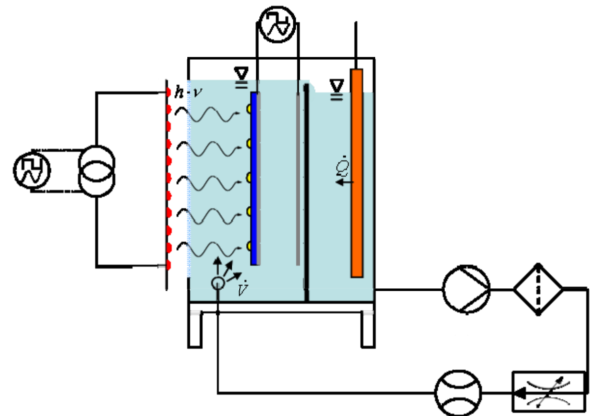


Figure 2 Schematic image of the used plating equipment

Barrier layers were deposited with light-induced nickel plating and electroless nickel plating. Schematic images of the process principles are shown in Fig. 3. The electroless plating process works only on catalytically active surfaces, especially certain metals. Thus, deposition will occur only on the printed silver seed layer. The LIP process works on all parts of the grid that have an electrical connection to the cell and are therefore negatively polarized under irradiation. Nickel is reduced on such surfaces by excited electrons which originate from the cell.

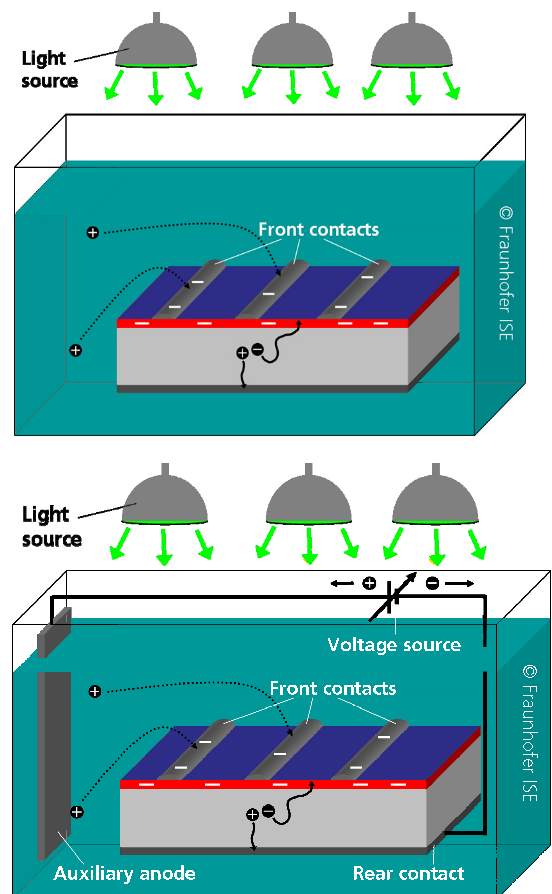


Figure 3: Schematic images of the light supported electroless plating (upper image) and light-induced plating (lower image)

The requirements of the nickel layers are sufficient thickness and homogeneity over the entire front side grid. As soon as copper is prevented from entering the cell for the desired lifetime, the diffusion barrier layer is adequate. However, the thinner the nickel layer, the better, as the conductivity of nickel is rather low compared to copper, and the contact is desired to consume as little metal as possible, for economical (reduction of material consumption) and optical reasons (no excess plating). An estimation of the lifetime can be made with an accelerated ageing procedure Here, the diffusion is amplified by exposing the cell to thermal stress, and the loss in junction quality (due to copper penetration) is monitored by measuring the pseudo fill factor. The estimation of the lifetime is achieved by plotting the degradation data into an Arrhenius-diagram. The method is described in more detail elsewhere [8].

In order to optimize the nickel layer thickness, first experiments were carried out choosing rather long plating durations (up to 900s) in the electroless plating bath, to obtain very thick and homogenous nickel layers. These layers were expected to exceed the requirements for the long term stability, which is the key property for each metal stack. However, the SEM characterization of these layers revealed an insufficient integrity (Fig. 4). Apparently, nickel layers deposited with the chosen system exhibit a high internal stress, which causes the deposited metal to lift of the seed if it becomes too thick. Thus, the layers were firstly optimized regarding this behaviour. A reduction of the plating time led to better results, as can be seen in Fig. 5, upper image (540s plating time) and Fig. 5, lower image (460s plating time). The metal layer adheres to the seed over the whole cell, but there are still some cracks visible. In general, the number of cracks is reduced with shorter plating times.

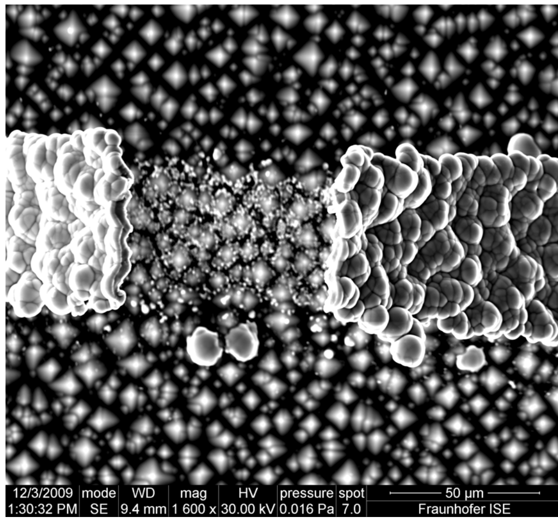


Figure 4: SEM image of a nickel layer plated on top of an aerosol seed layer (light supported electroless plating), 900s plating duration.

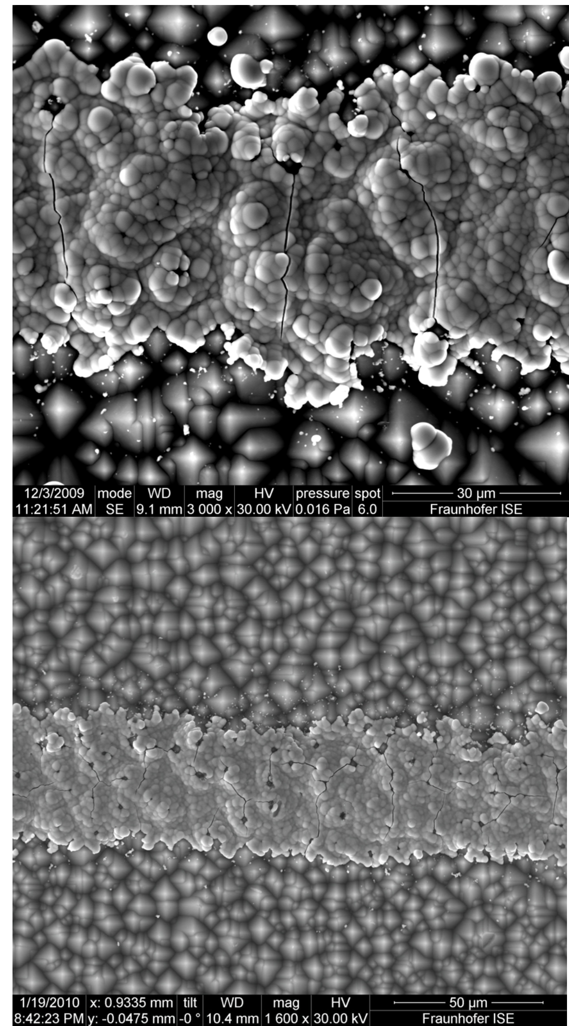
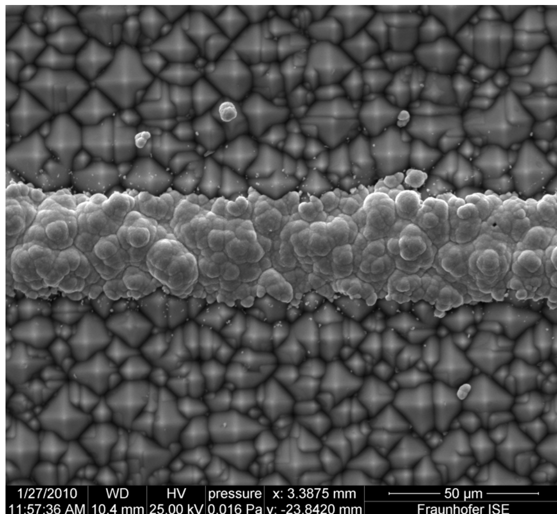


Figure 5: SEM images of a nickel layers plated on top of an aerosol seed layers (light supported electroless plating). Upper image: 540s plating duration. Lower image: 460s plating duration.

For seed layers plated with the Ni-LIP process, a similar characterization was made. A variation of protective potential and time showed that a dense nickel layer could be deposited quite homogenously in less than 180 seconds (Fig. 6, upper image). However, some areas of the cell remained poorly plated, probably due to inhomogeneities of the printed seed layer (Fig. 6, lower image). A further optimization of the seed layer is needed to fix this issue. The nickel layer which was selected for the degradation experiment was deposited in 300 seconds. Compared to the deposition from the electroless process, the LIP nickel shows no cracks even for longer deposition times.



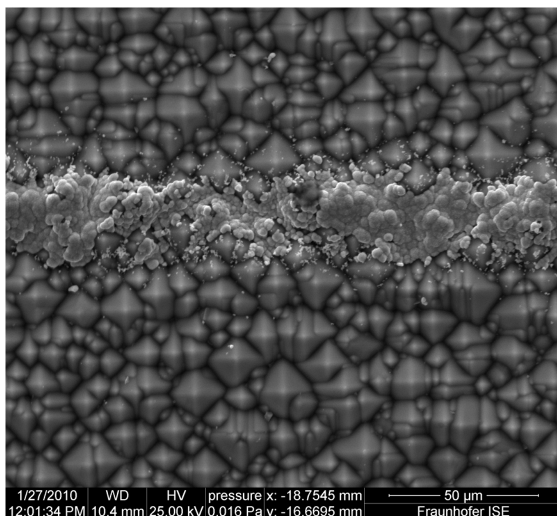


Figure 6: SEM images of a nickel layer plated on top of an aerosol seed layer (nickel-LIP), 300s plating duration. Upper image: Full coverage. Lower image: not fully plated.

4 COPPER DEPOSITION PROCESS

The solar cell contacts were finished by copper and tin plating, in order to achieve a sufficient lateral conductivity. A cross sectional SEM image with a corresponding EDX analysis can be seen in Fig. 7. The amount of silver that is used for such a contact is very little, especially if an aerosol-printed seed layer is used (approx. 5mg Ag for a 156x156mm² wafer).

However, rough surfaces like the random pyramids of monocrystalline silicon solar cells are not trivial to plate with copper. Sharp features on substrates for electrodeposition are known to be spots of increased field density. Moreover, the mass transport to such exposed sites may be superior, leading to predominant deposition there [9]. Especially for the aerosol seed layers, we had to develop a pulse plating process in order to achieve copper layers of good quality, i.e. homogenous layer thickness and high conductivity. Direct plating on such a surface was found to result in very inhomogenous plating results (Fig. 8). Optimized direct current plating processes are easier to realize and may lead to similar results, and are currently investigated. Also, a combination of pulsed and direct currents is possible, Once the substrate is relatively homogenous (after some time of pulse plating, or if the seed layer is screen printed), a direct current process can be applied.

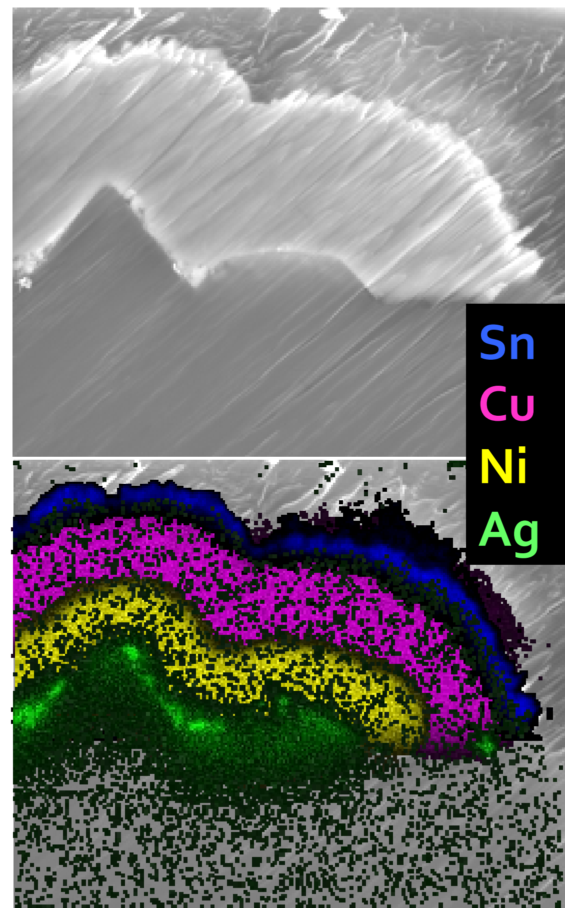


Figure 7: Cross sectional SEM and EDX analysis of a contact structure with nickel, copper and tin plated on top of an aerosol Ag seed layer.

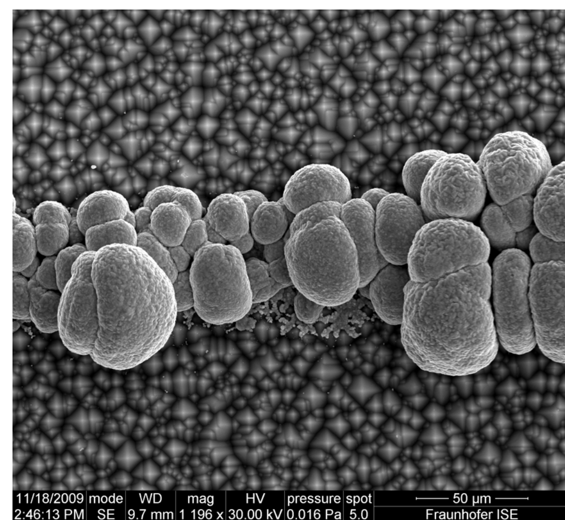


Figure 8: SEM image of a copper deposition result on an aerosol seed layer with nickel, after direct current copper plating.

5 SOLAR CELL RESULTS

The replacement of silver with copper means exchanging one highly conductive material with another. The intermediate nickel barrier layer is not expected to introduce any significant transfer resistance. Accordingly, the solar cell performance should be comparable.
A front side metallization stack consisting of an aerosol-printed and fired seed layer, a barrier layer deposited by light-supported electroless nickel plating and a conducting layer created by copper (LIP) was tested on high efficiency cells. These were made of 4'' FZ silicon wafers (0.5 Ω*cm), a 110 Ω/sq shallow emitter, passivated rear and front side and laser fired contacts (LFC). The cell size was 2x2 cm². The best cell we obtained had an efficiency of $\eta = 20.3\%$ and a FF of 80.8% (see table 2), which was comparable to the reference with aerosol-printed seed and silver-LIP. This result shows the high potential of the metallization system.

Table 2: Solar cell result on 2x2cm² high efficiency substrate with aerosol-nickel-copper-tin metallization demonstrating the potential of this concept.

V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]
646.4	**38.86**	**80.8**	**20.3**

In a second batch of experiments, we used test structures with a size of 50x50 mm² that were cut out of 156x156 mm² Cz Wafers using a dicing saw. The samples have a shallow emitter with a sheet resistance of $R_{SH} = 65$ Ω/sq, passivated by an SiN_x ARC-layer, full rear BSF and an aerosol-printed seed layer as described in [5]. These industrially produced standard solar cell samples have been used for the optimization of plating processes in our lab for some time. The efficiencies achieved with the described nickel-copper-tin stack are in the same order of magnitude as for equally processed cells with aerosol + silver-LIP metallization (table 3). The use of a nickel layer deposited by LIP instead of electroless plating had no influence on the cell performance.

Table 3: Solar cell result on 5x5cm² Cz test substrates with different metallization systems, based on printed and fired seed layer

	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]	η [%]
Aerosol-Ni-Cu-Sn (average of 9 cells)	613.8	35.74	74.9	16.4
Aerosol-Ni-Cu-Sn (best cell)	616.8	35.69	76.2	16.8
Aerosol-Ag-reference group (best cell)	607.2	35.75	76.2	16.5

A batch of solar cells using a Cz substrate of improved quality was used in another experiment, using screen printed seed layers. The efficiency that could be achieved was up to 17.2%, with a short circuit current density of 35.1 mA/cm². A comparison to similar cells with an aerosol-seed + silver LIP system as front side metallization shows these cells to have a potential to reach up to 17.7 % efficiency (j_{SC}=36.7mA/cm²). An experiment with an aerosol-seed finished with a nickel copper tin stack is under preparation. A similar efficiency potential is expected.

Table 4: Solar cell result on 5x5cm² Cz test substrates (improved material quality) with different metallization systems, based on printed and fired seed layer

	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]	η [%]
Aerosol-Ag reference (average of 4 cells)	614.2	36.4	78.4	17.5
Aerosol-Ag (best cell)	614.1	36.7	78.4	17.7
Screen-print Ni-Cu-Sn (best cell)	615.2	35.10	79.5	17.2

6 LONG TERM STABILITY EVALUATION

As shown, the efficiency potential of the investigated metal systems for the front side metallization is equal or even higher than for systems that are currently standard in industrial application. The key to a possible introduction is the proof of the long term stability of such a system. The degradation method, applying thermal stress to solar cells, has been used on several stack systems described above. Temperatures between 150°C and 275°C have been used. Fig. 9 shows the evolution of the pFF over time at thermal stress at 200°C for all the investigated metallization systems. The effect of the nickel barrier layer is clearly visible. Samples without diffusion inhibiting layer degrade much faster than corresponding samples with similar seed layer + plated nickel.

However, there are important differences between the different nickel processes. On an aerosol-printed seed layer, the barrier deposited in an electroless process acts far more effective than the barrier from the LIP-process. This behaviour was found not only for 200°C, but also for all other temperatures investigated. The estimated lifetime (Fig. 10) for the LIP-processed cells is consequently lower. This is unexpected, as the deposited layer from the LIP process was found to have better properties in the SEM analysis. A possible explanation for this behaviour can be found in the partly interrupted coverage of this Ni-layer (Fig. 6, lower image). Whereas the aerosol-seed is not entirely plated by the LIP process, due to some areas with increased contact resistance to the cell, the electroless process plates nickel to all parts of the metallic seed layer, regardless of the connection to the solar cell. This theory is supported by the behaviour of the LIP barrier layer on screen printed silver, which was found to give the best long term stability estimation in our investigation. For this seed layer, even parts of the grid that may have a higher contact resistance to the cell are connected to better connected parts by a layer of good conductivity. Thus, these parts also adopt a negative potential, which allows a homogenous plating result over the entire solar cell. However, the degradation of these cells was so slow (especially at low temperatures), that a reliable quantitative estimation of the long term stability was difficult. The hollow symbols in Fig. 10 are data points that were extrapolated from the degradation

experiments, as the reduction to 95% pFF was not achieved during thermal exposure times of up to 1000 h. Thus, an estimation for the system screen print + Ni-LIP + Cu was not made. For the system aerosol-print + electroless nickel + copper, the estimation is 5%$_{rel}$ pFF-loss in several hundred years.

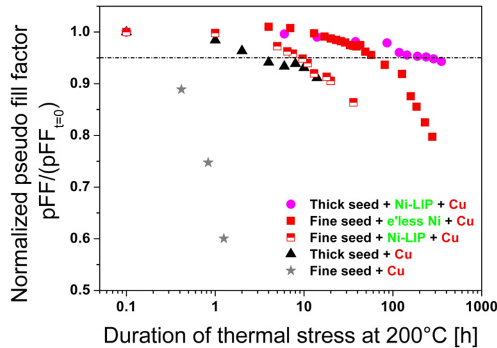


Figure 9: Degradation behaviour under 200°C of thermal stress for different metal stack systems containing copper.

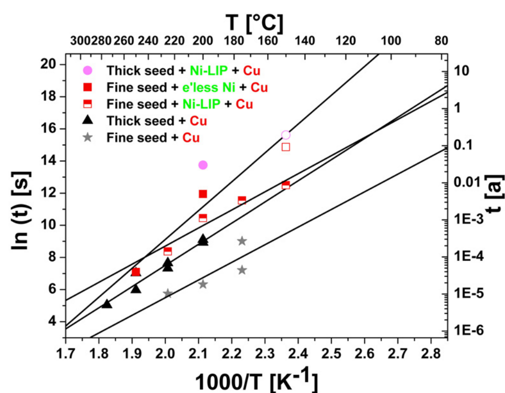


Figure 10: Arrhenius diagram for the tested metal stacks, with extrapolation of the degradation duration to 95%$_{rel}$ pFF at a constant thermal exposure of 80°C.

7 CONCLUSION

Suitable processes to create stack systems of nickel as diffusion barrier, copper and tin on top of printed and fired seed layers haven been developed. The efficiencies of the resulting solar cells are, as expected, in the same order of magnitude as with a comparable metallization which is fully based on silver. It is of course crucial that the copper layer is plated uniformly, which can be difficult, especially on rough surfaces. A pulse plating process has successfully been applied to get high quality copper deposits. The layer thickness and the homogeneity, especially of the diffusion barrier layer, have been found to be critical regarding good long term stability. Plated nickel layers deposited with an electroless plating process have been found to be sensitive to internal stress, resulting in cracks and peeling off of the metal. This behaviour was found to be proportional to the plating thickness. Layers plated with nickel LIP were found to be less sensitive to this phenomenon. However, these layers may require some more building up of the seed layer, in order to plate uniformly. Further development in this direction is currently carried out in our labs. For solar cells with electroless nickel plating on top of aerosol seed layers, lifetime estimations indicate a lifetime limitation due to copper penetration into the solar cell of >100 years, which is more than sufficient. On screen printed seed layers, even longer stability is expected, although no reliable extrapolation could be made to date. We are working further on improving our evaluation of the lifetime estimation, addressing also other remaining issues, like adhesion improvement and parasitic plating (e.g. at cell edges).

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OPTIMIZATION OF ELECTROLESS NICKEL PLATING FOR FRONT SIDE SILICON SOLAR CELLS METALLIZATION

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ABSTRACT: The aim of the present work is to study the results of a two-step front contact process consisting of a thin electroless nickel-phosphorus (NiP) seed layer thickened by electrolytic deposition of silver. The electroless NiP layer was deposited from an alkaline bath containing sodium hypophosphite as a reducing agent and ammonia for pH control. It can be used as a seed layer because it ensures the required adherence, a low contact resistance and prevent copper from diffusing into the silicon. Typical contact resistivities of 10^{-4} Ω.cm^2 have been obtained by Transmission Line Model (TLM) measurements. The developed process is selective because the NiP deposition occurs only onto the desired region of the silicon sample. Solar cells using this front metallization have been characterized by I-V measurements and compared with standard screen-printed solar cells. A silicon nitride layer (PECVD SiNx:H) at the front side of the wafers has been used as an anti-refection coating and as a mask for the metal deposition. This dielectric layer has been patterned thanks to an etching step through a screen-printed resist. pH of the electroless bath, the light application, annealing temperature were investigated. Experimental conditions have been found to avoid the shunt formation during annealing of the contact.

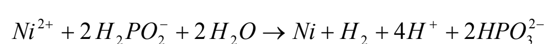
1 INTRODUCTION

One of the major problems limiting the efficiency of solar cells is the quality of the contacts. Currently, screen-printing is the prefered metallization technique for silicon solar cells production in the industry. However, standard screen-printing technology presents some limitations such as the requirement of high surface doping for contact formation, the necessity to pattern and align for selective emitter technology and the shadow losses induced by the relatively large thickness of the fingers. The development of alternative metallization technologies that could eventually replace screen-printing is required. A solution is to develop a “two-layer” contact. This paper is focused on the establishment of a nickel-phosphorous (NiP) electroless seed layer thickened by a silver electrolytic deposition. Electroless NiP deposits are very interesting because of their low resistivity, the low process temperature, their good diffusion barrier property and their self alignment. However, one of the principal issues linked to the NiP deposition step is the shunt formation [1]. To solve this problem, parameters like the characteristics of the bath and the annealing conditions of the NiP layer were studied.

2 NIP ELECTROLESS CONTACT ON SILICON

2.1 Principle

The electroless deposition of NiP is performed using a low temperature alkaline plating bath containing sodium hypophosphite as a reducing agent and ammonia for pH control. The operating temperature is 95 °C and the deposition rate is about 10 µm/h. This autocatalytic process is based on the capture of electrons by the nickel cations Ni^{2+} present in the solution. Electrons are supplied by a reducing agent, in our case sodium hypophosphite (NaH_2PO_2). When dissolved in the solution, sodium hypophosphite gives $H_2PO_2^-$ ions which are adsorbed at the surface of silicon. The chemical reaction is the following:



$$Ni^{2+} + 2H_2PO_2^- + 2H_2O \rightarrow Ni + H_2 + 4H^+ + 2HPO_3^{2-}$$

Other reactions take place simultaneously in the solution. An important one is the formation of atomic phosphorus which gets incorporated into the lattice of the metal film. Moreover it is a selective process because the deposition occurs only onto the desired region of the silicon sample as shown on Fig. 1.

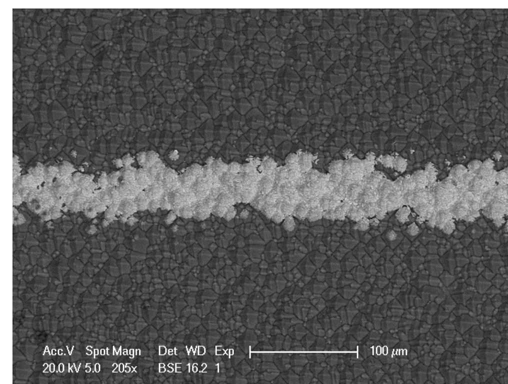


Figure 1: SEM view of a NiP/Ag contact through a silicon nitride etched

2.2 Initiation of the deposition

It is believed that the mechanism of the initial deposition of nickel on Si wafer is different from the autocatalytic reaction involving the reducing agent. It means that deposition on Si can be described as a two step reaction: an initial reduction of Ni^{2+}, also called the activation, and then the NiP autocatalytic deposition by reaction with the reducing agent. In this paper, two activation mechanisms have been tested for the initiation of the Ni deposition.

The first one is the spontaneous deposition which occurs by simple immersion in the plating bath at high pH (pH>9). It has been observed that the more alkaline the plating bath is, the quicker the initiation. The reduction of Ni^{2+} occurs thanks to the galvanic displacement reaction of silicon in the alkaline aqueous solution. In other words, nickel ions receive electrons released by the electrochemical oxidation of Si.

According to Takano et al. [2], a silicon oxide layer between the Ni deposit and the substrate is produced as a result of the reaction of oxidized Si with OH^- ions, which is promoted by Ni^{2+}.

Another way to initiate nickel deposition is the photoactivation. During this mechanism, electron-hole pairs are generated in Si and used to reduce the Ni^{2+} cations at the silicon surface. Simultaneously, O_2 is generated by the anodic reaction since electrons are injected from hydroxide ions into the valence band of silicon. In our experiments, a halogen lamp was used and an homogeneous layer is obtained after a few seconds of illumination.

2.3 Reaction between NiP and Si with temperature

The reactions between Ni and Si under thermal annealing have been extensively studied for vacuum-deposited contacts [3-5]. It is known that Ni is the dominant diffusing species in the case of thin Ni film deposited on Si substrate [6]. As the temperature increases, the following phase formation is usually found in the literature [7, 8]: Ni/Si → $Ni/Ni_2Si/Si$ → Ni_2Si/Si → $NiSi/Ni_2Si/Si$ → NiSi/Si → $NiSi/NiSi_2/Si$ → $NiSi_2/Si$. Initially, the Ni_2Si phase appears at 200-300 °C. Then, the monosilicide NiSi begins to form at 400 °C. Above 700 °C, a $NiSi_2$ phase occurs through silicide nucleation in NiSi. At 900 °C, NiSi is completely transformed into the stable $NiSi_2$ phase. In our case, the silicide formation in NiP/Si system has been investigated using RBS, GIXRD and SEM to understand the variation of ρ_c with annealing temperature [9]. The results enabled us to conclude that the lower contact resistivity values were obtained after rapid thermal annealing treatment at temperature between 400 °C and 600 °C during 30 s in a N_2 atmosphere. Considering the experimental results and the properties of silicides found in the literature [6, 10], the decrease of ρ_c observed between 400 °C and 600 °C is attributed to the formation of NiSi silicide detected with GIXRD and RBS.

Table 1: Best values of ρ_c obtained on n-type $POCl_3$ emitter (40 Ω/□) by TLM after 30s in N_2 atmosphere in RTA furnace

Annealing temperature (°C)	200	400	500
ρ_c (Ω.cm²)	7.10^{-4}	3.10^{-4}	9.10^{-5}

From Table 1, it is obvious that even at lower annealing temperature, contact resistivities are still better than typical screen-printing contact resistivity of about 10^{-3} Ω.cm² [11]. It could be preferable to choose this range of temperature in the case of silicon solar cell contacts to avoid the potential shunt formation of the junction during annealing of the NiP contact.

3 EXPERIMENTAL

All the cells were made with crystalline CZ silicon wafers, p-type, 250 µm thick, ~ 1.5 Ω.cm. The wafers were 125 x 125 mm² samples textured and submitted to $POCl_3$ diffusion. The emitter sheet resistance was around ~ 40 Ω/sq. Samples were cut into 4 cells with an active area of 5 x 5 cm² and divided into three groups, as presented in Fig. 2. The screen-printed group was used as a reference. Wafers were screen-printed on the front side with an Ag paste using a pattern with a finger width of 120 µm and a finger distance of 2 mm. The rear side was fully printed with an Al paste and fired to form the back surface field. The NiP deposition was performed through the antireflection coating. For process 1, the solution was very alkaline (pH ~ 10) and the substrate is immersed during 1 min. For process 2, the pH of the bath was about 8 and the deposition occurs thanks to the irradiation with an halogen lamp during a short time (3-5 s). The NiP layers were annealed 30 s in N_2 atmosphere in a RTA furnace. Finally, an electrolytic deposition of Ag (~ 7 µm) was realised. The finger width was ~ 130 µm and the finger distance 2 mm for both processes.

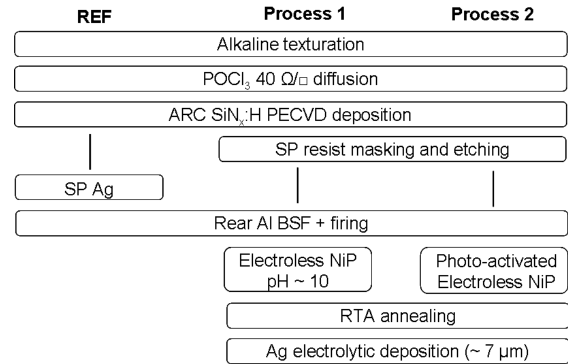


Figure 2: Processes applied for the comparison between two electroless NiP techniques and standard screen-printed

4 RESULTS AND DISCUSSION

To evaluate the shunt formation, the pseudo-fill factor (pFF) was determined by Suns-Voc measurements [12]. For process 1, a strong degradation of pFF was revealed after deposition and annealing of the NiP contacts as shown on Fig. 3.

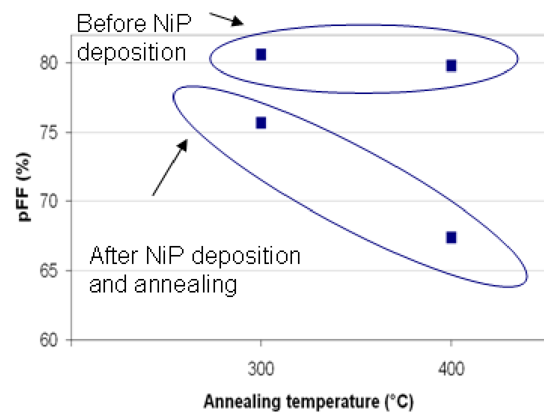


Figure 3: pFF as a fonction of annealing temperature for cells realised with process 1 (average of 3 cells for each temperature)

Infrared thermography of cells from process 1 under inversed bias presented on Fig. 4 confirms the presence of local shunts situated on the metal lines (Fig. 4). The hypothesis that could explain this shunt formation is the activation mechanism of the deposition which occurs in the alkaline environment. Indeed, at high pH, the initiation of the deposition begins from active sites which expand to finally produce a uniform layer. However, this mechanism induces an inhomogeneity in thickness and

results in local spikes because nickel diffuses more easily where the thickness is larger.

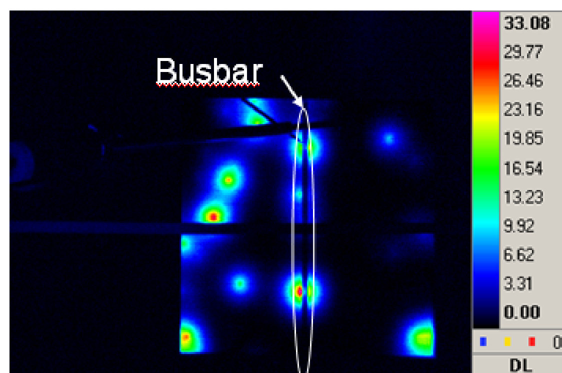


Figure 4: Infrared thermographic of a cell from process 1 in inversed bias

The alternative photoactivated process 2 leads to a very thin (< 50 nm) and homogeneous NiP layers in a few seconds. Moreover, during this step, silicon is not consumed in opposition to the activation mechanism at high pH.

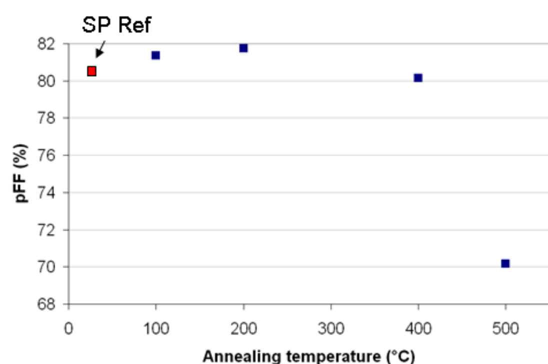


Figure 5: pFF as a fonction of annealing temperature for cells realised with process 2 (average of 3 cells for each temperature)

The evolution of pFF as a function of annealing temperature represented on Fig. 5 shows the possibility to anneal the NiP deposits up to 400 °C without shunt formation. As presented on Tab. 2, best result with process 2 has been obtained for a low temperature annealing (200 °C). The series resistance Rs was calculated by comparing the Suns_Voc measurements with the IV characteristics for the cells at their maximal power point [13].

Table 2: IV results for the best cell realised with process 2 compared with the best standard screen-printed reference

	Jsc (mA/cm²)	Voc (mV)	FF (%)	pFF (%)	Rs (Ω.cm²)	η (%)
Ni/Ag	35,4	617,3	76	80,1	0,82	16,6
SP ref	35,6	620,7	76,3	80,4	0,81	16,8

This result is very promising compared to the screen-printed reference but a lower Rs was expected. Corescan [14] of the best cell realised with process 2 have revealed higher contact resistance at edge of the cell (Fig. 6). The first hypothesis that could explain this problem is an inhomogeneous irradiation during photoactivation avoiding a uniform NiP deposition. Another explanation could be an inhomogeneity of annealing temperature in the RTA furnace.

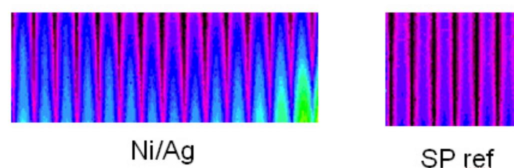


Figure 6: Corescan of a process 2 cell edge

5. CONCLUSION

The optimization of a nickel phosphorous electroless deposition for the front side silicon solar cell metallization has been investigated. The photoactivation of the NiP deposition induces a better control of the metal thickness Experimental conditions have been found to avoid pseudo-FF decrease after metallization and to obtain cells with efficiencies similar to screen printed cells at low annealing temperature.

ACKNOWLEDGEMENTS

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ADVANCED FRONT SIDE METALLIZATION FOR CRYSTALLINE SILICON SOLAR CELLS BASED ON A NICKEL-SILICON CONTACT

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ABSTRACT: Silicon solar cells were metalized on the front side using plated nickel-silicon contacts. Nickel is used as a seed layer for silver LIP, or simultaneously used as a seed and diffusion barrier for copper LIP. Suitable plating techniques and parameters were determined, using electroless nickel and tin, and light induced plating of nickel, silver and copper. Solar cell efficiencies 17.4% on CZ industrial-type material (5x5cm²) have been achieved for a two step nickel-silver metallization, and 17.1% for a nickel-copper-tin stack. Long term stability limitations due to copper diffusion with respect to $5\%_{rel}$ degradation have been evaluated by a method developed in our labs. A cell life time limitation well exceeding several hundred years was estimated.

1 INTRODUCTION

Today's standard front side metallization is screen printing of a silver containing paste, which is able to etch through the anti reflection coating (ARC) for contact formation in a high temperature firing step. Yet the common industrial product is a lead containing, porous grid with a poor aspect ratio and relatively low specific conductance. Considering rising cell sizes this may become a limiting factor for cell performance, unless the metal fraction of the surface is increased, leading to more shading losses. Additionally the cost of metallization amounts to roughly 30% of module construction, where the use of silver pastes contributes to this very importantly. At present the power generation costs of photovoltaic energy are not competitive to the costs of fossil energy sources. In order to reach competitiveness, it is strived for a combination of lowering production costs of solar cells and raising their efficiency.
An alternative to printed and fired paste is the deposition of a contact forming material onto the emitter after selectively opening the ARC. Nickel is a suitable material, due to its low barrier height and the possibility of thermal nickel-silicide formation for increased adhesion and decreased contact resistance. Additionally it can be applied by the inexpensive method of plating, which has the further advantage of being a self aligning process, since plating only occurs on conductive surfaces or in case of electroless plating on catalytically active surfaces, respectively. The firing of the rear side aluminium paste can be optimized on back surface field (BSF) formation, instead of being engaged by the firing parameters of the front side metallization.

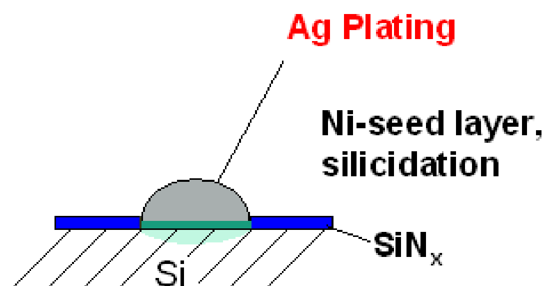


Figure 1: schematic cross section of a Ni/Ag two-step metallization

As presented by A. Knorz and M. Aleman [1] on high efficiency wafers, after laser ablation of the ARC, a two step front side metallisation system based on a plated nickel seed layer which is then thickened by silver plating, has a the potential of a grid with low specific resistance and high aspect ratio. An efficiency as high as 20.7% has been demonstrated (see fig. 1).
A plated Nickel-Copper-Tin stack (see fig. 2) system has a similar potential, since the highly conductive silver is replaced by virtually equally conductive copper, while using materials of lower cost (see tab. 1).

Table 1: property comparison of utilized metals

	Silver	Copper	Nickel
Conductivity [10^6 S/m]	61,39	59,1	13,9
ρ [g/cm³]	10,49	8,92	8,9
Costs (2 year mean) [€/kg]	388,8	4,1	12,8

The price of plating electrolytes is not significantly higher than the cost of the bulk metal, while the cost of screen printing silver pastes influences the metallization cost to some extent compared to the bulk silver price.
A major drawback on the utilization of copper is the combination of its high diffusivity in silicon and its unfavourable impurity level, making copper a kind of poison for silicon solar cells. Nickel is not only suitable for contact formation, it can also act as a diffusion barrier to copper [2], enabling the use of copper for front side metallization of silicon solar cells. Its functionality is already being used in microsystems engineering and has been proven in a solar cell process by BP-Solar with laser grooved buried contacts [3].

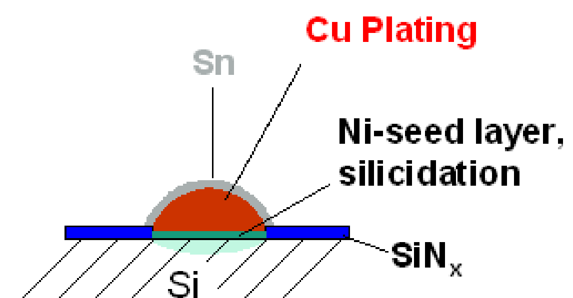


Figure 2: schematic cross section of a Ni/Cu/Sn three-step metallization

Furthermore, two step metallization systems have been shown to move the performance of industrial solar cells towards the efficiency of laboratory solar cells [4]. They enable the application of very narrow contacts with high aspect ratio, leading to an important increase in j_{SC}.
A major concern of copper utilization is the long term stability of silicon solar cells, obliged to meet the requirement of at least the warranty time, given by solar panel distributors, being 25 to 30 years. The method we applied for estimating solar cell lifetimes under operation conditions has been described in another publication [5].

2 EXPERIMENTAL

For the plating experiments, commercially available industrial substrates with a size of 156x156 mm², featuring a shallow 65Ω/sq emitter and a SiNx-ARC were used. Rear side aluminium screen printing and firing were done in our labs. These wafers were cut into 5x5 cm² test cells. Two different techniques were examined for selective ARC-opening: the mask & etch method and laser ablation. In the first technique a hydrofluoric acid resistant ink is applied to the ARC by inkjet printing, leaving gaps in the regions the grid is to end up (fig. 3 a).Since this is done free of mechanical contact, the risk of breakage is minimized. The unprotected ARC is etched by hydrofluoric acid, exposing the emitter (fig. 3 b). The mask can then be stripped by an organic solvent (fig. 3 c).

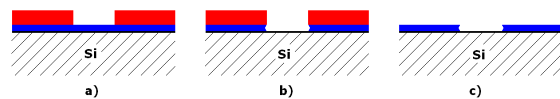


Figure 3: schematic mask & etch sequence

The laser-ARC-ablation is done by scanning the wafer with a pulsed laser beam at a wavelength of 355 nm in the desired grid pattern. Since the geometry of the random pyramids focuses the light on their edges [6], the emitter is primarily exposed in these areas. This leads to a smaller opened area than with the use of masking and etching (compare fig. 10 and left part of fig. 14), but it is well sufficient for electrical contact. Laser ablation allows the application of extremely thin fingers down to 30µm (10µm wide seed layer plus 10µm growth in every direction by LIP of conductive layer) for minimal shading loss. These methods have the distinction of a low cost opening with a minimized risk of breakage, since they are performed free of mechanical contact.

The used electrolytes were commercially available silver, copper and electroless nickel plating solutions, and a simple Watts type nickel electrolyte for light-induced plating (LIP) set up in our labs. Temperature and electrolyte properties (e.g. pH-value) were kept constant between all experiments and according to the manufacturer's specifications. Potentials and currents were applied and measured by either using a versatile multichannel potentiostat (VMP, Bio-Logic) for the silver deposition experiments, or a programmable source measure unit (Keithley) with a coupled power amplifier. A schematic image of the plating bath's setup can be seen in figure 4.

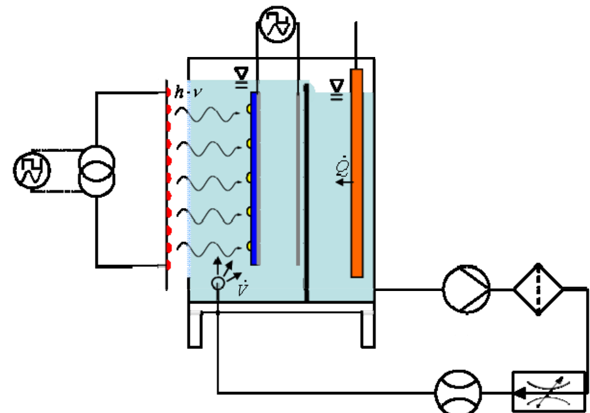


Figure 4: schematic plating bath setup

In case of the electroless nickel plating no rear side voltage is necessary. Deposition only takes place on catalytically active surfaces, meaning the exposed areas of the emitter and not on the ARC. Light is used for adjustment of the electrochemical potential of front and rear side (see fig. 5).

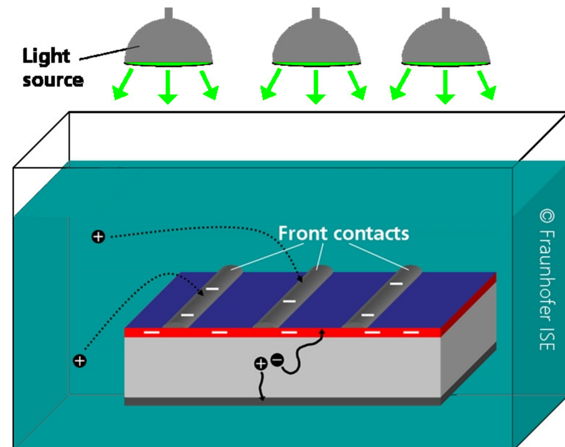


Figure 5: schematic light assisted electroless plating

In case of the light induced plating, the power produced by the illuminated cell is used for plating. A voltage is applied between the rear side of the cell and the nickel, silver or copper source (see fig. 6). Deposition only takes place on conductive surfaces, meaning the opened areas, not covered by the ARC.

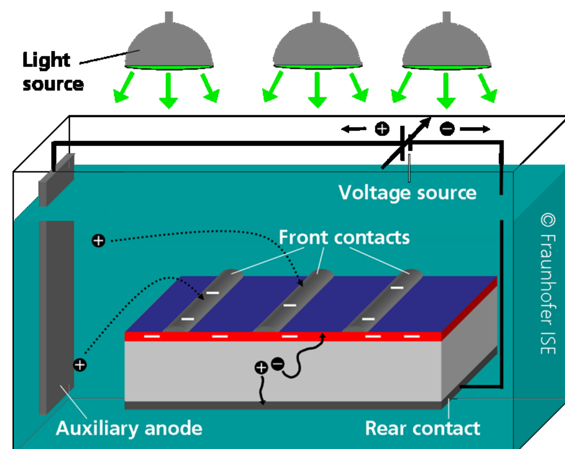


Figure 6: schematic light induced plating

The properties of resulting nickel layers feature different advantages which implicate the application of one or the other plating technique, depending on the intended process: The Ni-LIP method is rather simple and has a high plating rate, while requiring only minor process maintenance, though obtaining good homogeneity of the plated layer is challenging. It is well suited for seed layer deposition and barrier layer deposition - also on a printed and fired seed. The light assisted electroless plating is an extremely simple process with an easier control of layer homogeneity. Electrolyte maintenance is generally more demanding, since chemicals are used up, changing concentration proportions. It is suitable for seed layer deposition, while barrier layer deposition is limited due to relatively low deposition speed (even if accelerated by light irradiation).

Temperature stress experiments for simulated ageing and long term stability estimation were carried out using an ordinary hotplate with a programmable control unit. Pseudo fill-factor (pFF) measurements were made with the Suns-V_{OC} technique as described by Sinton and Cuevas [7], using the generalized analysis type, with temperature correction to 25°C.

Adherence was tested by a simple qualitative peeling test, by sticking a length of self adhering tape to the metallisation and pulling the tape off. If metal adherence to the tape was higher than to the wafer, it was validated as “insufficient adherence”.

3 CONTACT FORMATION

An ideal contact would be an ohmic contact with a negligible contact resistance. In reality a metal-semiconductor contact has a rectifying character, described by Schottky in 1938 [8]. This phenomenon is known as “Schottky Barrier”. When metal and semiconductor are put to contact, an electron transfer takes place for thermal equilibrium. A zone close to the surface is charged negative in the metal and positive in the semiconductor. The result is a space charge region similar to the one in case of a p-n-junction, yet smaller for a given semiconductor.
As mentioned in the introduction, nickel is a suitable material for contact formation due to its low barrier height (figure 7).

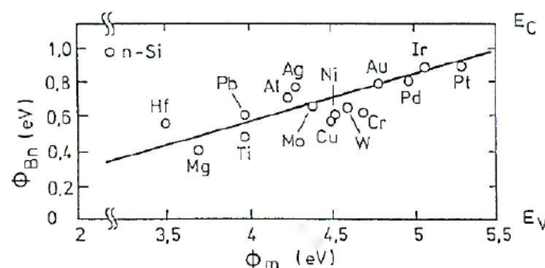


Figure 7: Barrier heights of potential contact forming materials plotted against their work function. [10]

Additionally a nickel silicide can be formed by thermal treatment. Depending on the temperature either $NiSi_2$, NiSi or Ni_2Si is formed, which all show low contact resistance and raised adhesion. Especially on shallow emitters this step is critical, since an overtreatment will lead to silicide formation deeper than the emitter depth d, resulting in damaging the space charge region (SCR), leading to a shunt in the most extreme case (see fig. 8).

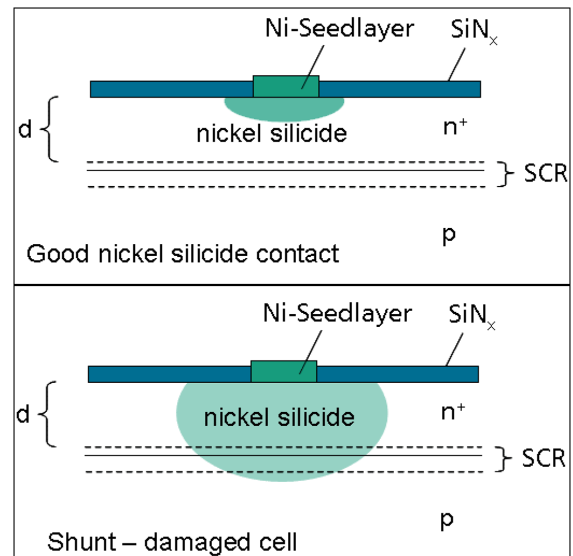


Figure 8: schematic good nickelsilicide contact (top) and a shunted cell (bottom)

There is a narrow window of temperature and time for ideal silicide formation. A wide variation was made to find the borders of this window for inkjet and laser opening. For extremely thin nickel layers no shunts were created even after long annealing time. Presumably all nickel was used up for silicide formation in this case. Apparently silver lacks adhesion to the silicide, similar to the lack of silver adhesion to pure silicon [9], since following silver LIP did not lead to useful plating, or silver falling off spontaneously. For thicker nickel seed layers, plated silver showed sufficient adherence, yet it set a maximum annealing temperature before shunting the cell (see fig. 9). This was determined by a degradation of the pFF in Suns-V_{OC} measurement after annealing. The annealing time was found to have only little influence on the pFF. On best cells it was not possible to determine a contact resistance as the measured values were lower than the resolution of the used measurement device (R_CxW<0.3Ωcm).

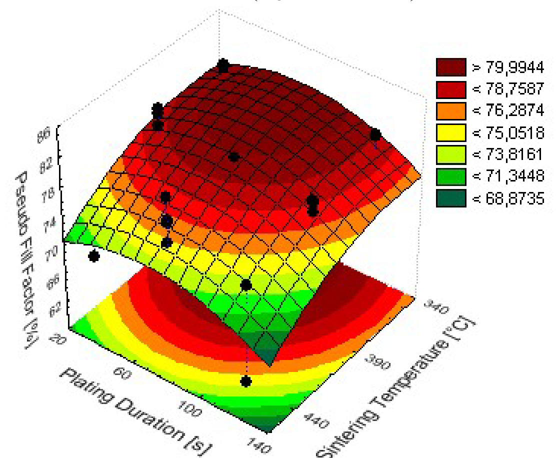


Figure 9: pFF obtained for laser opened cells, plotted against annealing temperature and duration.

First test cells were plated with only a minimal amount of electroless nickel, serving as a seed layer for following silver LIP, while representing a finite nickel source for silicide formation (see fig. 10). For serving as a diffusion barrier to copper, a thicker nickel layer is likely to be needed to withstand a long period of copper impact. Since a silicidation technique had been determined for a thin nickel layer, the barrier was grown in a two step process on to an annealed thin nickel seed layer at first. In later experiments a nickel barrier was plated directly (see fig. 11). The barrier was covered by thick copper LIP for high lateral conductivity (see fig. 12).

For anti corrosion and enhanced solderability purposes the stack was finished by electroless tin plating.

4 CHARACTERIZATION OF METAL LAYERS

The properties of nickel layers were evaluated by SEM imaging, in respect to the homogeneity and integrity of the nickel deposition. A minimal amount of nickel was plated as a seed layer for later silver LIP (see fig. 10).

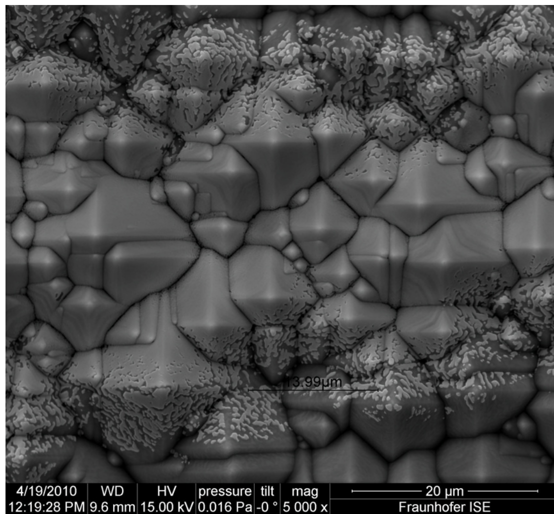


Figure 10: thin nickel seed layer on inkjet ARC-opening example of an underetched mask

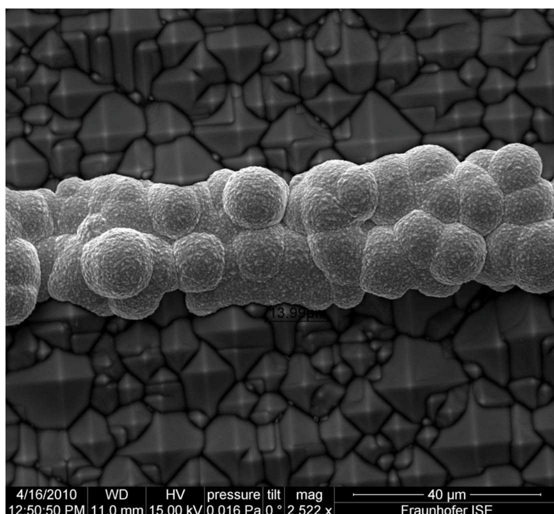


Figure 11: single step processed diffusion barrier, plated on laser ARC-opening

For high lateral conductivity these layers were plated by copper. The homogeneity of copper deposition was evaluated by SEM imaging likewise (see. fig. 12).

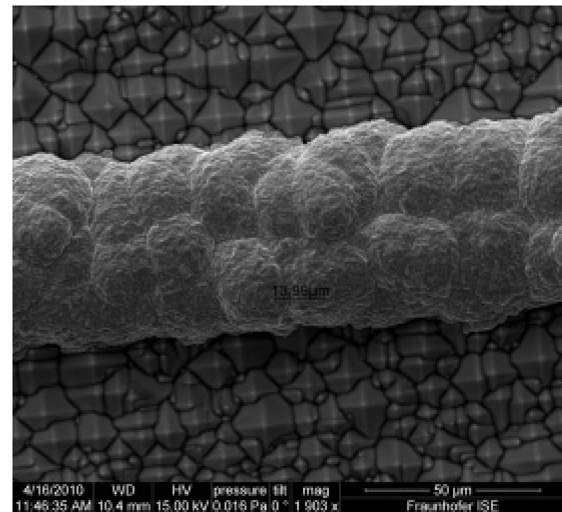
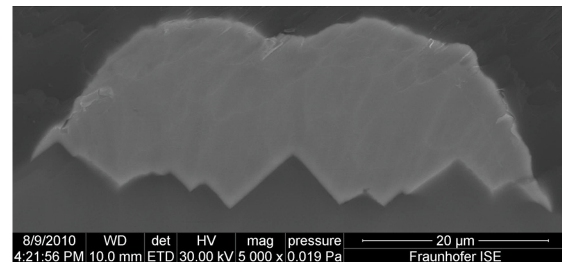


Figure 12: copper layer deposited onto a nickel diffusion barrier

Layer thicknesses were measured by SEM imaging of polished cross sections and EDX measurements in case of multilayered samples (see fig. 13).



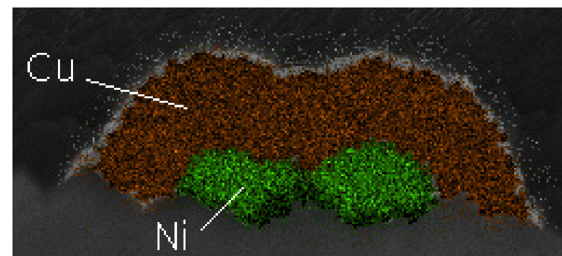


Figure 13: cross section SEM image of a full stack (finger inclined to the edge) and EDX element mapping

5 SOLAR CELL RESULTS

Experiences with the used precursors plating a nickel copper tin stack on fired silver seed layer, exhibited a maximal efficiency of 17.2% [11]. Since the focus was set on the optimisation of nickel seed layers and diffusion barriers, an optimisation of useful copper plating had only secondary priority. Nevertheless efficiencies of 17.4% for a nickel silver stack, and 17.1% for a nickel copper tin stack were achieved (see tab. 2).

Table 2: best cell results. SP: Screen printed and fired silver. AP: Aerosol-printed and fired silver seed layer

	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]	η [%]
SP	615	35.7	75.1	16.5
AP/Ag	614	36.7	78.4	17.7
SP/Ni/Cu/Sn	615.	35.1	79.5	17.2
Laser/Ni/Ag	624	37.0	75.3	17.4
Laser/Ni/Cu/Sn *	623	37.1	73.9	17.1
Inkjet/Ni/Ag	621	36.1	76.5	17.1

***: calibrated measurement: ISE-CalLab**

In the case of AP/Ag an aerosol printed and fired fine line was thickened by silver LIP and in the case of SP/Ni/Cu/Sn a screen printed silver seed was plated by nickel LIP, copper LIP and electroless tin. In the case of Laser/Ni/Ag a laser opened ARC was plated by a thin electroless nickel layer which was annealed and thickened by silver LIP, as it was done in the case of Inkjet/Ni/Ag on a masked and etched opening. In the case of Laser/Ni/Cu/Sn a laser opened ARC was directly plated by a thick nickel layer by LIP, which acts as a diffusion barrier, covered by copper LIP and electroless tin. The raised V_{OC} of cells based on a nickel contact are possibly an effect of an enhanced BSF. The low FF is presumably caused by slight emitter damage by laser impact, and a non-optimized copper layer or grid design. The slightly lower short circuit current density for cells structured by mask and etch can be speculated to be due to slightly wider contact openings, however, better fill factors are achieved, which may be due to lower damage in the ablated area compared to the laser ablation process.

In contact structures where the nickel layer was created in two steps (thin seed layer, thermal contact formation, thick diffusion barrier layer) the seed layer was found to withstand the qualitative peeling test, while the later plated barrier was ripped off (see fig. 14). This improved adhesion of the seed layer is likely to be caused by silicide formation. Also, especially laser structured samples with a nickel diffusion barrier plated in one step exhibit very promising adhesion properties, since most cells withstand the mentioned qualitative peeling test. However, adhesion remains an important challenge for direct metallization.

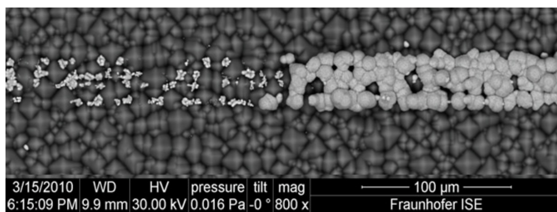


Figure 14: partly torn off Finger of a two step Ni-plating

6 LONG TERM STABILITY EVALUATION

Because of the mentioned problematic nature of copper in silicon, a method for evaluation of long term stability was developed, using the cell itself as a detector for copper diffusion in accelerated ageing tests, by thermal treatment [5]. A stack system of printed and fired silver seed layers, plated by nickel, copper and tin, presented by Jonas Bartsch [11] provides experience in terms of 5% degradation by copper impact in a magnitude of several hundred years. A graph of the degradation over time at different temperatures of these cells is shown in figure 15.

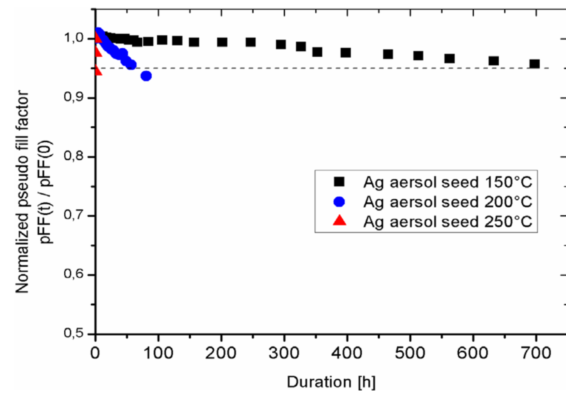


Figure 15: pFF degradation by copper diffusion in an accelerated ageing experiment of solar cells based on a printed and fired silver seed, at different temperatures

Cells presented in this work were exposed to the same temperatures for a multiple amount of time without degrading (see fig. 16 and 17).

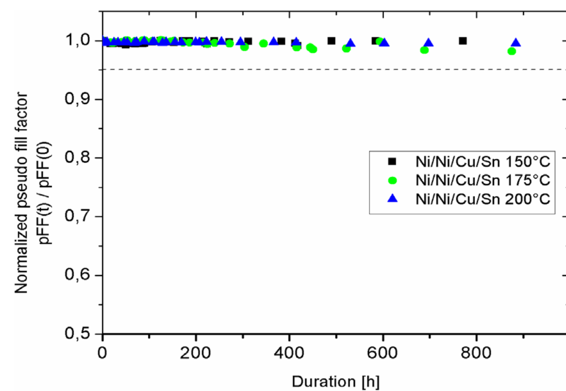


Figure 16: thermal accelerated ageing experiment of cells based on a two step nickel plating.

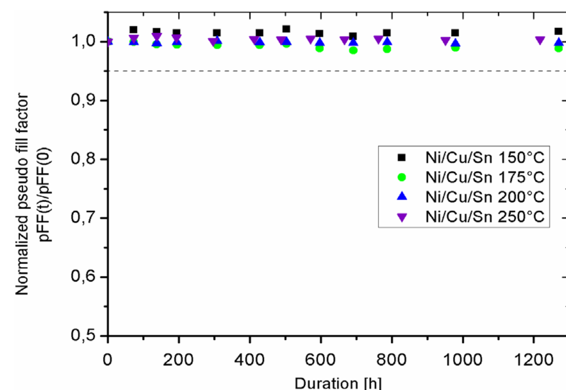


Figure 17: thermal accelerated ageing experiment of cells based on a single step nickel plating.

In the case of Ni/Ni/Cu/Sn a thin electroless nickel layer was annealed and thickened by nickel LIP, while Ni/Cu/Sn is based on a single step nickel LIP barrier.
Since the mentioned long term stability evaluation method requires a measured time until cells have experienced 5% degradation, no quantitative life time estimation was able to be made. The comparison to the mentioned experience [11] leads to the presumption of a well sufficient cell life time.

7 CONCLUSION AND OUTLOOK

The aim of replacing screen printed silver pastes as front side metallization of silicon solar cells by cost effective plating processes seems to come into reach. Plating processes are already entering stages beyond laboratory experiments and are more and more realized in an industrial scale. Nickel plating was shown to be a suitable method to deposit a contact forming seed layer. A suitable nickel-layer enables the possibility of utilization of copper, as was shown with the long term stability investigations. We have found estimated life times in terms of possible degradation by copper diffusion, well sufficient for use of such solar cells on module level. Solar cell efficiencies were able to be increased slightly, in comparison with printed and fired silver pastes. The obtained fill factors are still slightly lower, which is compensated by a higher short circuit current density. As expected, replacing highly conductive silver by highly conductive copper has lead to efficiencies in the same order of magnitude at low price. Quantitative life time estimation can be made by the mentioned method as soon as accelerated ageing experiments have lead to a degradation of 5%. We will continue improving our estimation by generating more measurement points for being able to specify a standard deviation. Also, climate chamber degradation tests will complement the evaluation.

ACKNOWLEDGEMENTS

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INLINE HIGH-RATE THERMAL EVAPORATION OF ALUMINUM AS A NOVEL INDUSTRIAL SOLAR CELL METALLIZATION SCHEME

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ABSTRACT: We evaluate a novel high-throughput thermal evaporation system for the aluminum metallization of solar cells (ATON500, Applied Materials). We demonstrate a maximum throughput of 720 wafers/h (156 × 156 mm² Si wafers coated with a 5 µm Al layer) applying dynamic deposition rates of up to 5 µm × m/min. By adjusting the individual aluminum evaporation rate for each evaporation boat, we achieve an excellent thickness uniformity across the 50 cm wide deposition area on the substrate carrier of less than ±3.4%. The specific contact resistance of an aluminum layer on a 0.5 Ωcm p-type Si wafer is determined to be 4 mΩcm^2 which is in the same range as Al contacts deposited by laboratory-type evaporation systems. During deposition the wafer temperature increases up to 370°C at deposition rates of 2.9 µm × m/min, which is still compatible with high-efficiency Si solar cell processes. By applying these high-rate thermal evaporation of aluminum as metallization to our buried-emitter rear-contact solar cell, we demonstrate a conversion efficiency of 20.6%, proving the applicability of the novel inline evaporation system to the production of industrial next-generation high-efficiency solar cells.

1 INTRODUCTION

Inline high-rate thermal evaporation is used on an industrial scale since many years, for example, for the deposition of aluminum coatings on plastic foil wrapping in the food industry. For the metallization of wafer based silicon solar cells Schott Solar AG used a batch evaporation system from 1992 to 1997 for aluminum deposition in a pilot production [1]. To our knowledge apart from seed layer deposition [2] only laboratory-type evaporation equipment has been used so far [3,4,5]. First results evaporating aluminum in a high throughput inline evaporation system as a solar cell metallization has been published recently [6]. In the photovoltaic industry, screen-printing is widely used for metallization. However, the advantages of aluminum evaporation are that the aluminum used for metallization is relatively inexpensive compared to screen-printing pastes. In addition, the contact resistivity of evaporated aluminum on silicon is lower compared to screen-printed contacts.

2 THE EVAPORATION SYSTEM

In our new ATON 500 inline high-rate thermal evaporation system (Figure 1), up to 720 Si wafers (156 × 156 mm²) can be coated per hour with highly precise process control at 30 times higher deposition rates compared to typical laboratory-type static evaporation systems. In order to compare static to dynamic evaporation rates we use the following conversion formula:

$$R_{stat} = \frac{d}{t} = \frac{d\,v}{L} = R_{dyn} \qquad (1)$$

R_{stat} and R_{dyn} are the static and the dynamic evaporation rate, respectively. The thickness of the deposited film is d, and t the duration of the static deposition. In case of a dynamic deposition the substrate travels with velocity v across a deposition area with length L. Accordingly, the substrate remains within the deposition area for a duration of L/v seconds. The formula furthermore assumes a homogenous aluminum flux within the deposition area.

The ATON 500 consists of a loading area, seven vacuum chambers and an unloading area and can be used in a continuous or in an oscillating substrate flow mode (Figure 2). The oscillating substrate flow simulates multiple serial evaporation chambers by crossing the evaporator several times during one deposition.

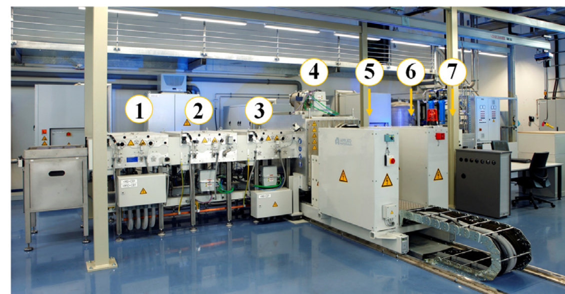

Figure 1: ATON 500 inline high-rate evaporation system installed at the ISFH. The modules indicated by numbers in the photo above will be explained in the schematic drawing in Figure 2.

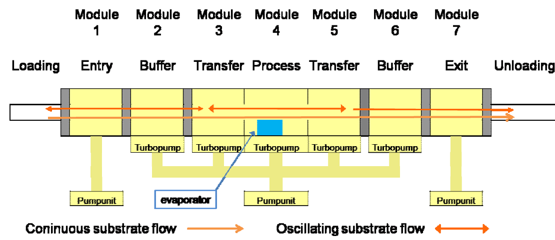

Figure 2: Schematic drawing of the ATON 500 inline high-rate evaporation system. In continuous substrate flow, a user-defined number of carriers move through the system from the loading to the unloading zone by passing the evaporator only once. In oscillating substrate flow, one carrier moves from the loading zone to module 5, changes its direction, moves to module 3, changes its direction, and so on. This carrier leaves the system either at the unloading or at the loading zone, depending on the number of oscillations.

The thermal evaporation of aluminum wire in the evaporation chamber is illustrated in Figure 3. The boron nitride evaporator boats heated to between 1200°C and 1400°C are constantly supplied with aluminum wire by stepping motors. The end of the wire evaporates close to the boats and vaporous aluminum fills the part of the vacuum chamber above the boats. The sample carrier passes through this metal vapor cloud with its solar cells, so that aluminum condenses on the solar cells and forms the metallic contact. In order to avoid overheating, an efficient cooling system with an external cooling water supply has been installed in the vacuum chamber.

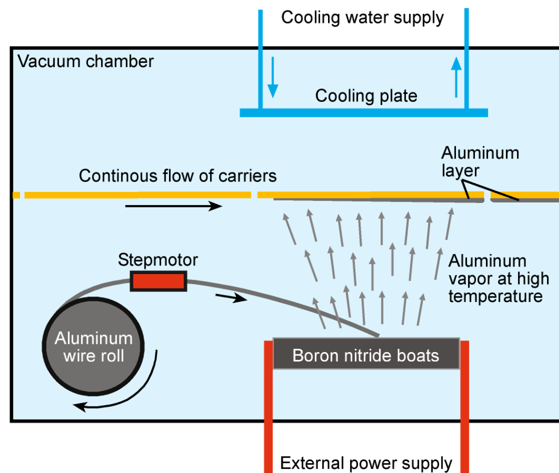

Figure 3: Schematic drawing of thermal evaporation of aluminum.

3 EXPERIMENTAL RESULTS

We measure the deposition uniformity on glass substrates with 45 measurement points on one carrier, as shown in Figure 4, using a Dektak 150 surface profiler. To this end we bond pieces of high temperature stable tape on the glass substrates, evaporate the aluminum layer and peel the tape off. Then we measure the step hight between aluminum layer and glass surface.

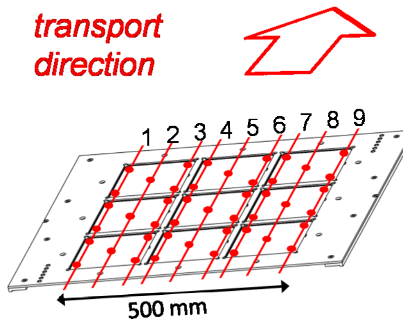

Figure 4: Schematic drawing of the positions of the aluminum thickness measurements on the carrier.

The thickness uniformity was calculated using the equation

$$D = \frac{D_{max} - D_{min}}{D_{max} + D_{min}} \qquad (2)$$

Due to ten separately-adjustable evaporator boats in the process chamber of the ATON system, a very precise thickness control is possible, leading to a thickness uniformity across the carrier of only ±3.4%, as shown in Figure 5.

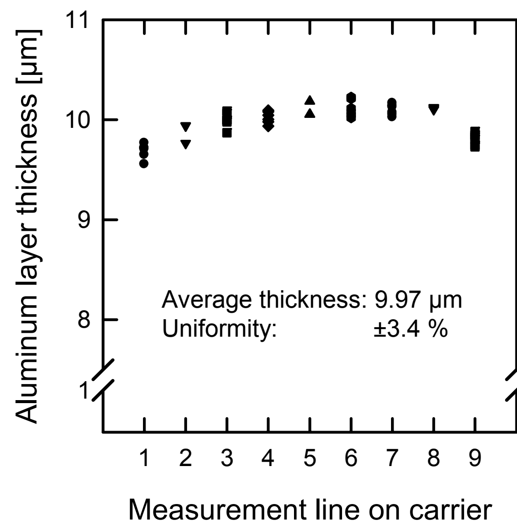

Figure 5: Uniformity of a 10 µm aluminum layer across the carrier width of 500 mm.

The high evaporation rates necessary for high process speeds cause a high penetration of heat into the solar cell. In order to reduce heat penetration, both practical experiments and two-dimensional simulations with the finite-element method are being conducted. Details on two-dimensional simulations can be found in [7]. As a result of our experiments, Figure 6 shows maximum wafer temperatures for aluminum layers of different thicknesses, deposited at different dynamic deposition rates (ddr).

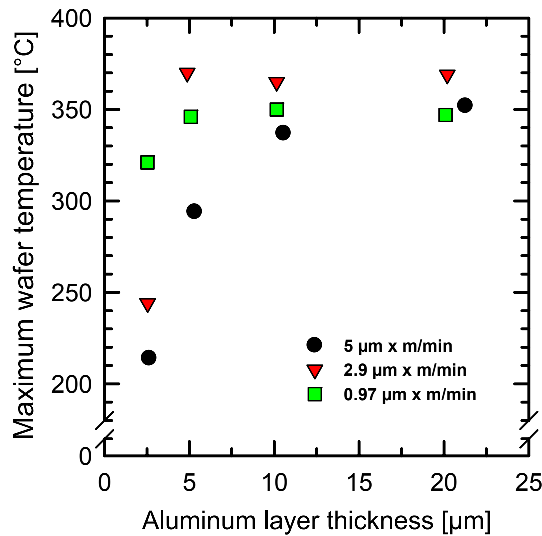

Figure 6: Maximum temperature load on a wafer as a function of aluminum layer thickness deposited at different dynamic deposition rates.

At aluminum layer thicknesses of 2.5 µm, as can be used for example for the back contact of two-side contacted solar cells, a deposition with a ddr of 0.97 µm × m/min leads to a maximum wafer temperature of 320°C, while a deposition with a ddr of 5 µm × m/min leads to a much lower temperature of 215°C. For thin aluminum layers the selected process has a big influence on maximum wafer temperature. At an aluminum layer thickness of 20 µm, as required for rear-side interdigitated contacts, temperatures measured are between 350°C and 370°C. The temperature differences between the dynamic deposition rates of 0.97 µm × m/min to 5 µm × m/min have considerably less variation at thicker aluminum layers.

Therefore wafer temperatures depend on (i) the aluminum layer thickness, (ii) the dynamic deposition rate used and (iii) the number of evaporation sources. For many solar cell concepts, the measured temperatures of up to 370°C for aluminum deposition are in the tolerable range. The actual tolerance to the deposition temperature depends on a broad range of conditions. One of them is the question whether merely base-type surfaces are metallized or whether emitters are metallized. In case of very shallow emitters that are metallized with pure aluminum (e.g. not doped with Si) the temperature tolerance may be even lower than 370°C due to spike formation of Al in Si.

Contact resistance measurements are carried out on test structures using the transfer length method (TLM). As an example, Figure 7 shows the contact resistance measurements on a p-type FZ-Si wafer of 0.5 Ωcm resistivity, revealing specific contact resistances of 4 mΩcm^2 for ATON-coated samples compared with samples, metalized in static laboratory-type systems. This laboratory-type systems (in this paper referred to as “BAK EVO liner” and “BAK EVO crucible”, “BAK 550” and “BAK 600”) are equipped with different electron-beam evaporation systems or equipped with thermal evaporation systems (in this paper referred to as “BAK EVO thermal”) with one boron nitride boat. The evaporation rates of this laboratory-type systems are in the range of 4 to 8 nm/s. The ATON 500 system is equipped with 10 boron nitride boats for thermal evaporation. A dynamic deposition rate of 5 µm m/min equates to a static rate of approximately 280 nm/s. The samples prepared in the static laboratory-type systems with low deposition rates require subsequent heating to achieve low contact resistances. In contrast, the specific contact resistance of test structures prepared in the ATON system shows a value of 4 mΩcm^2, independent of subsequent annealing. The samples in the inline system were already exposed to higher temperatures during deposition of the aluminum layer, as heating has already occurred during the deposition process with high evaporation rates. A detailed analysis of aluminum layers deposited as point contacts on crystalline silicon wafers is given in Ref. 8.

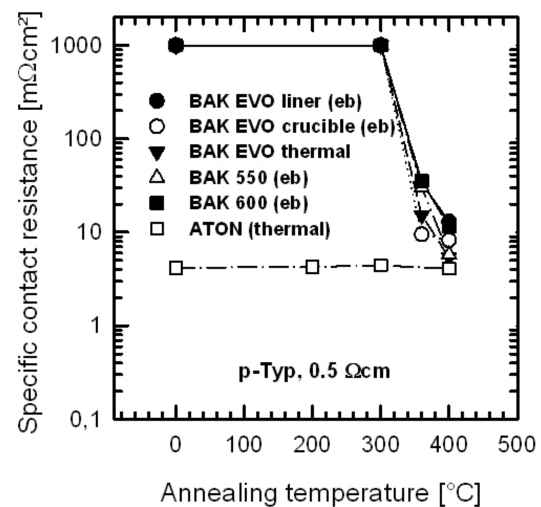

Figure 7: Specific contact resistance on a p-type wafer of 0.5 Ωcm resistivity. Samples were prepared in different laboratory-type static BAK systems (low deposition rates) and in the inline high-rate evaporation system ATON (high deposition rates) with electron-beam (eb) or thermal (thermal) evaporation.

By applying the novel, optimised high-rate thermal evaporation of aluminum as metallization to buried-emitter rear-contact solar cells [4] on 2.6 Ωcm *n*-type Cz-Si, we demonstrate a conversion efficiency of 20.6%. This solar cell was first metallized with Al in the static BAK EVO system, then the metallization layer was structured and all cell testing was done. Afterwards the metallization of this solar cell was etched back and a new aluminum layer was deposited in the inline ATON system, followed by structuring and cell testing.
Table 1 compares the solar cell parameters for both processes. The results are very similar. The *I-V* curve of the cell with the ATON metallization is shown in Figure 8.

Table 1: Solar cell data of a buried-emitter rear-contact cell, first metallized in the static BAK system, etched and then metallized in the inline ATON system.

	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	η [%]
BAK	644	41.1	78.3	20.8
ATON	649	41.3	77.0	**20.6**

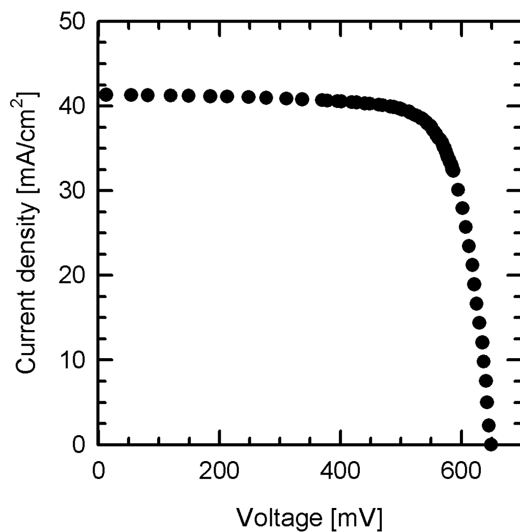

Figure 8: *I-V* curve of a buried-emitter rear-contact solar cell (3.96 cm², Cz-Si, 2.6 Ωcm) with 10µm aluminum layer, metallized in the ATON system showing a conversion efficiency of 20.6%.

4 SUMMARY

We have analyzed several different thermal evaporation processes using a novel high-throughput inline evaporation system. All relevant aluminium layer thicknesses from 1 µm to more than 20 µm, depending on different solar cell concepts, can be fabricated. Thickness uniformity across the 500 mm wide deposition area varies only by ±3.4%. Depending on layer thickness deposition temperatures reach values from 200°C to 370°C. Samples prepared in the inline system achieved specific contact resistances of 4 mΩcm² without subsequent annealing. Compared to static laboratory evaporation systems comparable cell efficiencies of up to 20.6% were reached. This demonstrates the applicability of the novel inline evaporation system to the production of industrial next-generation high-efficiency solar cells.

ACKNOWLEDGEMENTS

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INDUSTRIAL INLINE PVD METALLIZATION FOR SILICON SOLAR CELLS WITH LASER FIRED CONTACTS LEADING TO 21.8 % EFFICIENCY

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ABSTRACT: In this contribution we present the latest results of our experiments in regard to an industrially feasible inline physical vapor deposition (PVD) metallization method for the rear side of passivated solar cells. In an earlier publication, the quality of such processed layers and the feasibility of the tool was already shown and compared with a commonly used laboratory process based on electron beam evaporation. Since then a difference in the V_{oc} potential in the range of ~ 4 mV between both processes was observed on highly efficient cell devices. Ongoing experiments were then carried out to study the cause of this loss. First, it can be shown that the front side of the devices is not harmed in any way by the inline process. On the rear side, investigations regarding the impact of the lower aluminum purity and the higher process temperature in the case of the inline process were carried out. Finally, it is shown that an altered annealing process, which is likely to be necessary due to the different process temperature will exceed the voltage potential of the laboratory e-gun process, leading to very high efficiencies of 21.8 %.

1 INTRODUCTION

To make solar energy long-term competitive, the price per watt-peak has to decline. Therefore new cell concepts, with higher efficiency and cost saving potential, have to be introduced in the market. Even metallization by means of PVD is not compulsory for some of these concepts – they all benefit from the advantages which come along with it, such as lower materials consumption, lower temperature treatment and a lower mechanical impact compared to screen printing, which is still the state of the art metallization technique in the photovoltaic industry. A lower stress impact is especially important when producing thinner and thinner wafers – enabling a substantial cost reduction potential for all future cell concepts [1].

We use thermal aluminum evaporation along with other techniques for manufacturing solar cells with laser fired contacts (LFC) [2], which is a promising technique for realizing local contacts on a dielectrically passivated rear cell surface, introduced by Blakers et al. with the passivated emitter and rear cell (PERC) already more than 20 years ago [3]. In this approach, the aluminium is contacted with the silicon through the dielectric passivation by means of single laser pulses.

In a previous publication related to this metallization process we already showed its sufficient quality by reaching efficiencies of 21.0 % [4]. Nevertheless, these cells fell short of the voltage potential of our reference process by ~ 3-4 mV. Since we discovered a similar voltage decrease at another batch, this matter motivated our ongoing work, where the focus again was put on LFC cells. However, the most important results of this paper hold for all cell concepts that feature a SiO_2 passivated rear side, covered by aluminium with a subsequent annealing process [5],[6].

2 PVD EQUIPMENT

Three different PVD techniques can be applied in general for the deposition of aluminum: sputtering, thermal and e-gun evaporation. In the years 2003-2006,

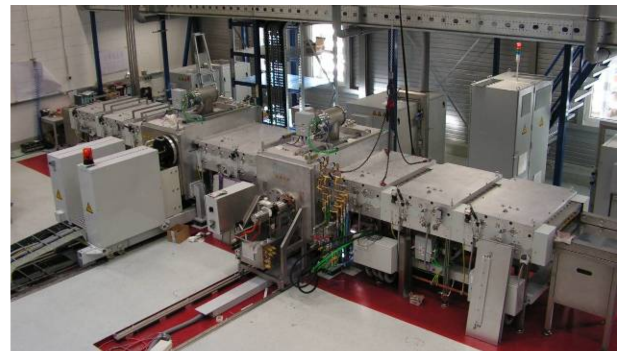

Figure 1: Picture of the ATON 500 based evaporation equipment.

Fraunhofer ISE and Applied Materials - among others - together ran the joint project “INKA” in order to investigate the industrial-scale feasibility of these individual technologies [7], since at that time all high efficiency concepts depended on the PVD process, which is widely performed in laboratories. As a result a pilot line system, seen in Figure 1, based on the ATON 500 [8] was developed and set up at Fraunhofer ISE at the end of 2008. It features an inline process with a thermal evaporation technique, which induces less damage to the passivation than coating by electron beam (e-gun) [7], achieving an industrial suitable throughput of 540 156x156 mm^2 sized wafers per hour. For this purpose, aluminum wires are driven on several heated crucibles; see Figure 2, resulting in a continuous generation of aluminum vapour, which condensates on the samples. The wire feed rate and the power of the crucibles can be adjusted independently and separately for each crucible, resulting in different possible dynamic deposition rates A_{dep}. Thus the homogeneity over the complete tray width as well as the overall deposition rate can be controlled. The thickness of the aluminum layer can additionally be adjusted by the transport speed of the tray through the machine. Each tray contains nine 156x156 mm² wafers.

Figure 2: Aluminum wires and evaporation boats

3 FIRST PROCESS QUALIFICATION

To qualify the machine, several experiments were carried out to determine the properties of the aluminum layer, the results of which can be found in an earlier paper [4]. There it is shown that sufficient homogeneity of 4.5 % on one wafer and 6.3 % on one tray can be reached together with very low resistivity values ρ of 32 nΩ*m, which is only 20 % higher than the value of bulk aluminium (ρ_{bulk} = 26.5 nΩ*m). Additionally, the ability of these processes for the production of passivated solar cells was qualified by means of lifetime measurements on special samples and a batch of highly efficient solar cells. Within these experiments, a comparison with the laboratory system that is commonly used also took place, in which aluminum is evaporated in a crucible by an electron beam underneath a rotating wafer carrier. Despite reaching high lifetimes of up to 500 µs on FZ 1 Ω*cm material in combination with a 100 nm SiO_2 passivation and an final annealing process as well as cell efficiencies η of up to 21.0 %, the voltage potential of the reference process could not be reached, lying at ~ 3-4 mV below potential as mentioned before [4]. Our search for the origin of this effect began with an investigation of the most important process parameters, which tend to differ between both processes.

In [4] we already presented investigations into the temperature rise of the sample during the inline evaporation, which is mainly caused by the heat of condensation. Consequently, the peak temperature depends on the process speed and amount of aluminium; specifically, its layer thickness. In case of a deposition of 2 µm aluminium, a 200 µm thin wafer reaches peak temperatures above T_{peak} > 300°C for just a few seconds as was determined by means of a measurement console from ECD.

Unfortunately, this measurement can not be applied to the laboratory e-gun system due to the electromagnetic field inside the evaporation chamber, which is necessary to guide the electron beam. However, the maximum temperature reached in the laboratory system in the case of a 2 µm aluminium deposition is identified as T ~ 90°C by means of temperature sensible labels. Since this process features a homogeneous deposition rate over 25 minutes, it is obvious that the process temperature between both processes varies strongly, what can result in a diverse layer composition at the interface.

Beside the process temperature, the purity of the used aluminum varies strongly when comparing both processes. While aluminium, with a pureness of 99.98 % is used in the inline system, 99.9998 % is used in the laboratory machine. Since it is possible that, in addition to other causes, those distinctions are responsible for the detected voltage decline in highly efficient solar cells, further experiments were carried out.

4 FURTHER EXPERIMENTS

A first experiment was designed to determine whether the evaporation process can have a negative influence on the front side of the solar cell, since it can not be ruled out that aluminum diffuses throughout the evaporation chamber and hence reaches the front side. Therefore we used 20 156x156 mm^2 sized ready-made solar cells with an aluminum BSF rear side. All of the wafers were driven through the machine under standard process conditions, but only ten of them received an evaporated aluminum layer of 2 µm since the other ten wafers were placed with their rear side on dummy wafers. A comparison of the open circuit voltage $V_{oc,2}$ after metallization and $V_{oc,1}$ before the PVD process is shown in Figure 3, where $\Delta V_{oc} = V_{oc,2} - V_{oc,1}$. Therefore, the positive value which can be seen at both groups indicates a voltage increase during the process. That is not a contradiction to the voltage decline that was detected before, since the cell structure totally differs from the highly efficient solar cells, but it is a clear sign that the front side is not affected negatively by any aluminum. The difference between both groups is not negligible and also indicates that the evaporation of the rear side can influence the cell performance. Thus it is very likely that the reason for the voltage decline is due to the rear side of the solar cells. Hence the loss can result either from the LFC contacts or the passivated area. Since the LFC process leads to an aluminum doped area underneath the contacts [9], it is possible that the lower purity of aluminum causes a higher recombination at these regions and consequently a lower voltage potential. To determine the recombination at single LFC contacts a certain procedure can be used based on measuring the effective surface recombination velocity S_{eff} in dependency of the covering fraction of LFC contacts. S_{eff} values are therefore derived from the lifetime of the minority charge carrier, which can easily

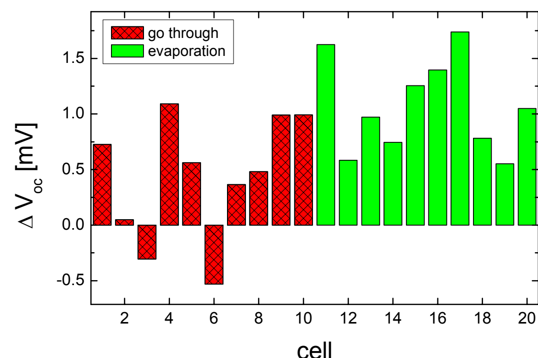

Figure 3: Gain in open curcuit voltage V_{oc} of ready-made solar cells after an additional process run with (green) and without (red) an evaporation of 2 µm aluminum on standard solar cells with aluminum BSF

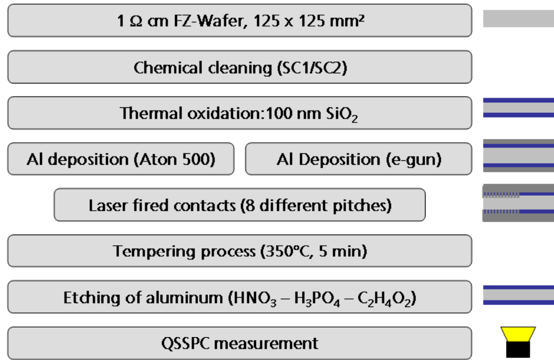

Figure 4: Process flow (left) and appearance (right) of samples to measure the minority carrier lifetime by means of QSSPC to determine the impact of different aluminum purities on the recombination current at LFC contacts.

be measured with symmetrically processed samples by Quasi Steady State Photo Conductance measurement (QSSPC) [10]. From the distribution of the S_{eff} values, the recombination velocity at the contacted area S_{met} [11], and the recombination current, which is caused by a single contact $I_{0b,LFC}$ can be derived [12].Therefore we prepared, as shown in Figure 4, two 125x125 mm^2 sized, shiny etched p-type 1 Ω*cm FZ silicon wafers with a SC1 SC2 cleaning sequence [13] followed by a 100 nm thermal SiO_2 passivation. Afterwards a 2 µm thin layer of aluminum was evaporated on both sides by standard processes by means of the different systems, leading to different aluminum purities on each sample. Later eight regions on each wafer were processed with a standard LFC process from both sides with different contact fractions and different contact pitch L_p. One part of the wafer was not covered with any contacts to derive the recombination velocity on the passivated area S_{pas}. After the LFC process a following annealing step at 350 °C for 5 minutes in forming gas is performed to improve the passivation quality and partly heal the laser damage before the aluminum is etched off with a HNO_3-H_3PO_4-$C_2H_4O_2$ solution in order to measure QSSPC [14]. From the determined lifetimes, the S_{eff} values are derived and plotted versus the contact pitch L_P in Figure 5.

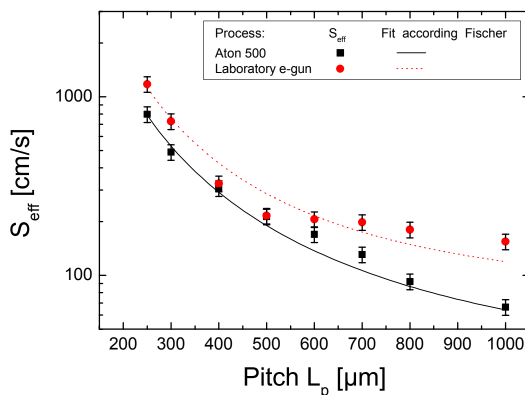

Figure 5: Effective surface recombination velocity S_{eff} versus contact pitch L_p for different evaporation processes and a fit of the data according to the Fischer equation [11].

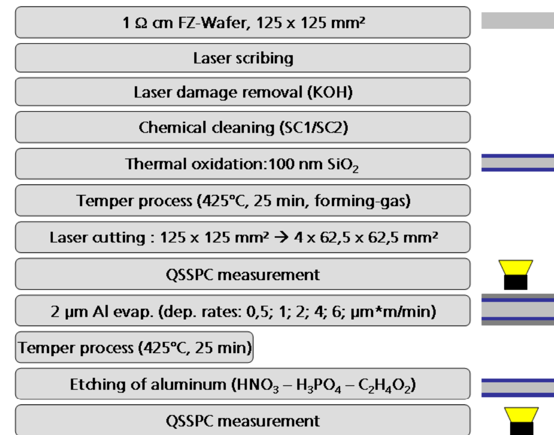

Figure 6: Process flow (left) and appearance (right) of samples to investigate the impact of evaporation processes with different deposition rates at the Aton 500 on passivation layers consisting of 100 nm thermal SiO_2.

Due to the non-uniform distribution of the S_{eff} values in the case of the “laboratory” evaporated sample, the uncertainty of the derived recombination current is vague and a comparison of these values difficult. Nevertheless, the difference of the two curves is obvious and clearly denotes the higher passivation quality in the case of the Aton 500 based process, as can be seen in the region of high pitches.

In the region of small LFC pitches and high contact fraction the S_{eff} values of those samples, which received aluminum by the Aton 500 process are lower, which shows that the recombination of the charge carriers at the contacts is smaller in this case. Consequently, the lower aluminum purity does not downgrade the cell performance, as already claimed by Grohe et al. [7]. To find out about any harming influence of the evaporation process on the passivation quality, we again processed symmetrically structured samples to measure the minority carrier lifetime by means of QSSPC. The process flow is shown in Figure 6. From the lifetime, the surface recombination velocity (SRV) can be derived by formula (1) [15].

$$S = \frac{W}{2}\left[\left(\frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{bulk}}}\right)^{-1} - \frac{1}{D}\left(\frac{W}{\pi}\right)^{2}\right]^{-1} \quad (1)$$

And from the latter, the dark saturation current density on the rear side j_{0b} can be calculated using formula (2) [16].

$$j_{ob} = \frac{q \cdot n_i^2 \cdot D_p}{L \cdot N_D} \cdot \frac{S \cdot \cosh\frac{W}{L} + \frac{D_p}{L}\sinh\frac{W}{L}}{\frac{D_p}{L}\cosh\frac{W}{L} + S \cdot \sinh\frac{W}{L}} \quad (2)$$

Moreover, according to the one diode model and equation (3), the upper limit of the voltage can be derived.

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{j_{lum}}{j_{0e} + j_{ob}} + 1 \right) \qquad (3)$$

Since in a similar former experiment at the Aton 500 that dealt with this issue an influence of the deposition rate was observed, we again used different evaporation processes with dynamic deposition rates of 0.5; 1; 2; 4 and 6 µm*m/min. At each process, the velocity of the samples in the machine was adjusted to receive an equal layer thickness of 2 µm. As in the previous experiment we used ten 125x125 mm^2 sized, shiny etched 1 Ω*cm FZ silicon wafers. First, they were marked by laser. Then a KOH dip was performed to remove the laser damage, followed by an additional wet chemical cleaning sequence (SC1/SC2), again to prepare the samples for the subsequent thermal oxidation of 100 nm SiO_2. Afterwards the samples were annealed for 25 minutes at 425 °C under a N_2H_2 atmosphere (anneal), divided by laser into four pieces, and the lifetime was determined for all 40 samples via a first QSSPC measurement at an injection level of $\Delta n = 5{*}10^{14} cm^{-3}$. Then the aluminum deposition was performed on both sides using each deposition rate for eight samples. Half of each group was annealed again at 425°C for 25 minutes (al-neal) before all the samples underwent a treatment in a HNO_3-H_3PO_4-$C_2H_4O_2$ solution in order to etch the aluminum for the final QSSPC measurement. The results of this measurement, which can be seen in Figure 7, show several different points:

- From the red hollow and bold symbols, respectively the lifetimes before and after metallization, it can be seen that the lifetime level remains constant for all different deposition rates (except 6 µm*m/min) and consequently none of these thermal evaporation processes has a harmful impact on the passivation.
- Looking at the difference between the bold blue squares and bold red circles, respectively the influence of the al-neal process, one can see the positive impact of this effect.

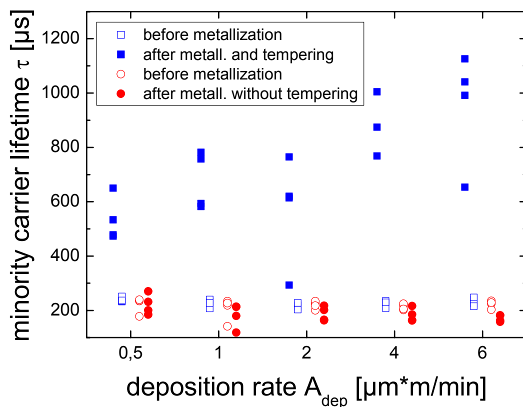

Figure 7: Minority carrier lifetimes measured via QSSPC on symmetric SiO_2 passivated FZ samples in dependence of the deposition rate of the metallization process with (blue squares) and without (red circles) an al-neal process before (hollow) and after (bold) the metallization or metallization plus annealing.

- In combination with an al-neal process, very high lifetimes above 1 ms can be reached.
- The lifetime and therefore the efficiency potential rises with increasing deposition rate.

The best minority carrier lifetime values vary between 650 – 1125 µs, depending on the different process parameters. According to formula (1), this results in a surface recombination velocity S between 12.8 – 4.7 cm/s for the given material - 1 Ωcm FZ wafer with thicknes W = 250 µm - assuming a bulk lifetime of τ_{bulk} = 3 ms (Auger limit) [17] and an diffusion constant D = 27.1 cm²/s. Using equation (2) we derive dark saturation current densities between 16.27 – 23.8 fA/cm^2, neglecting the negative impact of the LFC. Neglecting also the emitter recombination (j_{0e} = 0 fA/cm^2) and assuming $j_{lum} = j_{sc}$ = 40 mA/cm^2, the maximum voltage of such an device can be calculated by inserting the derived dark saturation current densities in formula (3) to 723 - 732 mV depending on the evaporation process. This high potential emphasizes the very high passivation quality, resulting from the investigated metallization process in combination with a thermal SiO_2 passivation and an al-neal annealing step. Consequently, this issue cannot be blamed for any voltage drop detected at previous highly efficient solar cells.

In summary, it can be noted that neither at the front side, nor the back side (LFC + passivated areas) could any reason for limits in V_{oc} potential up to a high level be found. Consequently it seems to be necessary to adjust the overall cell process to the new metallization process in order to reach the maximum efficiency potential. For several reasons it is likely that the annealing process needs to be changed:

1. The temperature and hence the annealing process can have a serious impact as seen in the previous experiment.
2. The temperature of the samples differs strongly during the Aton 500 and the e-gun laboratory process.
3. Despite using the same silicon material, passivation, evaporation and annealing process for the solar cell batch and the previous experiment, the supreme quality of the passivation as seen in Figure 7 can not be directly assigned to the solar cells. This is due to the fact that the “lifetime samples” underwent two evaporation processes in order to process them symmetrically. The second evaporation leads to an additional undefined temperature rise of the sample that does not take place during the cell processing sequence and can therefore improve the passivation quality significantly.
4. As seen in Figure 5, the kind of metallization process performed by the Aton 500 has no negative impact on the quality of the LFC process. Beside this laser process, the annealing step is the only process remaining in the process chain of solar cells.

5 INVESTIGATION ON THE INFLUENCE OF THE FINAL ANNEALING PROCESS

To determine the influence of different final annealing processes, we manufactured another batch of highly

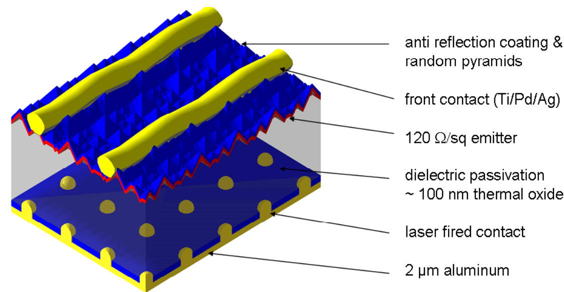

Figure 8: Schematic structure of the highly efficient solar cell used to determine the potential of different evaporation and annealing processes.

efficient solar cells where aluminum evaporation was done with different deposition rates at the Aton 500 and the e-gun reference process. This batch contains 25 p-type 1 Ohm*cm float zone silicon wafers, each containing seven 20x20 mm² cells. The cells feature a deep phosphorous emitter with a sheet resistivity of 120 Ohm/sq on a random pyramid textured surface and a 100 nm thick thermally grown SiO_2 front and rear side passivation. The photolithographically defined front contact grid consists of an evaporated thin TiPdAg stack which is thickened by electroplating in silver. For the 2 µm thin aluminum layer on the rear side, we use the thermal evaporation process with five different deposition rates between 0.5 – 6 µm*m/min as well as the reference e-gun process, each on four wafers (28 cells), followed by the LFC contact formation. It should be stated that the opening of the SiO_2 and the subsequent PVD processes on the front side were carried out after the rear side metallization was finished to avoid any influence of the different temperature characteristic on the front side contacts. Half of the batch, 2 wafers (14 cells) per process, was annealed at the standard annealing process for such cells for 25 minutes at 425°C under forming gas in a tube oven. Afterwards I-V as well as SunsVoc measurements were performed and the voltage potential was compared [18]. From Figure 9 it can be seen that again the voltage level of the e-gun reference process fell short by ~ 5 mV.

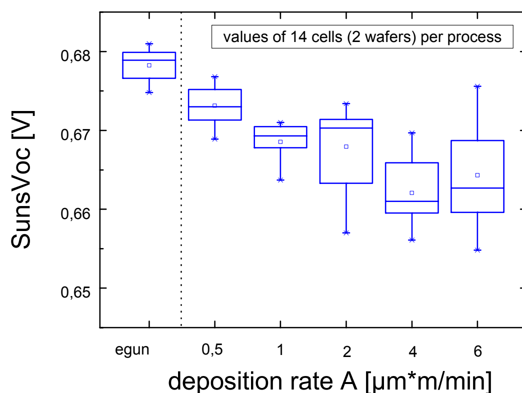

Figure 9: V_{oc} values measured by SunsVoc in dependence of the rear side metallization process after receiving a standard forming gas al-neal at 425°C for 25 minutes.

Additionally it can be seen that the voltage potential decreases further with increasing deposition rates at the Aton 500, which is in contrast to the results from the lifetime measurement in Figure 7, showing that indeed these results can not be devolved to the conditions in real solar cells. From the second half of the batch, individual cells were cut out of the wafer by laser and measured via SunsVoc to determine the voltage potential before annealing. Afterwards, to investigate the impact of annealing time, single cells were put under normal atmosphere on a hotplate for a certain, comparable short period of time of 1 minute and measured again via SunsVoc. Then, to insure that only the effect of the annealing is seen in the voltage development the same cell is annealed and measured again. This action is repeated until the voltage decreases or several minutes of accumulated annealing time is reached. The whole procedure is carried out at different hot plate temperatures T of 300, 350, 400, 450 and 500°C. To compare the influence of different evaporation processes, cells with similar voltage before the first annealing step were chosen. In Figure 10 the voltage characteristics of the annealing experiment is shown on the right side in the case of a medium deposition rate A_{dep} of 1.5 µm*m/min. Additionally, the distribution of the voltages measured by SunsVoc of the 14 reference cells (e-gun evaporation + standard annealing 424°C, 25 min) of the first half of the batch is shown on the left side.

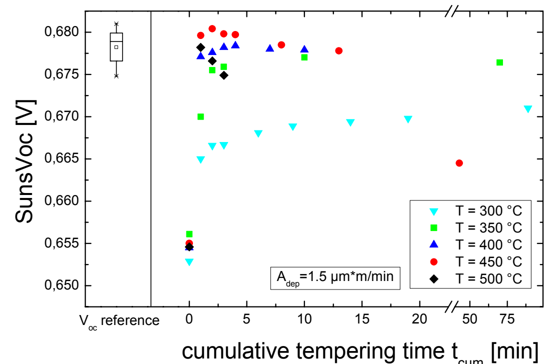

Figure 10: Measured SunsVoc values in dependency of the cumulative annealing time on a hotplate at different temperatures for highly efficient solar cells, which received rear side metallization by the Aton 500 with a deposition rate A_{dep} of 1.5 µm*m/min compared to the level of the reference cells with e-gun evaporation and standard annealing (left).

The following behaviour can be observed:

1. Regarding the V_{oc} value before annealing ($t_{cum} = 0$), the positive effect of this annealing process in general is obvious.
2. Until a temperature T = 400°C the voltage increases with increasing annealing time or stays at a constant level for several minutes.
3. Above temperatures T > 400°C the voltage reaches a maximum level within the first three minutes and decreases afterwards with further annealing time.
4. This decrease starts earlier and is steeper with increasing annealing temperature.
5. The gain in V_{oc} increases with higher temperature T until 450°C.

6. It seems possible that the voltage still improves when being annealed at 500°C for less than one minute.
7. The voltage potential of the reference process, which can be seen on the left side, is reached.

To learn about the influence of the different evaporation processes, the SunsVoc values at consistent annealing conditions are compared in Figure 11. Therefore an annealing process at 450°C is chosen, since this leads to the best results at medium deposition rates.

The following characteristics can be derived:
1. For all deposition processes, the maximum voltage is reached after two to three minutes.
2. The maximum level is higher in combination with higher deposition rates, which is in accordance with our results regarding the passivation quality in an earlier experiment (see Figure 7).
3. The e-gun process (black rhombus) starts at a much lower level before the first annealing process due to the harming effect of the x-ray irradiation during the process.
4. The reference level is already reached with deposition rates A_{dep} = 1.5µm*m/min.
5. The e-gun evaporated samples also benefit from the altered annealing condition but do not outreach those deposited with the inline process any more.

Although a reliable conclusion can not be derived from only one solar cell, it seems possible that with high deposition rates the voltage potential of the reference process can be exceeded. Therefore the measured voltages at different hotplate temperatures in combination with an aluminum evaporation process featuring a deposition rate of 6 µm*m/min are plotted in Figure 12. At a temperature of 500°C the first two annealing periods at the beginning were decreased to 30 seconds, resulting in the highest values besides one runaway value at 400°C. It should be pointed out that at this deposition rate, the voltages after annealing at T = 400, 450 and 500°C all clearly exceed the reference process.

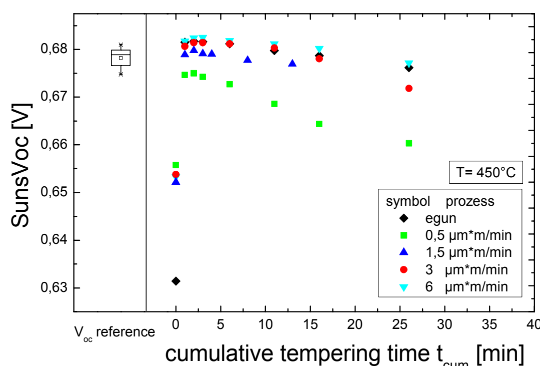

Figure 11: Measured SunsVoc values for highly efficient solar cells in dependency of the cumulative annealing time on a hotplate at a temperature of 450°C for different rear side aluminum evaporation processes.

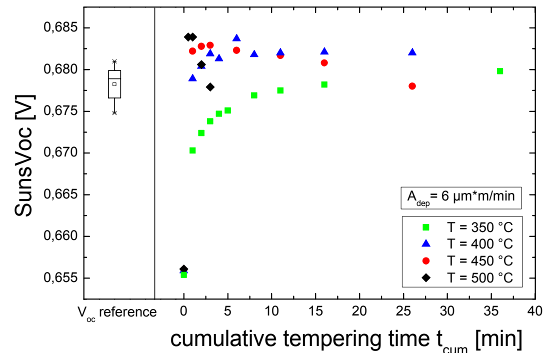

Figure 12: Measured SunsVoc values in dependency of the cumulative annealing time on a hotplate at different temperatures for highly efficient solar cells, which received rear side metallization at the Aton 500 with a deposition rate A_{dep} of 6 µm*m/min compared to the level of the reference cells with e-gun evaporation and standard annealing (left).

6 SOLAR CELL RESULTS

After annealing on the hotplate was finished, the I-V characteristic of the most promising cells was measured. Since the loss in voltage occurred quickly at higher temperatures at the end of the experiment, most of the cells annealed at T= 400°C still had a voltage level close to their maximum potential. Consequently, cells that were not processed ideally were measured.

Table 1: Solar cell parameters of the most promising but not ideally annealed solar cells, which run trough the former anneal process investigation.

Process	A_{dep} [µm*m/min]	V_{oc} [mV]	j_{sc} [mA/cm^2]	FF	η [%]
e-gun		678.9	39.5	80.5	21.6
Aton	1.5	675.2	39.3	81.6	21.6
Aton	3	679.2	39.1	81.9	21.8
Aton	6	678.7	39.6	80.6	21.6

However, the results seen in Table 1 point out two major results:
1. The open circuit voltage of the reference laboratory e-gun process is reached even by different evaporation processes with the Aton 500 system.
2. The industrial feasible inline evaporation process leads to the highest efficiencies η of 21.8 % reported to the knowledge of the authors with this cell structure on silicon material with a base resistivity ρ of 1 Ω*cm.

7 CONCLUSION AND OUTLOOK

In this paper we showed first that the voltage decline, which was regarded earlier in combination with the investigated inline metallization PVD process, does not result from the front side or any harmful influence on the rear side. Instead it is shown that this metallization

process requires an adopted annealing process in order to achieve perfect passivation quality.
Annealing experiments carried out on a hot plate with highly efficient solar cells indicate that temperatures above 450°C are necessary to obtain the maximum potential. In contrast, very small annealing periods as short as 30 seconds to 3 minutes, depending on the used temperature, are needed. Additionally it is shown that high aluminum deposition rates are preferable, since they also increase the efficiency potential. This can be due to a denser layer at the interface, since a higher deposition rate comes along with higher machine power, boat temperature and vapour density and thereby probably higher particle velocities. Still, this is speculation and further investigations need to be carried out.
In combination with an optimized annealing process, the voltage potential exceeds that of the laboratory e-gun reference process. Finally, even with a non-ideal process, solar cell efficiency η of 21.8 % could be reached.

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SOLDERING OF CRYSTALLINE SILICON MODULES: LOSSES, RELIABILITY AND IMPROVEMENTS

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ABSTRACT: In the standard process for manufacturing crystalline silicon modules the cells are soldered to each other with flat tinned copper ribbons. Strings of 8 to 12 cells are then interconnected with bussing ribbons, which are finally fed into the junction-box. Joule losses and additional shading losses from these ribbons are discussed and the effect of an increased number of bus bars is calculated on the cell and on the module level. The reliability problems of soldered ribbons on sintered silver bus bars are highlighted and a list of alternative materials for soldering ribbons and an overview on more innovative interconnection technologies are given and commented.

1 INTRODUCTION

The flat copper ribbons used as cell-to-cell interconnects in the standard crystalline silicon module production are introducing additional electrical and optical losses in the modules. At the same time the soldering step remains the major yield loss in terms of cell breakage in the module production. The target of getting larger and thinner in the cell dimensions will even enhance these problems. Although, there are new contact formation schemes under investigation on the cell level, the soldering approach remains a well established interface between cells and modules and therefore not easy to replace, blocking contact innovations on the cell.

A second issue is the annual degradation rate of crystalline silicon modules, which is numerated with 0.3% to 0.5% per year in standard energy yield calculation programs or more than 1% per year in [1]. Apart from the initial degradation during the first hours of operation, the annual degradation in the field is said to consist of a decrease in the short circuit current I_{sc} from transmission losses of the encapsulant and a decrease in the fill factor *FF* from increasing series resistance losses at the cell contacts and interconnects [2].

Manufacturability, reliability and module efficiency are of equal importance in the evaluation of new contacting schemes on the cell level and new approaches to interconnect the cells on the module level..

2 LOSSES FROM SOLDERING

Fig. 1 sketches a string of silicon cells soldered by flat tinned copper ribbons from back to front.

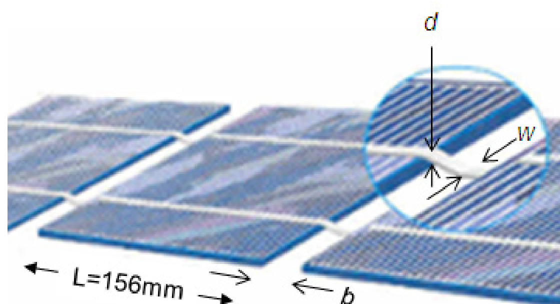

Figure 1: Interconnection from cell to cell with tinned copper flat wires in crystalline Silicon PV modules

The losses for the front ribbons (Eq. 1), back ribbons (Eq. 2), ribbons between the cells (Eq. 3) and additional shading from the ribbons (Eq. 4) are:

Front: $$\frac{P_{loss,front}}{P_{\max}} = \rho_{Cu} \cdot \frac{L}{3 \cdot n_{busbar} \cdot w \cdot t} \cdot \frac{I_{MPP}}{U_{MPP}} \quad (1)$$

Back: $$\frac{P_{loss,back}}{P_{\max}} = \frac{1}{\frac{w \cdot t}{\rho_{Cu}} + \frac{L \cdot t_{Al}}{\rho_{Al\ paste}}} \cdot \frac{L}{3 \cdot n_{busbar}} \cdot \frac{I_{MPP}}{U_{MPP}} \quad (2)$$

Spacing: $$\frac{P_{loss,spacing}}{P_{\max}} = \frac{\rho_{Cu}}{w \cdot t} \cdot \frac{b}{n_{busbar}} \cdot \frac{I_{MPP}}{U_{MPP}} \quad (3)$$

Shading: $$\frac{P_{loss,shading}}{P_{\max}} = \frac{n_{busbar}(w - w_{busbar})}{L} \quad (4)$$

The ribbon losses in Fig. 2 are calculated with a cell edge length L= 15.6 mm, ribbon width w = 2.3 mm, a bus bar width w_{busbar} = 1.5 mm, ribbon thickness t = 0.15 mm, spacing between the cells in the module b = 3 mm and number of bus bars n_{busbar} = 2 and I_{MPP} = 7.9 A and U_{MPP}= 0.508 V for the cell's maximum power point, the specific resistance of solid copper ρ_{cu} = 1.8·10^{-8} Ωm and sintered Aluminium $\rho_{Alu,paste}$ = 2.9·10^{-9} Ωm and its thickness t_{Al} = 15 µm. The additional power loss in the Aluminium paste in Eq. 2 was determined by measuring the voltage drop over the length of the copper ribbon before and after soldering the ribbon on to the back of the cells. In [3] the resistivity of the back aluminim paste was neglected, what underestimates the loss. While in [4] the losses were overestimated from assuming the same soldering losses for the front as for the back side.

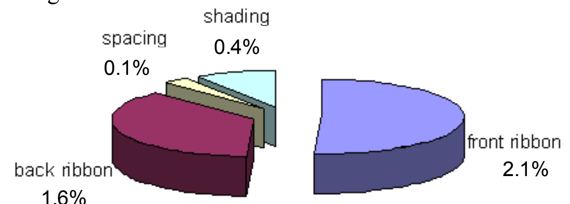

Figure 2: Ribbon losses for a 156mm 2 bus bar cell

The resistance losses of the contact between the solder, i.e. the tin-silver alloy coating of the ribbon, and the sintered silver bus bars of the cells are neglected. Despite of the by 6 times lower conductivity of the solder compared to copper, the solder forms a full area contact

with the bus bar. However, compared to the contact losses from the finger probes in the cell testing, it is not clear, if the solder contact is a loss or gain.

Table 1: Encapsulation and soldering losses for 60 cell modules with 156 x 156 mm² two bus bar mono (Impp = 8 A) crystalline, acidic (7.9 A) and alkaline (7.5 A).textured multi crystalline silicon cells.

Cell-to-module gains/losses	mono	multi acidic	acidic alkaline
Δ Isc from optical match	-1.3%	1.8%	3.7%
ΔIsc ribbon shading (Eq. 4)	-0.38%	-0.38%	-0.38%
ΔUoc	-	-	-
ΔFF ribbon (Eq. 1- 3)			
(2 x 0.15mm x 2.3mm)	-3.83%	-3.78%	-3.63%
ΔFF bussing (1.4m x 1mm²)	-0.68%	-0.67%	-0.64%
ΔFF cable (1.1m x 4mm²)	-0.26%	-0.26%	-0.25%
total	-6.5%	-3.3	-1.2%

The optical losses in Table 1 were measured on single cell modules with an opaque surrounding frame to simulate the 3mm cell spacing. Because of the optical losses in: I_{sc}, the total losses are higher for mono cells.in Table 1: Due to their more effective texturisation, the lower reflectance of the mono cells in air leaves less space for the decrease of the reflection losses by the encapsulant [6]. The optical losses of alkaline textured crystalline silicon cells were reported to be by 2.1% relatively lower than for alkaline textured cells in [7], i.e. the flater the cell's surface, the more pronounced are the optical encapsulation gains.

Table 2: Relative ribbon losses for two and three bus bars with typical dimensions for bus bars and ribbons for 156 mm cells, 0.2 mm thickness is a limit in the industry

Ribbon thickness	loss (2 bus bars)	loss (3 bus bars)
0.10 mm	5.8%	5.0%
0.15 mm	4.2%	3.8%
0.20 mm	3.3%	3.2%
Width of Bus bar/Ribbon:	2 mm/2.3 mm	1.5 mm/2 mm

Table 2 is comparing the calculated losses for two and three bus bars cell designs from Eq.1-4. These losses are visible as a fill factor drop at the module tester independent from the optical losses above. The three bus bar design leads to an improvement of 0.4% relative for a 0.15 mm thick ribbon, where the ribbon width is reduced from 2.3 mm to 2 mm in the industry at the same time.

Figure 3 demonstrates, that the bus bar and ribbon width of 1.5 and 2 mm for 2 and three bus bars cells in table 2 are near the calculated optima, where the ribbon width are chosen up to 0.5 mm wider with the intention to tolerate positioning errors in the soldering step.

The higher number of bus bars increases the cell efficiency on the cell level as well. Because of the shorter finger length, the current is collected much more efficient on the cell. The decrease of the unit cell comes already to full effect at the cell tester, where more finger probes are used to access the third bus bar. There is an on-going discussion between cell and module manufacturers, who benefits more from additional bus bars.

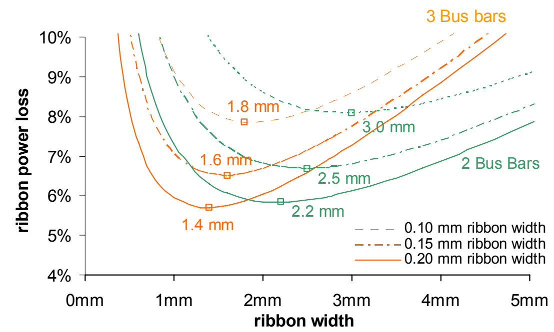

Figure 3: Ribbon losses for 156 mm two and three bus cells calculated with bus bar width w_{busbar}= 0 (i.e. shading losses are shifted completely to the ribbon).

The calculation of the power loss in the grid fingers of the cell [5] follows the same scheme as for the front ribbon in Eq. (1):

$$\frac{P_{loss,finger}}{P_{max}} = \rho_{Ag\ paste} \cdot \frac{d_{finger} \cdot L_{finger}^2}{3 \cdot w_{finger} \cdot t_{finger} \cdot L^2} \cdot \frac{I_{MPP}}{U_{MPP}} \qquad (5)$$

The specific resistance of the silver paste is $\rho_{Ag,paste} = 3 \cdot 10^{-8}\,\Omega$m, the finger width w_{finger} = 100 µm and the finger thickness t_{finger} = 5 µm.
The unit cell is defined by the area given by $d_{finger} \cdot L_{finger}$, where d_{finger} is the distance from finger to finger and L_{finger} is function of the number of bus bars with $L_{finger} = \frac{1}{2} \cdot (L/n_{busbar} - w_{busbar})$.

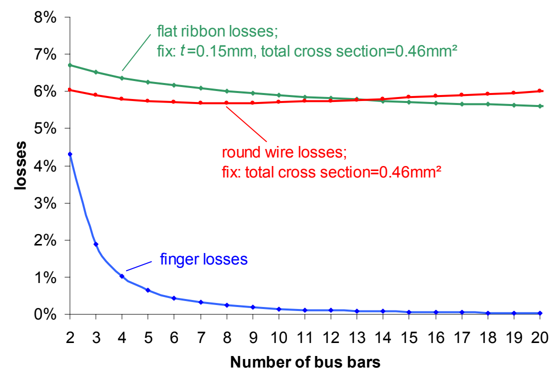

Figure 4: Relative ribbon losses from Eq. 1-4 and finger losses for 156mm cells from Eq. 5 vs. number of bus bars with constant total cross section of 0.46 mm² and constant thickness of t = 0.15 mm for flat wires. For 14 bus bars the flat ribbons are 0.33 mm wide. In the case for round wires it is a diameter of 0.1mm.

Because of the decreasing finger length, the finger losses drop under 0.1% for 12 bus bars. For the flat ribbons, the losses are decreasing with the number of bus bars. The losses for the round wires show a minimum at 8 bus bars with a diameter of 0.27 mm and the diameter undergoes 0.15 mm for more than 26 bus bars. The shaded area from the round wires increases with the square root of the amount of bus bars. For the flat ribbons, the shaded area was kept constant and because of this, the aspect ratio of thickness to width increases to higher number of bus bars.

Changing from 2 to 3 bus bars means a fill factor loss reduction of 2.4% relative in Fig. 4. In the experiment, it was only 1.5%, when shading one third of the active areas on both sides of the bus bar on a two bus bar cell.

The difference to the calculated value might be due to the relative increase of the dark current, which remained unchanged under shading.

In summary, an increase of the number of bus bars can reduce the fill factor losses by 3% relative and up to 6%, where roughly 80% takes place on the cell level and 20% on the module level.

The possible reduction of the finger width when using more bus bars was not considered here, because their minimum width is fixed by the limits of the actual screen printing technique. This might change within future developments and new metallisation schemes.

3 RELIABILITY OF SOLDERED INTERCONNECTS

The constructional design of photovoltaic modules needs to withstand temperature changes in the range of -40°C to 85°C.

Table 3: Different expansion coefficients for materials used in standard crystalline silicon modules

Material	thermal expansion (K^{-1})	E-module (GPa)
Silicon	2E-06	160
Glass	9E-06	70
Copper	1.7E-05	130
Back sheet	3E-4	0.02

The back sheet polymers show the highest value for the thermal expansion, but because of the low E-modulus, photovoltaic modules show only a slight bending to the front after lamination at 150°C. But after module breakage this is clearly visible. The higher glass expansion compared to silicon leads to a compression of the solder ribbons between the cells, which is not giving problems so far.

The coefficient for copper is nearly one order of magnitude higher than for silicon, which leads to cell bowing after stringing parallel to the bus bars and as well to shear forces of the ribbon over the width of the bus bar in perpendicular direction.

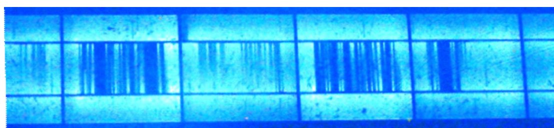

Figure 5: systematic finger interruptions at the bus bar edges after cell soldering in the module production

The electroluminescence image in Fig. 5 shows finger interruptions near the bus bars after soldering on an automated production stringer, while power losses were detected on the finished module. Silicon fracture under the printed front grid were reported as a root cause for these interruptions in [8]. This was supported by FEM Simulation of the tensile stress over the ribbon width after soldering.

The following approaches have been proposed in the past to release the thermal mismatch between the copper ribbons and the silicon cell:

- softer copper ribbons (Yield strength < 95MPa)
- narrower soldering contact area
- Multi wire ribbons
- Low melting solder, e.g. SnBi or SnBiAg
- lower CTE value than Copper, e.g. Cu-clad Ni-Fe Invar wire (CIC) in [9]
- more bus bars, but thinner ribbon

The stress is released either by lower mismatch in the thermal expansion coefficients, lower temperatures or less or softer material.

In addition to this systematic conflict, the most frequent problems for soldering copper ribbons to silicon cells are:

1. Silicon fracture under the bus bars (cratering)
   - solder temperature too high
   - cooling too fast

2. Bad wetting
   - solder temperature too low
   - bad flux
   - bus bar is oxidised from bad cell storage
   - missing solder (standard: 10-15 µm)

The soldering process is evaluated through peel-off tests to monitor the bonding force and silicon fracture or bad wetting by subsequent visual inspection. Because these tests are destructive, they are performed on broken or discarded cells in the production. Fig. 6 shows the peel-off test comparing automated soldering and manual soldering:

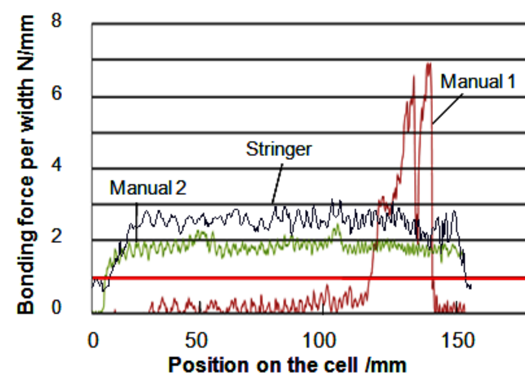

Figure 6: Comparison of bonding forces between manual and automated soldering on a stringer. “Manual 1” and “Manual 2” are taken from different bus bars of the same cell, cell thickness: 160 µm

The red line in Fig. 6 at 1 N/mm denotes the accepted industry standard for the bonding force of soldered cells. Although manual soldering often deviates from this value and even fluctuates by one order of magnitude on the same cell, there is no evidence so far, that manually soldered modules are less reliable in the field or in the IEC tests than those from automated soldering. The accepted threshold is apparently larger than necessary for reliability needs. Anyway, higher and more constant bonding forces are more redundant, but this seems not to be an urgent need in the field. The stress on the cells is compressive in regard to 85°C as the highest operating temperature and the fixation temperature of the module components - solidification of the solder at 220°C, curing of the encapsulant at 150°C. At the moment, corrosion effects are used to explain series resistance increases over 20 years in the field, moreover than effects from thermal fatigue. But this is indeed still unclear and under investigation. The threshold value of 1 N/mm reflects at

least, what is feasible with automated stringers.

Reliability problems from other parts of the electrical circuit in the module, e.g. soldered ribbon-to-ribbon interconnects and more recently soldered j-box interconnects, were solved by changing the product design.

In summary, soldering is preferably avoided in outdoor applications or kept as redundant as possible, e.g. with continuous soldering of the ribbons on the cell or at least with the maximum number of solder spots.

4 IMPROVEMENTS AND NEW CONCEPTS

Soldering with ribbons on screen printed bus bars is very well established and its long-term stability is proven in the field.

But in respect to the remaining reliability issues shown above and the need for further cost reductions and efficiency improvements, the following approaches have emerged as alternative module concepts:

- Spherical cells from Texas Instruments (now Matrix), Scheuten (CIGS thin film), Kyosemi, Spheral SolarPower and Fujiprea
- PUM concept from ECN: back contact cells with a structured interconnecting back sheet, allowing larger cells through connecting smaller unit cells
- SunPower/Advent: current collection without ribbons on the cell, up to now limited to 125 mm cells
- Sliver from Origin: slim cell stripes from a wet etching process, which are connected in series for high voltage cells. These cells are connected in parallel in the module
- On-laminate soldering of back contact cells from ISFH in Hameln,Germany
- Day4Energy with high a number of low-melting solder wires, which are soldered perpendicular to the fingers without bus bars
- HD cell (Honeycomb Design) from Sanyo and QuarterCells from Powerquant, splitting of one cell in four cells in series

These approaches all benefit from smaller current densities in the interconnecting ribbons, which lead to higher fill factors in the module.

Although most of them are originally motivated by manufacturability, better silicon usage or higher cell efficiencies, some of them use smaller cells to increase the module fill factor as in the case of Sanyo's and Powerquant's quarter cells. Day4Energy's multi wiring approach accomplishes this also on larger cells by reducing the unit cell [10]. The back contact cell concepts enable much more conducting material without shading limits, either on the cell like SunPower or on the back sheet like ECN. But in both cases, there are still disadvantages to overcome on the cost side.

5 CONCLUSION

The standard soldering scheme with two or three ribbons per cell has its limits in further efficiency increases and reliability, but it is a proven standard interface between cell and module and therefore difficult to replace.

The use of more interconnects is increasing the fill factor and the reliability on the module level. In an innovative approach, the single unit cells are accessed separately instead of collecting their currents in bus bars re-enforced by the copper ribbons. At first, fine metal contacts without limiting constraints on series resistances are requested on the cell side. In the second step, wires or ribbons are used to connect all unit cells of one cell to the next cell, either by soldering, bonding or gluing. This raises the question, if the latter will be part of the cell or of the module manufacturing and reminds on the vision of many module manufacturers asking for a cell with "plugs on board".

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