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# Manufacturing 100-μm-thick silicon solar cells with efficiencies greater than 20% in a pilot production line

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Reducing wafer thickness while increasing power conversion efficiency is the most effective way to reduce cost per Watt of a silicon photovoltaic module. Within the European project 20 percent efficiency on less than 100-μm-thick, industrially feasible crystalline silicon solar cells ("20plμs"), we study the whole process chain for thin wafers, from wafering to module integration and life-cycle analysis. We investigate three different solar cell fabrication routes, categorized according to the temperature of the junction formation process and the wafer doping type: p-type silicon high temperature, n-type silicon high temperature and n-type silicon low temperature. For each route, an efficiency of 19.5% or greater is achieved on wafers less than 100 μm thick, with a maximum efficiency of 21.1% on an 80-μm-thick wafer. The n-type high temperature route is then transferred to a pilot production line, and a median solar cell efficiency of 20.0% is demonstrated on 100-μm-thick wafers.

**1 Introduction** The 2010 International Technology Roadmap for Photovoltaics (ITRPV) predicted that a large reduction in silicon solar cell wafer thickness was necessary to realize a steep decrease in cost per Watt of solar energy [1]. By 2020, the wafer thickness in industry was expected to reach 100 μm and, though ITRPV has since pushed back this date to 2023 in light of recent market developments [2], a reduction in wafer thickness paired with an increase in device efficiency remains the most effective way to reduce cost per Watt of a silicon solar module. Thinner wafers can be exploited not only to lower silicon consumption, but also to simultaneously yield higher efficiencies if surface passivation (to increase open-circuit voltage) and light management (to mitigate short-circuit current losses) are very good.

The average silicon consumption shrank from about 11–12 g/$W_P$ more than 10 years ago to about 8 g/$W_P$ in 2010. During the same period, the wafer thickness was reduced from 330 μm to around 200 μm while more than doubling

the cell area to the current 225 $cm^2$. Today's standard silicon solar cells are still 160–180 μm thick. However, SunPower recently reduced wafer thickness in production to 135 μm using a diamond-wire saw while at the same time increasing module efficiency to up to 21%, with the consequence that they have a silicon consumption of only 4.2 $g/W_P$ [3]. Last year, Panasonic demonstrated even thinner solar cells on 98-μm-thick wafers with higher cell efficiencies of 24.7%, but this achievement occurred in a research and development setting and has not yet been transitioned to production [4].

In this contribution, we demonstrate silicon solar cells with wafer thicknesses of 100 μm and efficiencies above 20% fabricated in the pilot production line of Hanwha Q CELLS. To reach these values, we first investigate three industrially feasible cell fabrication routes and focus on five research areas that are key to achieving high-efficiency and manufacturable cells on thin wafers: wafering, handling, surface passivation, light management, and metallization. We also present complementary cost and life-cycle analysis for the three different solar cell fabrication routes.

## 2 Experimental

**2.1 Solar cell fabrication routes** Three different solar cell fabrication routes, distinguished by the temperature of the emitter formation process and the wafer doping type, were investigated: p-type silicon with a high-temperature emitter (PHT), n-type silicon with a high-temperature emitter (NHT), and n-type silicon with a low-temperature emitter (NLT), see Fig. 1.

All silicon wafers were (100) Czochralski (CZ) with a resistivity of 1–5 Ω cm, unless otherwise stated, and cell fabrication was performed after alkaline texturing and cleaning. Wafer thinning to the desired thickness was achieved via a prolonged saw-damage-removal etch step. The high-temperature emitters were realized by diffusion from phosphorous oxychloride ($POCl_3$) or boron tribromide ($BBr_3$) sources, or from screen-printed aluminum. The low-temperature emitter is a hetero-emitter based on amorphous silicon (a-Si:H) layers deposited by plasma-enhanced chemical vapor deposition (PECVD). Additional fabrication details are given throughout this paper as appropriate. Figure 1 illustrates the different cell concepts investigated here according to the three fabrication routes. For the NHT route two different approaches were studied: a front-emitter cell, $NHT_{front}$, and a rear-emitter cell, $NHT_{rear}$. In addition to the full area rear metal as shown in Fig. 1 also bifacial solar cells with contact fingers at the front and at the rear side of the solar cell were investigated.

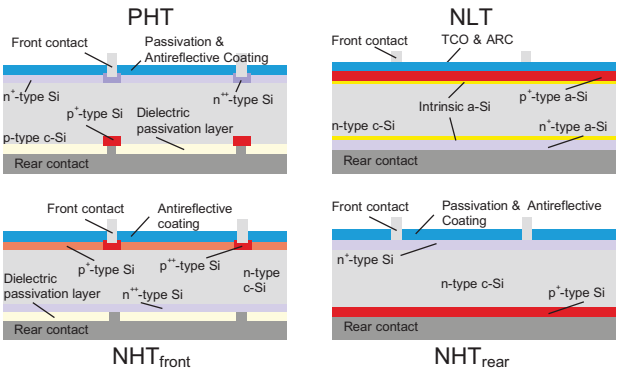


**Figure 1** Solar cell fabrication routes: PHT, NLT, and $NHT_{front}$ and $NHT_{rear}$.

**2.2 Challenges of 100-μm-thick silicon solar cells** Wafers only 100 μm thick hold specific challenges which are particularly crucial for the optimization of solar cell efficiency and manufacturing, as mentioned above.

The *wafering* of ingots for the current standard wafer thickness of 180 μm is conventionally carried out using a multi-wire slurry saw [5]. A stainless steel wire runs in one direction between two wire guide rollers, and an abrasive slurry containing silicon carbide (SiC) particles of a suitable diameter is added as a cutting fluid. Typically wafers sawn this way are thinner where the wire enters the cut compared to where it leaves the cut due to the larger diameter of the SiC particles at the wire entrance compared to the wire exit [6]. This total thickness variation (TTV) is in particular detrimental if the wafer becomes thinner, as the relative thickness variation will rise. Here, we compared the slurry sawing method with diamond wire and structured wire sawing. An additional challenge is the development of a thin-wafer sawing process with high yield; gluing the ingot to a glass plate and separating the wafers after the process are especially critical steps. We paid special attention to the post-sawing treatment of the wafers, which is important for the mechanical stability of the wafers, and breakage tests were carried out to assess the impact of the sawing and etching parameters on wafer strength.

The *handling* of 100-μm-thick wafers also needs to be adapted; standard vacuum grippers have local points of contact (typically four), at which significant stress is induced due to the thin wafer's flexibility. We developed a gripper based on Bernoulli forces that floats the wafer and does not make local contact. The Bernoulli gripper was tested at Hanwha Q CELLS.

*Surface passivation* becomes more crucial for thinner wafers because an increasing number of minority charge carriers reach a surface within their lifetime, and their non-radiative recombination needs to be avoided. Standard industrial solar cells feature an aluminum back-surface field (BSF) and a silicon nitride ($SiN_x$:H) layer for front side passivation The back surface field (BSF) in particular provides insufficient passivation for high efficiencies. Here, aluminum oxide/silicon nitride ($Al_2O_3/SiN_x$:H) stacks for PHT solar cells, and silicon dioxide/silicon nitride ($SiO_2/SiN_x$:H) stacks were investigated for both PHT and NHT solar cells, taking into account the anti-reflection properties of these layers and the industrial feasibility of their deposition. For the NLT route, intrinsic a-Si:H layers were deposited to passivate the silicon surface prior to deposition of the doped a-Si:H emitter and BSF.

Absorption of incoming light decreases significantly with decreasing cell thickness since silicon is an indirect semiconductor and thus the absorption probability is low for near-bandgap wavelengths. Wang et al. calculated that a 500-μm-thick silicon wafer absorbs 100% of the "usable photons" of the AM1.5 spectrum while a 100-μm-thick wafer absorbs only 95% [7]. For high efficiencies, no incoming light should be wasted, and thus device structures incorporating *advanced light management schemes* for minimizing the associated current loss are quantified and validated. In particular, diffractive rear reflectors were fabricated and measured, and – for the NLT route – new front a-Si:H layers and transparent conductive oxide (TCO) layers that reduce parasitic absorption were investigated.

The current standard *metallization* technique is screen-printing of metal pastes: silver for the front fingers and busbars, and aluminum for the full-area rear contact. The screen-printing process itself has the potential to break thin wafers. In addition, the aluminum rear contact induces a bow in the wafer, which becomes larger the thinner the wafer [8]. We both adapted the screen-printing process and evaluated low-mechanical-impact metallization techniques like plating.

Finally, the challenges of high-volume production of high-efficiency solar cells on thin wafers were tackled for the NHT route in a pilot production line, and cost and life-cycle analysis was used to examine the pros and cons of the three different routes in production.

## 3 Results and discussion of key topics

**3.1 Wafering** The present industrial standard wafering process is optimized for the production of wafers with a thickness of 160–180 μm. To cut thinner wafers with a standard wire saw, the pitch of the wire guide rollers was reduced and different types of wire were investigated. The thickness, roughness, saw damage, and breakage behavior of the cut wafers were then characterized. By iterative process development, a suitable sawing process for wafers $\leq$100 μm in thickness was achieved.

We observed that the sawing process is improved by reducing the surface roughness of the sawn wafers. This was achieved by using an F800 grit slurry, which has a small mean SiC particle diameter of $d_{50} \approx 6.5$ μm, i.e. 50% of particles have a diameter smaller and 50% larger than 6.5 μm. The slurry sawing process is dominated by brittle material removal, which consists of stochastic indentations of SiC particles into the wafer. Figure 2 shows the measured thickness variation of a nominally 90-μm-thick as-cut wafer that was cut using this slurry. The wedge shape of the wafer resulting from SiC particle erosion and drainage is visible; the wire entered from the left side of the image. One solution to avoid the wedge shape is to use an advanced sawing technique.

Diamond wire was anticipated to be suitable for cutting thin silicon wafers due to its lesser saw damage compared to slurry-based sawing. In addition, because the diamond particles on the wire surface are fixed, higher forces can be transferred to the silicon and therefore higher feed rates are possible. However, diamond-wire-sawn wafer surfaces show sawing grooves which are caused by the ductile silicon material removal process that dominates this type of sawing. The results of test cuts showed that, because of these grooves, diamond-wire-sawn wafers are more fragile than slurry-sawn wafers when bending them parallel to the wire direction.

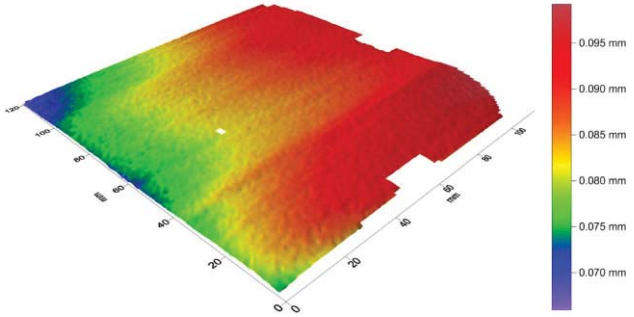


**Figure 2** Measured thickness variation of a nominally 90-μm-thick as-cut silicon wafer cut with a SiC slurry.

Consequently, we pursued another advanced sawing technique using structured wires in combination with SiC slurry. A structured wire is first manufactured as a straight wire, and then waves are created in one or two dimensions. The wavelength is on the order of millimeters [9]. Wafer surfaces cut by structured wires show characteristics of both diamond-wire- and slurry-sawn surfaces. The surfaces of structured-wire-sawn wafers suggest that a hybrid brittle-ductile material removal process is active. SiC particle indentations are visible without the typical wedge shape of standard slurry-sawn wafers. Wire sawing with a structured wire in combination with a SiC slurry did not show the disadvantage of reduced fracture strength, which is critical for thin wafers in particular and which was observed for diamond-wire sawing. Furthermore, the TTV values are reduced by about 50% when using a structured wire instead of a straight wire, as shown in Fig. 3, independent of the feed rate and wire velocity.

90-μm- and 120-μm-thick wafers were mechanically characterized by bending tests. Thin wafers are increasingly flexible which has the effect that, with a standard test setup, the classical linear elastic fracture mechanics theory cannot be applied. Consequently, we developed a ring-on-ring (ROR) bending test for round samples 22 mm in diameter that were cut by a laser out of the silicon wafers. Due to the reduced sample size, the maximum displacement before fracture was reduced, and induced crack lengths could be estimated. In Fig. 4a Weibull diagram for 90 and 120 μm thick wafers is shown.

The wafers were tested using the 2 mm round samples with the adapted ring on ring setup. The results shown are for the assumption that the classical linear elastic fracture mechanics theory is valid. This may not be the case due to the flexability of the wafers. However, the results can be used

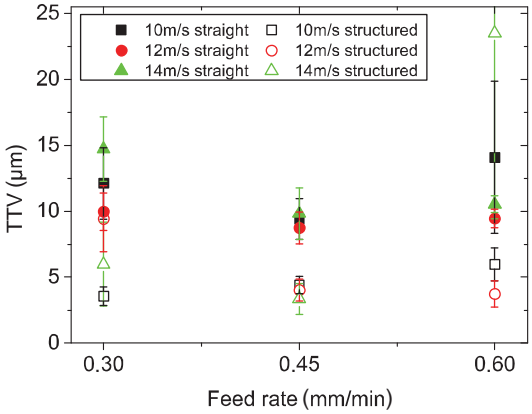


**Figure 3** TTV measurements of 180-µm-thick wafers sawn with a straight (closed symbols) or structured (open symbols) wire with various feed rates and wire velocities.

to gain a relative comparison of the mechanical behavior of thin wafers.

**3.2 Handling** To adapt handlers to wafers that are ≤100 µm thick and evaluate their performance, a demonstration unit was developed. This tool is able to carry out separation of silicon wafers or solar cells, placement on a belt, and transfer between carriers. Bernoulli-based handlers were identified as being the most suitable for thin wafers due to the low mechanical stress imposed on the wafer during handling, compared to a vacuum gripper.

The Mechatronics GmbH demo wafer handling system is able to handle a wide range of wafer types at varying production levels with high speed and low breakage rate. Special Bernoulli nozzles are arranged on the end effector so that a stable air cushion approximately 230 µm in height between the wafer and the end effector is generated. This results in contactless handling and, after optimization, no breakage caused by handling occurred for wafers 100–200 µm thick. The handling unit reached a throughput of 1560 wafers/h.

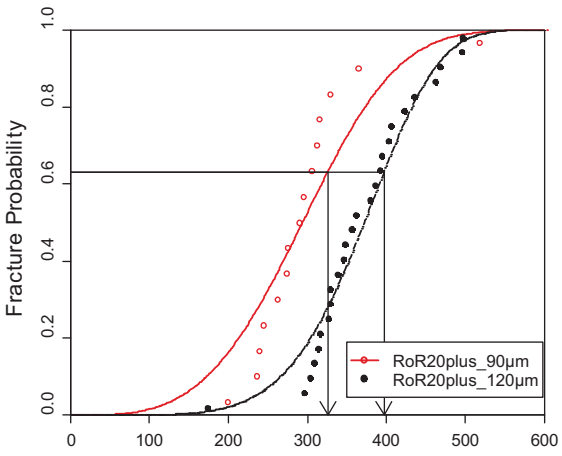


**Figure 4** Weibull diagram for 90- and 120-µm-thick wafers tested with a ring-on-ring setup.

The handling system was tested at Hanwha Q CELLS in the pilot production line, and demonstrated <5% breakage rate for thin wafers processed along the full cell route. We used diamond-wire-sawn silicon wafers in these tests. The metallization process generates more mechanical stress and bowing in the wafers than any other step. Therefore, the busbars were printed perpendicular to the sawing grooves, taking advantage of the higher stability of diamond-wire-sawn wafers in this direction. Finished solar cells 100 µm thick show a 3 mm bow in both directions (across the busbars and across the sawing grooves). During transfer of the wafers from a carrier to the belt the bowed wafers stuck together. To avoid this, the carrier height had to be corrected. With process and handling adjustments, a breakage rate of 4.5% was achieved, as measured by multiple handling of forty 100-µm-thick cells fabricated with a modified NHT process.

### 3.3 Surface passivation

**3.3.1 PHT route** The PHT solar cells employ a diffused phosphorus emitter on the front surface; the rear surface of the wafer is usually not diffused. Therefore, for PHT solar cells, we need a passivation layer for a heavily doped n-type front surface and a passivation layer for a lightly doped p-type rear surface.

A $SiN_x$:H layer can efficiently passivate heavily doped n-type silicon surfaces, as in standard industrial solar cells. The PHT emitter is diffused from a $POCl_3$ source and has a sheet resistivity of 100 Ω/sq. After $SiN_x$:H deposition and firing at 880 °C, this emitter exhibits an emitter saturation current density of $J_{0e} = 120$ fA/cm$^2$.

The front $SiN_x$:H layer is not only a passivation layer; it also functions as an anti-reflection coating. The optimal anti-reflection coating has a refractive index of $n \approx 2$ and low absorption from UV to IR wavelengths. Unfortunately, the passivation is best for absorbing $SiN_x$:H layers containing a high ratio of a-Si:H in the layer. Therefore a compromise has to be found between low absorption, a refractive index of $n \approx 2$, and good passivation. An alternative that sidesteps this compromise is a thermal $SiO_2$ layer 5–10 nm thick that passivates the surface, followed by a low-absorption-$SiN_x$:H layer. This layer is applied for the PHT solar cells in Section 3.6.

Very low surface recombination velocities are achieved on lightly doped p-type silicon surfaces using $Al_2O_3/SiN_x$:H stacks optimized for two types of deposition environment: a laboratory where the $Al_2O_3$ is deposited by atomic layer deposition (ALD) and the $SiN_x$:H is deposited by PECVD; and an industrial pilot line where both layers are deposited by PECVD. In order to withstand the metallization and post-metallization processes, the passivation layers need to be resistant to contact firing in a belt furnace.

For the laboratory passivation process, excellent surface recombination velocities of 6 cm/s were achieved on p-type silicon wafers. The firing process took place at 800 °C in a commercially available firing furnace. For the pilot line

passivation process, very good surface passivation was also reached with a lifetime peak of about 1 ms for a firing temperature of 870 °C. The lifetime measurements were performed over a width of 70 cm using a 90-cm-wide deposition carrier for three different deposition runs over several days. The process is therefore considered to be reproducible.

**3.3.2 NHT route** The $NHT_{front}$ solar cells use a diffused boron emitter on the front surface and a diffused phosphorus BSF on the rear surface. The $NHT_{rear}$ solar cells have a boron emitter on the rear surface and a diffused phosphorus front-surface field on the front surface. Therefore, for the passivation of NHT solar cells, we need passivation layers for heavily doped p- and n-type surfaces.

The passivation quality of $Al_2O_3$ layers was studied on heavily boron-doped silicon surfaces. For this study, a boron emitter of 90 Ω/sq was passivated by PECVD or ALD $Al_2O_3$ layers. In both cases, a low $J_{0e}$ of 36 fA/cm$^2$ was achieved [10]. It is calculated [11, 12] that this value corresponds to a surface recombination velocity of about $(340 \pm 20)$ cm s$^{-1}$ for a surface doping concentration of $7 \times 10^{19}$ cm$^{-3}$, which is more than one order of magnitude lower than for $SiO_2$ passivation layers [13].

**3.3.3 NLT route** The typical NLT solar cell features intrinsic and doped a-Si:H layers deposited on both sides of the absorber, an n-type silicon wafer that is chemically thinned down to the desired thickness. These layers are deposited by PECVD, usually using silane ($SiH_4$), hydrogen ($H_2$), trimethylboron ($B(CH_3)_3$ or TMB) and phosphine ($PH_3$) as precursor gases. The key point of this type of device is the excellent passivation of the wafer surfaces obtained with the very thin (<10 nm thick) intrinsic a-Si:H layers. The emitter and BSF are formed by the p- and n-type a-Si:H layers, respectively. As the intrinsic and doped layers are usually deposited sequentially without breaking vacuum, and the doped layers can influence surface recombination, surface passivation and junction formation are intertwined. In addition, the a-Si:H layers are known to cause significant parasitic absorption [14], so that surface passivation and light management are also interdependent: the best layers passivate the surface but are as thin as possible.

We recently reported high-quality passivation layers that give high carrier lifetimes in the as-deposited state and with minimal thicknesses [15, 16]. With the aid of *in situ* plasma diagnostics used during the PECVD process, we demonstrated that good a-Si:H passivation layers are obtained in regimes close to the amorphous-to-microcrystalline transition [15]. To approach this transition without risking epitaxial growth (which is detrimental to passivation), $H_2$ plasma treatments are used during a-Si:H deposition and are observed to improve the passivation level [16]. Finally, well-controlled wafer texturing and surface cleaning processes are extremely important in enabling a-Si:H passivation.

In this project, the thicknesses of the front passivation and emitter layers were further reduced, resulting in increased transparency without significant loss in minority carrier lifetime. Applying these layers to (float zone) silicon wafers of decreasing thickness, minority carrier lifetimes of 7.7, 4.3, and 3.2 ms were measured at $10^{15}$ cm$^{-3}$ for 230-, 160- and 96-μm-thick wafers, respectively. These led to impressive implied open-circuit voltage ($V_{OC}$) values of 736, 741, and 752 mV, respectively. Note that the injection level corresponding to one-sun illumination increases with decreasing wafer thickness (similar to a concentration effect), leading to increased implied $V_{OC}$. The final $V_{OC}$ of the NLT cell fabricated on the 96-μm-thick wafer was 735 mV. The front intrinsic/p-type stack in this cell was only 17 nm thick measured on flat glass, i.e., 10 nm perpendicular to the pyramid facets of the textured surface.

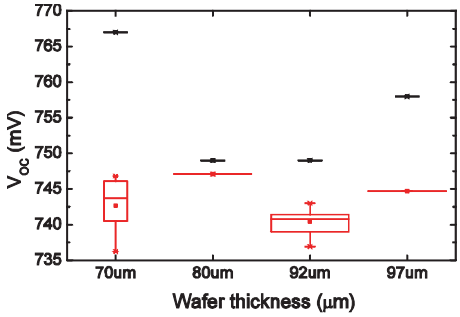


**Figure 5** $V_{OC}$ (red data) and implied $V_{OC}$ (black data) of NLT devices on wafers of different thicknesses. The layers were not co-deposited on the wafers. The 70- and 92-μm-thick wafers had nine 2 cm × 2 cm cells per wafer, and the error bars represent the deviation in these cells (i.e., they indicate spatial homogeneity).

Further work led to an implied $V_{OC}$ as high as 767 mV on a 70-μm-thick wafer (Fig. 5, black data). The $V_{OC}$ of finished devices on wafers 70–100 μm thick range from 737 to 747 mV (Fig. 5, red data). Note that the expected trend of increasing $V_{OC}$ with decreasing thickness – which we observed in the implied $V_{OC}$ measurements of co-deposited cell precursors mentioned in the previous paragraph – is not observable in Fig. 5. Figure 5 is a compilation of results recorded across the project (no co-deposition) and only one wafer was used for each thickness, though there were several cells per wafer in two cases. Consequently, the data do not minimize or exclude process and materials variation over time; they simply indicate that excellent $V_{OC}$s are possible on thin wafers.

**3.4 Light management** The thinner the silicon wafer, the larger the loss in short-circuit current density $J_{SC}$. To mitigate this loss, the aim is to enhance the pathlength of the light within the wafer through appropriate surface structuring. However, light with a long pathlength encounters the front and back surfaces many times and, as there are layers at these surfaces that may absorb, parasitic absorption may also be an issue.

Through a careful analysis of the IR optical losses in high-efficiency silicon solar cells, it is apparent that – unless the Yablonovitch limit can be exceeded [17] – the dominant

source of the losses is parasitic absorption [18]. This occurs because scattering from the random-pyramid texture is very near Lambertian after the first passes through the wafer. More specifically, for a 96-μm-thick NLT cell, we calculated that only a modest 0.6 mA/cm$^2$ can be gained by changing from a random pyramid structure to a Lambertian texture, after elimination of all parasitic absorption [19]. Thus we focus primarily on internal reflectance (i.e., parasitic absorption) of the solar cells in this work.

**3.4.1 Light management for the PHT route** The rear internal reflectance was studied for two PHT solar cells with wafer thicknesses of 100 and 250 μm. The rear of both wafers was identically polished and the same rear passivation stack was deposited (PECVD $Al_2O_3$, 10 nm, and PECVD $SiN_x$:H, 100 nm). Finally, a full-area aluminum back surface reflector and laser-fired contacts [20] covering less than 1% of the rear surface were applied to both wafers. The long-wavelength total reflectance is shown in (Fig. 6). The ideal reflectance spectrum would be zero at wavelengths less than 1200 nm (absorption of all super-bandgap light), with a sharp transition to 100% reflectance above 1200 nm (no parasitic absorption of sub-bandgap light).

The reflectance spectra are fitted using PC1D [21]. The best parameter for the rear internal reflectance on the first bounce is 90%, and for subsequent bounces is 95%. In order to understand the impact on $j_{sc}$ of these deviations from ideality, simulations are carried out in which the first-bounce rear internal reflectance is varied for different wafer thicknesses.

The thinner the wafer, the larger the gain in $J_{SC}$ per gain in internal reflectance. The potential increase in $J_{SC}$ for perfect first-bounce rear internal reflection is only 0.35, 0.26, 0.22, and 0.18 mA cm$^{-2}$ for wafer thicknesses of 50, 100, 150, and 250 μm, respectively. This rear layer stack is therefore not only an excellent passivation solution, it is also very close to ideal in terms of IR light management.

**3.4.2 Light management for the NLT route** We analyzed a 96-μm-thick NLT cell with an active-area short-circuit current density of $J_{SC,active} = 40.3$ mA/cm$^2$ by measuring the external quantum efficiency and reflectance spectra of this cell (Fig. 7). This cell was fabricated using a hydrogenated indium oxide/indium tin oxide (IO:H/ITO) bilayer at the front [22], and a very transparent ITO layer (featuring a low carrier density) at the rear. Consequently, the internal reflectance of this cell is already excellent and there is only a little remaining IR parasitic absorption at wavelengths >1000 nm (0.4 mA/cm$^2$).

To try to squeeze out this remainder, we introduced an improved rear reflector with an ultrathin ITO layer and a low-refractive-index magnesium fluoride ($MgF_2$) layer in place of the previous, transparent ITO layer. With this design, local contacts through the $MgF_2$ layer are required to make electrical contact between the ultrathin ITO and the silver or aluminum rear contact. A magnesium fluoride/silver ($MgF_2$/Ag) reflector yields an average rear internal reflectance of greater than 99.5% and an IR internal quantum efficiency that exceeds that of the world-record UNSW PERL cell [18].

In addition, a $MgF_2$/Al reflector performs nearly as well, enabling an efficiency of 21.3% and a $J_{SC}$ of nearly 38 mA/cm$^2$ in an NLT solar cell without silver or ITO at the rear. Besides IR parasitic absorption, and unique to the NLT cell design, there is appreciable UV and blue parasitic absorption in the front a-Si:H layers at wavelengths <700 nm [14]. While this loss does not vary with wafer thickness, it is the most important $J_{SC}$ loss in these cells and its *relative* importance increases for thinner wafers. If we were to eliminate short-wavelength parasitic absorption without making any changes to the internal reflectance, $J_{SC,active}$ of the aforementioned cell would increase by 1.6 mA/cm$^2$. Thus, there is the potential to achieve nearly 42 mA/cm$^2$ with a 96-μm-thick NLT cell with random pyramids and optimized TCO layers. Even slightly higher $J_{SC}$ should be possible for PHT and NHT cells, since these have little front parasitic absorption and a dielectric rear passivation layer is optically equivalent to a non-absorbing TCO.

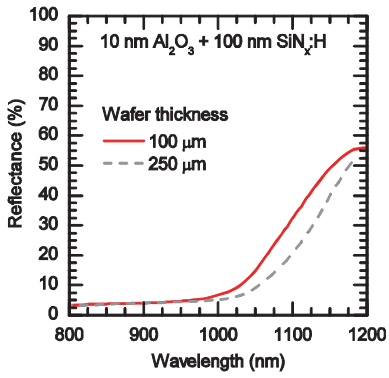


**Figure 6** Long-wavelength reflectance of two PHT solar cells with different wafer thicknesses and with the same rear passivation stack and reflector.

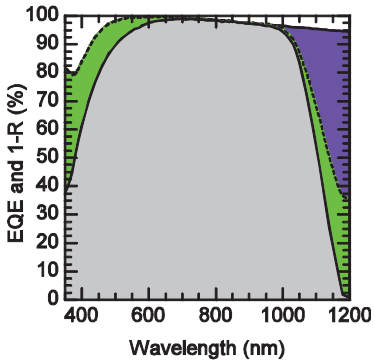


**Figure 7** External quantum efficiency (solid line) and total absorbance (1-reflectance, dashed line) of an NLT solar cell on a 96-μm-thick wafer. The gray area corresponds to collected carriers, the green areas correspond to parasitic absorption, the white areas correspond to front-surface reflectance, and the blue area corresponds to escape reflectance.

In fact, we calculated that the pathlength of IR light could be *reduced* (e.g., by worse internal reflection) to only 15 times the wafer thickness and we would still reach 41 mA/cm$^2$ if there were no front parasitic absorption. Note that the gains from eliminating short- and long-wavelength parasitic absorption are independent; thus, it is insufficient to make the internal reflectance of IR light perfect if the front a-Si:H layers remain the same. In this case, $J_{SC,active} = 40.7$ mA/cm$^2$.

Given the above analysis and the improvements that we have made in IR internal reflectance, our efforts are now better focused on reducing UV and visible parasitic absorption. To this end, we also investigated amorphous silicon carbide (a-SiC$_x$) as an alternative to pure a-Si:H for the front doped layer. Others have previously investigated a-SiC$_x$ for heterojunctions, including for both intrinsic and doped layer replacements [23, 24]. The advantage of this material is the adjustability of its bandgap and refractive index by changing the carbon content of the a-SiC$_x$ layer. By increasing the methane content during deposition, the optical bandgap increases and thus parasitic absorption in this layer decreases. From measured optical data, we found that $J_{SC,active}$ can be changed by more than 1 mA/cm$^2$ over the range of achievable carbon contents. By assuming no changes in $V_{OC}$ and fill factor (FF), this would increase the efficiency of NLT cells by approximately 0.5% absolute.

To evaluate the influence of the carbon content on the electrical properties, *Suns*$V_{OC}$ [25] and quasi-steady-state photoconductance (QSSPC) measurements were performed on solar cell precursors, yielding the pseudo or external voltage ($V_{OC,ext}$) and the implied or internal voltage ($V_{OC,imp}$), respectively (Fig. 8). In this experiment, the diborane ($B_2H_6$) doping concentration was varied in addition to the methane concentration. A large methane concentration dramatically reduces the external voltage. This can be explained by the reduced doping efficiency of layers with a high carbon content, which leads to a higher activation energy and thus a lower selectivity of the heterojunction. In comparison to pure a-Si:H (zero carbon content), it can be seen that a small amount of carbon reduces the impact of the doping concentration. Thus a small amount of carbon can be used to widen the bandgap and reduce the necessity of a high doping concentration, enabling high $V_{OC}$ and $J_{SC}$ simultaneously.

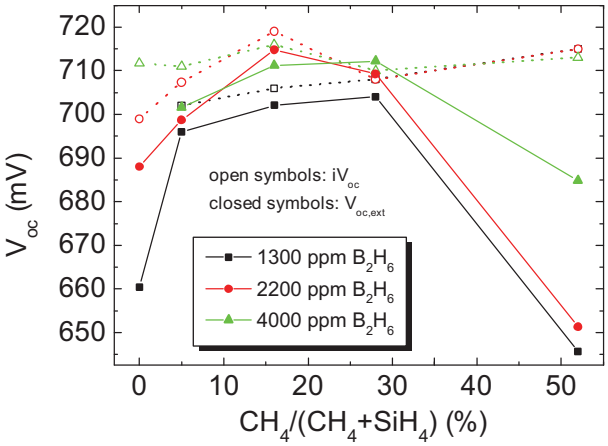


**Figure 8** Measured internal ($V_{OC,imp}$, QSSPC) and external ($V_{OC,ext}$, *Suns*$V_{OC}$) voltages of NLT solar cell precursors for different doping concentrations as a function of methane content during the front doped layer deposition.

**3.5 Metallization** In industry, screen-printed contacts are applied on the front and rear. While it is possible to adapt the printing parameters in such a way that breakage is low, the bow induced by a full-area aluminum BSF cannot be avoided and is determined to be as high as 4 mm on a 125 × 125 mm$^2$ cell. Therefore, at least for the rear contact of PHT cells, an alternative rear side concept has to be found. This concept is dielectric passivation in combination with a full-area screen-printed aluminum layer but only local contacts to the silicon wafer. These contacts to the silicon can be formed either by laser firing or by laser contact opening and subsequent aluminum alloying.

Another approach that still uses screen printing but avoids the bow is the formation of metal grids on both the front and the rear. This also allows for bifacial applications.

**3.5.1 Nickel-plated front contacts for front versus rear emitter cell concept** A major challenge for integrating nickel (Ni) seed layers into the fabrication of conventional p-type silicon solar cells is to prevent nickel contamination of the space charge region of the phosphorus-diffused $n^+$ emitter on the front. This contamination can occur during the thermal formation of the nickel silicide layer ($NiSi_x$), which is necessary for improved contact adhesion.

We have investigated the application of nickel-plated front contacts to front- and rear-emitter silicon solar cells [24]. We compare identically processed PHT and $NHT_{rear}$ silicon solar cells featuring (i) a homogeneous phosphorus-diffused $n^+$ front, acting as emitter or front-surface field, and (ii) a full-area aluminum-alloyed $p^+$ rear, acting as BSF or rear emitter. This results in an $n^+pp^+$ front-emitter cell structure and an $n^+np^+$ rear-emitter structure, respectively.

We have shown that the contact annealing temperature for the thermal formation of $NiSi_x$after the electroless nickel plating has a significant influence on the $NiSi_x$ layer thickness [26]. Increasing the temperature from 300 to 450 °C induces deep $NiSi_x$ spikes. The intensified penetration of the $n^+$ front by these $NiSi_x$ spikes leads to a strong degradation of the front-emitter p-type silicon solar cell performance due to decreased shunt resistance and contamination of the emitter space charge region. In contrast, the rear-emitter n-type silicon solar cells are predictably more stable. Therefore, by using n- instead of p-type silicon as the base material, improved stability against the nickel contact annealing can be easily realized without significant changes in the solar cell fabrication process.

**3.5.2 Metallization for the NLT route** Metallization of NLT solar cells differs significantly from that of diffused-emitter approaches since thin a-Si:H layers do not withstand post-processing temperatures much above 200 °C. Consequently, low-temperature silver screen-printing pastes are used for industrial cells, and nickel/copper (Ni/Cu) electroplating was investigated as an advanced alternative. Electroplating has the potential to increase efficiency by reducing shadowing and finger resistance, lower costs, and increase flexibility for the annealing process that is normally used to cure silver paste. Ultra-narrow fingers (~10 μm wide) were achieved by using Ni/Cu electroplating in a lithographically defined cavity. Figure 9 shows a focused-ion-beam cross-section of an electroplated Ni/Cu finger.

Due to the reduced shadow losses at the front-side, $J_{sc}$ improves by more than 1 mA/cm$^2$ compared to screen-printing, which increases the cell efficiency by 0.4% absolute.

### 3.6 Solar cell results

**3.6.1 NLT route** To fabricate complete NLT solar cells on wafers less than 100 μm thick, n-type CZ-Si wafers were used for the absorber. By using a saw-damage-removal step to reach the desired cell thickness followed by surface texturing, wafer thicknesses ranging from 56 to 96 μm were obtained. Intrinsic a-Si:H layers were deposited at temperatures below 250 °C on both sides of the wafers using PECVD in a reactor operated at very high frequency (VHF, 40.68 MHz). These layers were optimized as discussed in Section 3.3 to yield minority-carrier effective lifetimes as large as 11 ms on thick wafers. p- and n-type a-Si:H layers were deposited on the front and back of the cell, respectively, to form the emitter and BSF. The p-type layer thickness was kept below 5 nm to minimize blue and UV parasitic absorption, while the n-type layers were somewhat thicker. IO:H/ITO bilayers – high-mobility, low contact resistance TCO layers – were sputtered on the front side and a two-layer ITO stack was deposited at the rear of the wafer. The cells were finished with a sputtered silver reflector and a screen-printed silver front electrode grid.

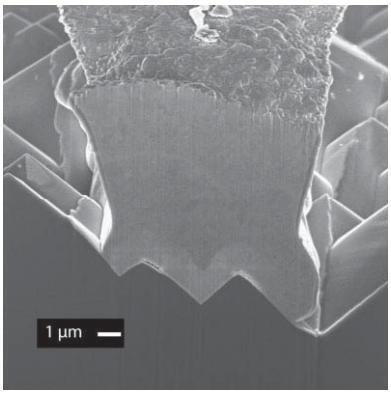


**Figure 9** Focused-ion-beam cross-section of an electroplated Ni/Cu finger on a NLT solar cell.

The performance of the best 100 cm$^2$ NLT devices is presented in Table 1. Using CZ-Si wafers, higher $V_{OC}$ values were measured than on thicker CZ-Si or FZ-Si wafers, which is a testament to the excellent surface passivation. A champion cell on an 80-μm-thick wafer reached an efficiency of 21.1%, and comparable performance was obtained on a 92-μm-thick wafer, with the expected slight increase in $J_{SC}$ and decrease in $V_{oc}$. These relatively large-area cells exceed the 20% efficiency goal of the 20 plμs project by 1% absolute, while using thinner wafers than the target 100 μm.

**3.6.2 PHT route** First, an adapted baseline process for PHT solar cells was developed on 100-μm-thick Cz–Si wafers. The silicon wafers (p-type, 2–3 Ωcm) were thinned down to the desired thickness and cut to a wafer size of 125 × 125 mm$^2$. The cells have a selective emitter on the textured front side, which is passivated with a thermal $SiO_2$ layer and covered by a $SiN_x$:H layer. The $SiN_x$:H layer acts as an anti-reflection coating. The rear is passivated by an Al BSF. The contacts on the front and rear side were formed by screen-printing.

Next, a PHT solar cell process based on dielectric passivation (a $Al_2O_3/SiN_x$:H stack) of the rear was developed, resulting in the solar cell structure shown in Fig. 10. A homogeneous phosphorous-diffused $n^+$ emitter was applied. The front contacts were formed by a two-layer

**Table 1** Solar cell characteristics of select 100 cm$^2$ NLT solar cells.

| cell | $V_{OC}$ [mV] | $J_{SC}$ [mA/cm$^2$] | FF [%] | efficiency [%] |
|---|---|---|---|---|
| Cz-Si, 92 μm, 100 cm$^2$ | 738 | 37.1 | 76.6 | 21.0 |
| Cz-Si, 80 μm, 100 cm$^2$ | 747 | 36.8 | 76.8 | 21.1 |

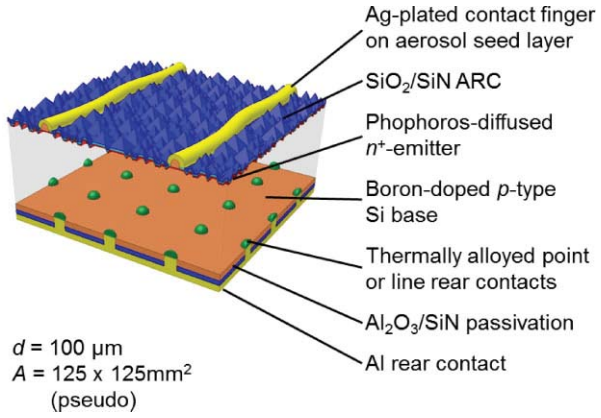


**Figure 10** Schematic of an optimized PERC p-type silicon solar cell from the PHT route featuring a homogeneous phosphorous-diffused $n^+$ emitter on the front and local Al-$p^+$ contacts through the passivated rear.

metallization technique, consisting of an aerosol-printed seed thickened by light-induced silver plating. This approach allows one to optimize contact resistance and line resistance separately.

For the optimized PHT solar cell, of locally defined rear contacts through the $Al_2O_3/SiN_x$:H passivation stack are required. Firing of full-area screen-printed Al paste onto the locally opened passivation layer results in drastically increased point-contact depths, leading to enlarged contact areas with only shallow Al-$p^+$ regions (acting as local back surface fields, LBSFs).

By modifying the composition of the Al paste and adding silicon powder, the local alloying process can be improved, i.e. the depth of the contact decreases while the Al-$p^+$ thickness increases [27, 28].

After optimising the front emitter and rear local contacts, we obtained an efficiency of 19.9% for our best thin PHT solar cell, fabricated on 0.5 Ωcm boron-doped p-type silicon (see Table 2). The area-averaged thickness of this cell is 103 μm, as determined via weight measurement. Note that this cell was realised without any alignment steps during fabrication. Compared to the adapted PHT baseline process, the optimized process shows a higher $J_{SC}$ and $V_{OC}$. As discussed in Section 3.4, the better rear internal reflection from the dielectric layer of the optimized PHT cell is at least partly responsible for the $J_{SC}$ increase. The lower rear surface recombination velocity of the dielectric passivation helps to improve $V_{OC}$.

**3.6.3 NHT route** Three NHT solar cell variations were explored: a homogenous emitter and BSF, a selective emitter and homogeneous BSF, and a selective BSF and homogeneous emitter. In all cases, both the front and rear were dielectrically passivated and, as dielectrically passivated boron-emitter solar cells can be contacted by metal finger grids on both sides, all cells were bifacial.

For the NHT bifacial solar cell concept, it is important to implement an excellent passivation of the heavily phosphorous-doped layer. To that end, we replaced our initial single-layer $SiN_x$:H passivation scheme with a passivation stack of thermal $SiO_2$ and $SiN_x$:H, leading to lower $J_{0BSF}$ values. However, the additional high-temperature step combined with the $SiO_2$ grown on the boron emitter surface leads to a significant depletion of boron towards the surface, which causes higher contact resistivities.

**Table 2** Solar cell characteristics of the best 103-μm-thick optimized PERC p-type solar cell from the PHT route, confirmed at Fraunhofer ISE CalLab (total cell area of 148.2 $cm^2$), and a 100-μm-thick PHT solar cell from the adapted baseline process (cell size of $125 \times 125\,cm^2$).

| cell | $V_{OC}$ [mV] | $J_{SC}$ [mA/$cm^2$] | FF [%] | Eff. [%] |
|---|---|---|---|---|
| PHT: optimized | 672 | 38.5 | 76.8 | 19.9 |
| PHT: adapted baseline | 645 | 36.6 | 79.3 | 18.7 |

In order to minimize electrical losses in the boron front emitter and the phosphorous BSF, selective doping structures were introduced into the NHT bifacial solar cells. Both selective, heavily doped layers were created by means of wet-chemical etch-back solutions. The selective phosphorous BSF is created via an etch-back process which has been presented in [29], whereas the boron emitter etch-back has been introduced in [30]. These selective doping structures avoid the trade-off between high surface doping concentration to achieve low contact resistance and high emitter sheet resistance to minimize $J_{0e}$.

Table 3 gives an overview of the performance of the best 100-μm-thick NHT bifacial NHT solar cells with an additional thermal oxidation.

Due to the "kink and tail" shape of a $POCl_3$ diffused profile, the $V_{OC}$ gain by a selective $n^+$ BSF is very high (17 mV). By employing the selectively etched-back boron front emitter, a $V_{oc}$ gain of 5 mV is achieved and $J_{SC}$ is maintained. $J_{SC}$ can be further enhanced by reducing the finger width (from 110 μm to 70 μm: $\Delta J_{sc} \approx 1.1\,mA/cm^2$). Because of decreased FF compared to the homogeneously doped solar cell, the selective $p^+$ emitter solar cell does not exploit its full potential. This is most likely caused by unoptimized co-firing conditions, as the depth and surface doping concentration of the selective emitter beneath the contacts are higher than in the homogeneous case and should therefore yield an even higher FF.

All solar cell types exhibit very high bifaciality, defined as $\eta_{RS}/\eta_{FS}$, efficiency illuminating from the rear and the front respectively, which is further increased up to >99% by a selective $p^+$ or $n^+$ layer under the metal contacts for the emitter and BSF respectively. The high bifaciality shows that with a suitable solar cell process the position of the emitter, front or back, can be freely chosen. Optimized solar cells featuring selective structures on both sides are expected to significantly exceed the conversion efficiency of 19.5% on 100 μm thick n-type solar cells that we have achieved so far.

**3.7 Solar cells from the pilot production line** The optimized PHT process that includes rear passivation and laser-fired contacts was determined to be the easiest to realize in an existing pilot production line within the duration of the European project 20 pl μs. An NHT process was

**Table 3** Solar cell characteristics of bifacial solar cells (5-inch n-type Cz-Si wafers, thickness ≈100 μm, $\rho_{base} = 2.0$–$4.5$ Ωcm, $\tau_{base} \approx 7$ ms) measured using a black chuck.

| cell | $V_{OC}$ [mV] | $J_{SC}$ [mA/$cm^2$] | FF [%] | efficiency [%] | bifaciality [%] |
|---|---|---|---|---|---|
| hom. emitter, hom. BSF | 644 | 37.1 | 78.3 | 18.7 | 94.3 |
| sel. $p^+$ emitter, hom. BSF | 649 | 37.0 | 77.3 | 18.5 | 95.9 |
| hom. emitter sel. $n^+$ BSF | 661 | 37.6 | 78.4 | 19.5 | 99.4 |

chosen as a backup and was also pursued on the pilot line. We believe that NHT cells have higher efficiency potential than PHT cells (though we were unable to demonstrate this in Section 3.6) but more complex process development is required. The NLT process has the highest efficiency potential, but is the least widespread technology; the equipment is currently not available at Hanwha Q CELLS and most manufacturers. Therefore, the development timeline in an industrial-type setting was too long for an NLT process given the scope of the "20 pl μs" project.

Because of successful and fast developments on the backup NHT route, we chose to transition this route to our primary approach. Furthermore, we did not implement a bifacial configuration, but instead used a rear-emitter configuration that more easily lends itself to mass production [31], see Fig. 1. With this modified NHT route, a complete n-type silicon ingot can be used, as fabrication results show, provided that the ingot has resistivity >5 Ωcm. While from 2 to 5 Ωcm, the passivation quality of the front $n^+$-n junction still improves with increasing bulk resistivity [32], and therefore $J_{SC}$ and the efficiency increase strongly.

In previous work, we demonstrated that rear-emitter NHT cells with efficiencies of up to 21.3% (5.2 W) are possible on 6-inch,standard thickness (160 μm) wafers after further improvement of passivation and metallization [33]. As this project was concerned with thin wafers, we first estimated the influence of wafer thickness by PC1D [34, 35]. The simulations indicated that rear-emitter NHT cells are suitable for 100–200 μm thick wafers to achieve an efficiency of above 20%. This means that it is possible to adapt to the changing wafer market with this process, and to reduce silicon consumption without compromising performance [36].

We next fabricated 100-μm-thick rear-emitter NHT cells on the pilot production line. Thinner cells show a $J_{SC}$ loss, which is consistent with the EQE loss at long wavelengths in Fig. 11. The 100-μm-thick cells fabricated in the pilot line of Hanwha Q CELLS had a median efficiency of 20.0% (median $V_{OC} = 659$ mV, median $J_{SC} = 38.5$ mA/cm$^2$, median FF = 78.7%). The best cell had an efficiency of 20.3% with $V_{OC}$ of 662 mV, $J_{SC}$ of 38.5 mA/cm$^2$ and FF of 79.6% [36].

**3.8 Cost and life-cycle analysis** As the goal of this project was a path to *manufacturing* of thin silicon solar cells, we performed a cost and life-cycle analysis (LCA) for each fabrication route. The cost analysis was based on available data and should be further refined when more reliable data are available for the new processes of the PHT, NHT and NLT routes. We assumed a pilot production facility located in Europe with a yearly production capacity of ∼60 $MW_P$. The calculated costs of ownership (CoO) of 20 plμs cells are 0.29 €/$W_P$, 0.30 €/$W_P$, 0.34 €/$W_P$ for the PHT, NHT and NLT processes, respectively, as listed in Table 4.

Note that PHT turns out to be the most cost-effective cell process for implementation into pilot line production. The cost analysis indicates that this is largely because the CoO is sensitive to the cost of materials and consumables. A particularly important cost is that of the metallization, as the electrodes require the use of precious metals.

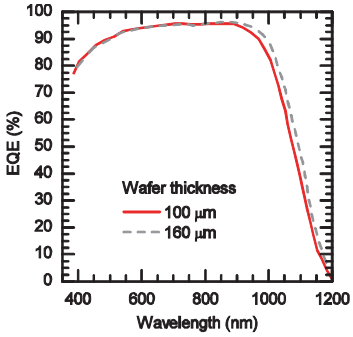


**Figure 11** EQE of rear-emitter NHT cells on 100- and 160-μm-thick wafers fabricated on a pilot production line. The thin cells exhibit a loss for long wavelengths compared to the thick cells, as expected.

We next stepped ahead from the pilot production scale to a mass production scenario for PHT cells. Given the fact that not all parts of the equipment needed for PHT cells which are presently available on the market have been used in mass production for a long time, a precise calculation of manufacturing costs is not straightforward and can be estimated only by assuming economies of scale. We simulated costs for a ∼1 $GW_P$ PHT cell fab located in Asia. Therein, the cost of thin wafers was assumed to be 0.63 €/wafer. The total cost – that is, the cost for the supply of wafers and manufacturing of PHT cells – was

**Table 4** The fabrication processes assumed for the CoO and LCA calculations.

| PHT | NHT | NLT |
|---|---|---|
| alkaline texturing | alkaline texturing | alkaline texturing |
| $POCl_3$ diffusion | $BBr_3$ diffusion | cleaning |
| emitter removal | BSG removal | PECVD FS & RS (i) a-Si:H |
| PSG removal | thermal $SiO_2$ | PECVD FS (p) a-Si:H |
| cleaning | PECVD FS $SiN_x$ | PECVD RS (n) a-Si:H |
| PECVD RS $Al_2O_3/SiN_x$ | emitter removal | sputter FS & RS ITO |
| PECVD FS $SiN_x$ | $POCl_3$ diffusion | screen-print FS Ag |
| screen-print FS Ag; RS Al | PSG removal | annealing |
| firing | PECVD RS $SiN_x$ | |
| LFC | laser ablation | |
| LIP | screen-print FS Ag/Al | |
| | firing | |
| | PVD RS Al | |
| | annealing | |

calculated to be 0.25 €/$W_P$. Further cost reduction can be achieved with an optimization of the PHT process – for example, lowering breakage rates (yield losses). With a decrease in yield losses from 7% to 2%, the total production costs could diminish from 0.25 €/$W_P$ down to 0.24 €/$W_P$. Compared to a reference industrial technology (a typical aluminum BSF cell fab with a production site in Asia and 1 $GW_P$ yearly throughput), PHT production may result in a savings of up to 28%.

An environmental sustainability evaluation was carried out by performing an LCA consisting of three stages of increasing refinement. The first and second LCA runs focused on the solar cell manufacturing process. In the second run of the simulation, critical process steps were identified for each route and compared to those in the other routes (see Table 4). We found in particular that the cleaning of exhaust gases and metallization steps transversely affect all environmental impact categories. In the third and final step, we introduced thin wafers into the cell manufacturing model and observed that the environmental performance of all cell types improved significantly. The environmental impacts were compared with the reference industrial process (again, aluminum BSF cells) and, category by category, lower impacts were observed for the 20 pl$\mu$s cell technologies (with the exception of the photochemical oxidation category).

The assembly of cells into modules and the installation of module arrays were also considered in the third LCA run. Here, we assumed a 3 $kW_P$ rooftop-mounted array in southern Europe. The energy payback time (EPBT) and carbon footprint, which are typical environmental performance indicators of photovoltaic systems, were calculated and compared with the reference process; both indicators are significant lower for the 20 pl$\mu$s cell technologies, especially

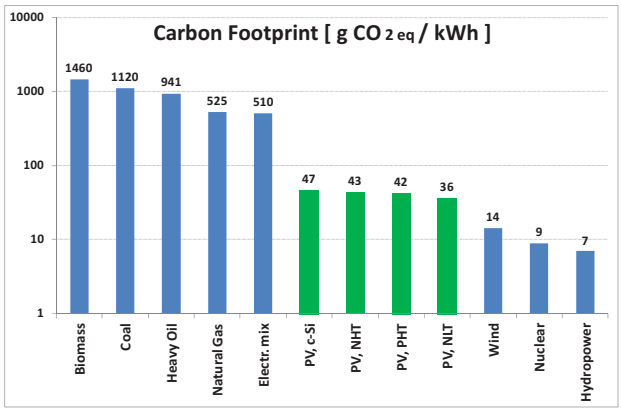


**Figure 12** Calculation of carbon footprint for the major conventional (coal, oil, natural gas, nuclear) and renewable (biomass, PV, wind, hydropower) electricity sources available. The carbon footprint of the EU-27 electricity grid mix is included for comparison. French technology was assumed for nuclear energy; all other energy sources assume Italian production technology.

NLT [37]. The EPBT of the reference system is 1.96 years, whereas it decreased by 27.2%, 26.6%, and 29.7% for PHT, NHT and NLT systems, respectively. Figure 12 shows the results of the carbon footprint calculations, and compares the photovoltaic technologies to all other major sources of electricity, including conventional technologies, other renewable sources, and the EU-27 electricity grid mix.

**4 Conclusion** This project demonstrated that 100-$\mu$m-thick silicon solar cells with efficiencies of 20% are industrially feasible in a pilot production line. To achieve this, we developed solar cell processes for three different fabrication routes: PHT, NHT, and NLT, and each demonstrated an efficiency near or above 20%. Although the routes result in very different device structures, five elements are fundamental to *all* thin silicon solar cells – wafering, handling, surface passivation, light management, and metallization – and high efficiencies were achieved for each route by focusing on these.

In the last five years, the primary cost driver of installed photovoltaic systems has shifted away from the cost of the silicon wafer and towards efficiency. Fortunately, as we have demonstrated here, it is possible to simultaneously increase efficiency while decreasing silicon consumption in industry-relevant solar cells. Furthermore, thinner wafers increase profitability of *cell* manufacturers specifically, since their costs decrease and the performance of their product increases. The present thrusts in the photovoltaics community to develop passivated contacts – many of which are deposited at low temperature – and novel structures that better trap infrared light are complementary to a transition to thin wafers, and thus we expect to see efficiencies climb well above 20% in the near future.

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